Preliminary solutions to exam in TSTE 87 ASIC for DSP 2007-03-17

1. a) The scheduling time must be larger than or equal to:
The sample period
The largest execution time of a process
An integer multiple of the sample period such that the scheduling period is an integer time unit.

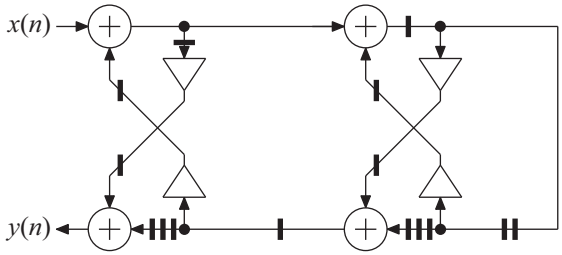
   b) Avoid overflow
Reduce round-off noise by utilizing the numerical range

   c) Bit-reversed for FFTs
Modulo adressing for cyclic buffers used in FIR filters

   d) 2's complement: W/2
CSD: W/3

   e) Less memory accesses
Less flexible schedule

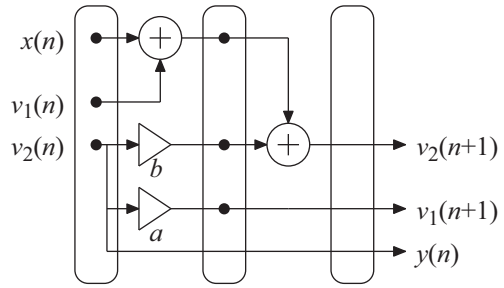
2.



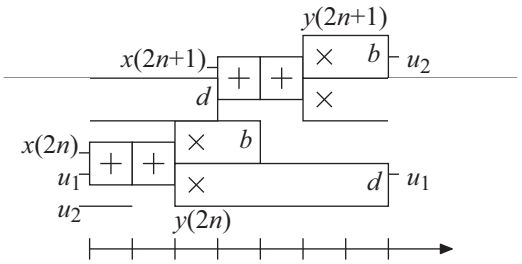
3. a) $T_{min} = max\left\{\frac{2+1}{1}, \frac{5+1+1}{2}\right\} = 3.5$ t.u.

   b) $T_{cp} = 5$ t.u.

   c)

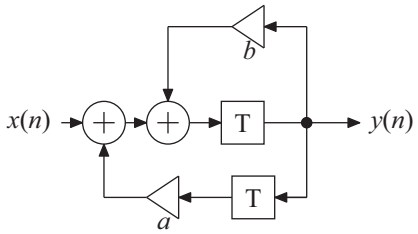


d)



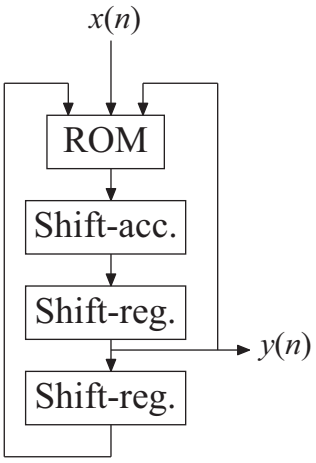
e) $T_{min} = 3.5$ t.u. Reordering additions gives $T_{min} = 4$ t.u., so no improvement.

4. Retime so that one DA unit can be used:



$$\begin{bmatrix} v_1(n+1) \\ v_2(n+1) \\ y(n) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ a & b & 1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1(n) \\ v_2(n) \\ x(n) \end{bmatrix}$$

a)



b)

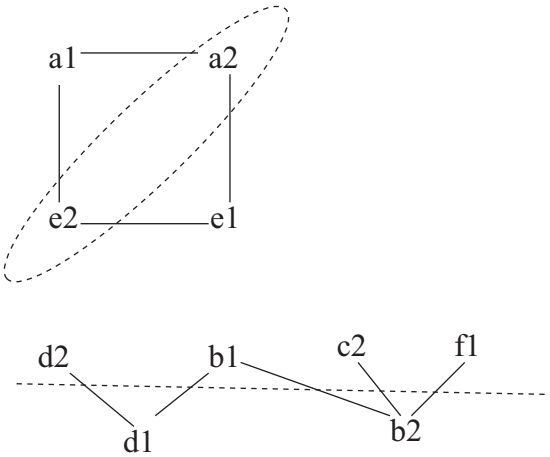
x(n)	$v_1(n)$	$v_2(n)$	ROM value	Two's complement
0	0	0	0	00.000000
0	0	1	b = –1/4	11.110000
0	1	0	a = 23/64	00.010111
0	1	1	a + b = 7/64	00.000111
1	0	0	1	01.000000
1	0	1	1 + b = 3/4	00.110000
1	1	0	1 + a = 87/64	01.010111
1	1	1	1 + a + b = 71/64	01.000111

c) The latency is equal to the number of fractional bits, i.e., 6 clock cycles.

d) $T_{min} = \left\{\frac{6}{1}, \frac{6}{2}\right\} = 6$ clock cycles

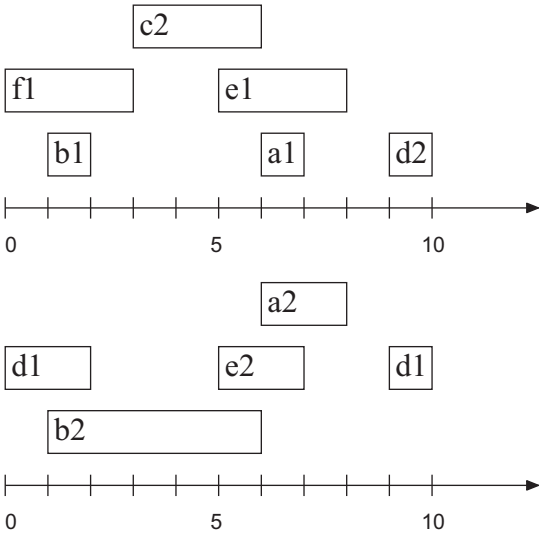
e) $a = 0.359375 = 0.010111_{2c} = 0.10\bar{1}00\bar{1}_{CSD}$

5. a) Derive an exclusion graph as shown below based on concurrent read/write. a1 denotes upper result from process a, etc.

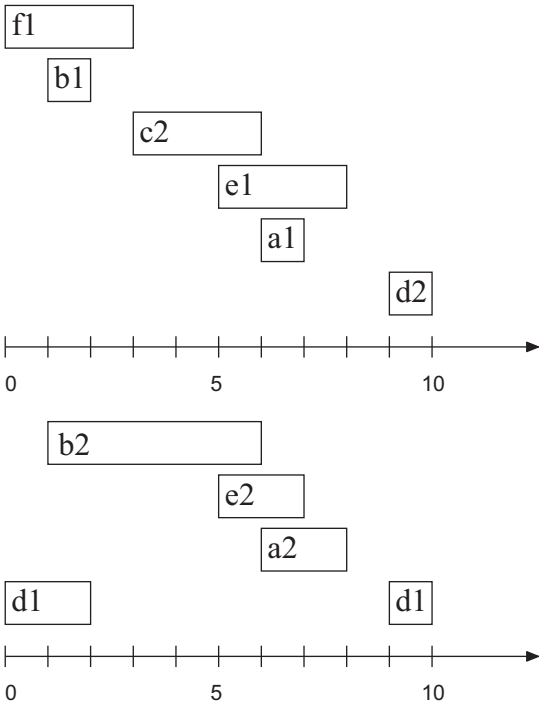


The exclusion graph is in fact two disjoint graphs. Find a disconnecting cut. Results in two sets of memory variable sets:
{{a1, e1}, {a2, e2}}
{{b1, d2, c2, f1}, {d1, b2}}
Pick one subset from each set and assign to a memory. In total two memories are required.

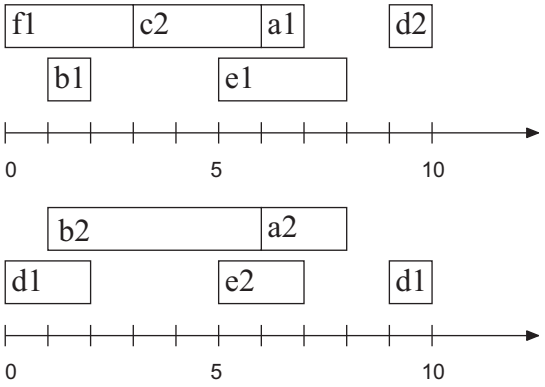
b) We select {a1, e1} and {b1, d2, c2, f1} for one memory and {a2, e2} and {d1, b2} for the second. We choose to use the left-edge algorithm.
Extracted memory variables:



Sorted according to start time:



Result after allocation and assignment:



c) $PE_{min} = \left\lceil \frac{3 \cdot 6}{10} \right\rceil = 2$