First solution approach

1. a) The number of partial products is halfed (for radix-2 Booth coding)

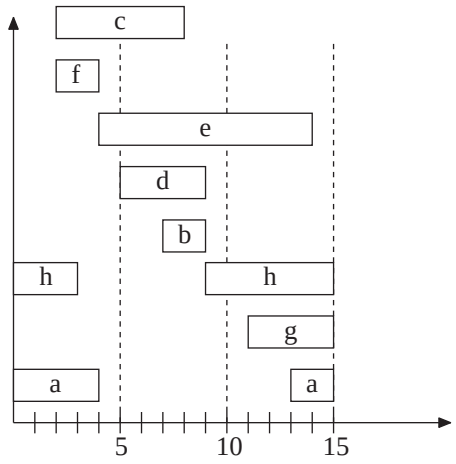
   b) Signed digit, carry-save, residue number systems.

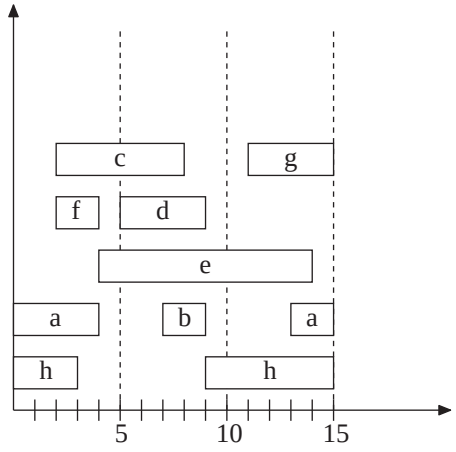
   c) No, there are no feedback loops in the SFG.

   d) Quantization noise, parasitic oscillations, overflow.

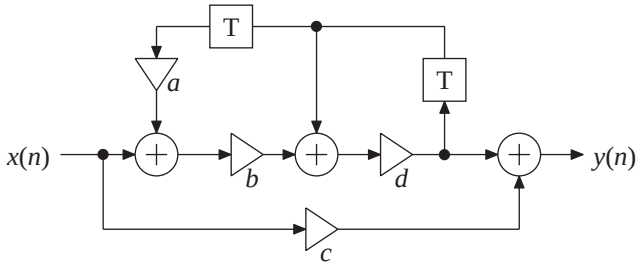
   e) Broadcasting, cache memory, interleaving, interprocess communication.

2. Sort according to starting time and assign,





3. Filtret nedan skall implementeras med en arkitektur som använder delat minne. Beräkningselementen är icke-homogena och non-preemptive. Latencyn är två tidsenheter för multiplikationerna *a* och *b*, fyra tidsenheter för multiplikationerna *c* och *d*, och en tidsenhet för additioner.
The filter below is to be implemented using a shared memory architecture. The processing elements are non-homogenous and non-preemptive. The latency is two time units for the multiplications a and b, four time units for the multiplications c and d, and one time unit for the additions.



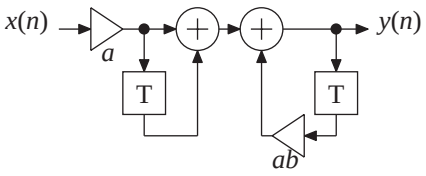
a) $$T_{min} = max\left\{\frac{T_a + T_b + T_d + 2T_{add}}{2}, \frac{T_d + T_{add}}{1}\right\} = max\{5, 5\} = 5 \text{ t.u.}$$

b) $T_{cp} = T_a + T_b + T_d + 3T_{add} = 11$ t.u.

c) Rita signalflödesgrafen i precedensform.
Draw the signal-flow graph in precedence form. (6)

d) Schedulera algoritmen så att $T_{sample} = T_{min}$.
Schedule the algorithm so that $T_{sample} = T_{min}$. (8)

4. For example:



5. a) $$\begin{bmatrix} v_1(n+1) \\ v_2(n+1) \\ y(n) \end{bmatrix} = \begin{bmatrix} d & abd & bd \\ 1 & 0 & 0 \\ d & abd & bd + c \end{bmatrix} \begin{bmatrix} v_1(n) \\ v_2(n) \\ x(n) \end{bmatrix} = \begin{bmatrix} \frac{3}{8} & -\frac{9}{256} & \frac{9}{64} \\ 1 & 0 & 0 \\ \frac{3}{8} & -\frac{9}{256} & \frac{65}{64} \end{bmatrix} \begin{bmatrix} v_1(n) \\ v_2(n) \\ x(n) \end{bmatrix}$$

b) Beskriv arkitekturen. Använd byggblock som skiftackumulatorer, skiftregister, ROM, etc.

Describe the architecture. Use building blocks such as shift accumulators, shift registers, ROM, etc. (6)

c) ROM for $v_1(n+1)$

Indata (v_1, v_2, x)	Value	2's complement
000	0	0.00000000
001	9/64	0.00100100
010	-9/256	1.11110111
011	27/256	0.00011011
100	3/8	0.01100000
101	33/64	0.10000100
110	87/256	0.01010111
111	123/256	0.01111011

ROM for $y(n)$

Indata (v_1, v_2, x)	Value	2's complement
000	0	00.00000000
001	65/64	01.00000100
010	-9/256	11.11110111
011	251/256	00.11111011
100	3/8	00.01100000
101	73/64	01.01100100
110	87/256	00.01010111
111	347/256	01.01011011

d) The latency is 8 clock cycles for both ROMs.

e) The minimal sample period is max{8/1, 8/2} = 8 clock cycles.

f) The latencies for the multipliers are 2, 3, 3, and 3 clock cycles for multiplier a, b, c, and d, respectively. Hence, we have T_{min} = max{(2+3+3)/2, 3/1} = 4 clock cycles.

g) Rita ett schema för de två multiplikationerna *b* och *c* genom att använda en förenklad bitseriell/parallel multiplikator baserad på CSD representation. Använd byggblock som fulladderare, D-vippor och logiska grindar.
Draw the schematic for the two multiplications b and c by using a simplified bit-serial/parallel multiplier based on CSD representaion. Use building blocks such as fulladders, flip-flops, and logic gates. (4)