Exam solutions ASIC (TSTE81) 000504

1. a) Yes. Example: 2nd order recursive halfband direct form filter structure. The algorithm has 2 operations. If T_{mult} = 3 time units and T_{add} = 1 time unit is T_{min} = (3+1)/2=2 time units. A schedule with T_{sample} = T_{min} requires 3 concurrent operations, thus three processing elements (assuming an execution time equal to the latency of the PE).

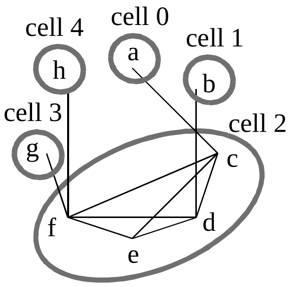
   b) Lookahead FSM, concurrent block processing

   c) No, the value of T_{min} may be any quotient. Example: 2^{nd} order halfband recursive direct form filter. Assume latency of multiplier to be 2 and adder to be 1. Then T_{min} = (2+1)/2 = 1.5.

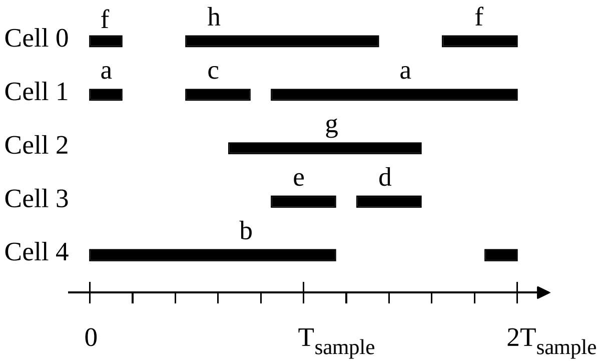
   d) CSDC (Canonic Sign Digit Code) is a non-redundant number representation. Each value has one unique representation in this number system.

   e) Standard-Cell Design, Gate Array Design, Sea-of-Gates Design, Unconstrained Design.

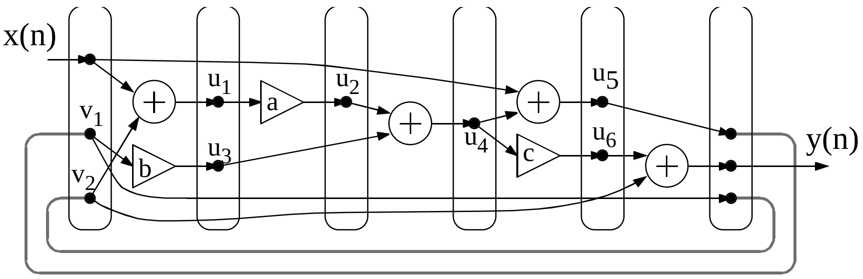
2. a) Connect variables that can share memory cells. Find minimal number of cliques (fully connected subgraphs):



   b) Sort variables by start time: h, c, g, a, e, d, f, b. Allocate memory cell and search for assignable variables starting from left in list. Remove variable from list when assigned. When list not empty and no variable possible to assign to current cell then allocate a new cell.



3. a)



b) $u_1 := x(n) + v_1;$
$u_3 := b\,v_1;$

$u_2 := a\,u_1;$

$u_4 := u_2 + u_3;$

$u_5 := x(n) + u_4;$
$u_6 := c\,u_4;$

$y(n) := u_6 + v_2;$

$v_2 := v_1;$

$v_1 := u_5;$

c)
$u_4 := a(x(n) + v_1) + bv_1;$

$y(n) := cu_4 + v_2;$

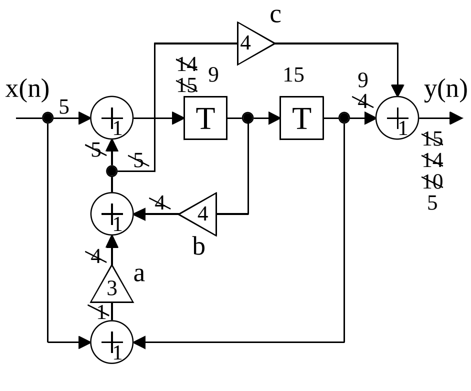
$v_2 := v_1;$

$v_1 := x(n) + u_4;$

4. a) Multiplication latency is equal to number of fractional bits in the coefficient plus one due to model 1 logic.

   $T_a = 2+1 = 3$ clock cycles. $T_b = 3+1 = 4$ clock cycles. $T_c = 3+1 = 4$ clock cycles.

   b) Number of clock cycles per sample = 150 MHz / 10 MSamples/s = 15 clock cycles/sample. Replace all T-element with 15 flipflops and add 15 flipflops to the output. Propagate them so all operations gets computation time.



5. a) $T_{min} = \max(T_{opi}/N_i) = (4+1)/2 = 2.5$ clock cycles. $f_{max} = f_{clk}/T_{min} = 70/2.5 \approx 28$ MSamples/s.

   b) The multiplication operation is longer than the sample period and the critical loop contains two delay elements. Must therefore schedule over more than one sample period. Use two sample periods.

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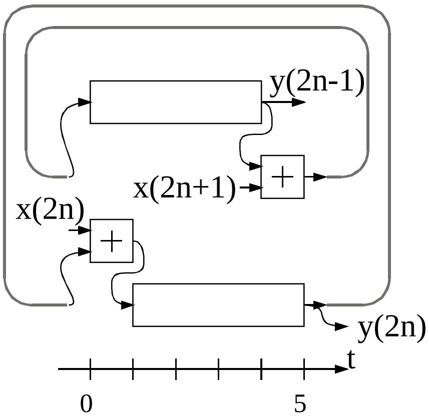
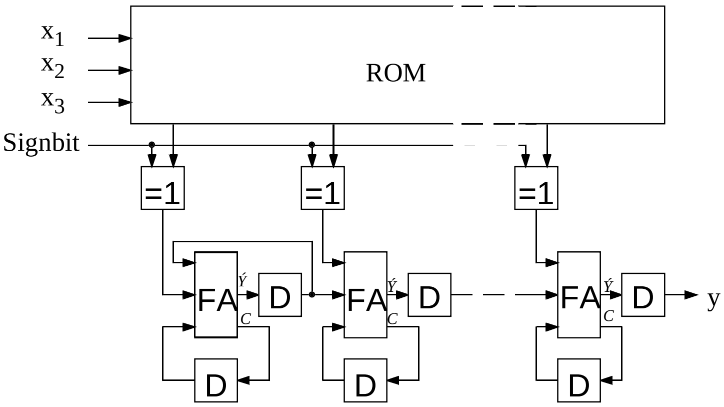


6. a) Reset all flipflops before starting the computation. Signbit is one when signbit of x_i is input, zero otherwise.



b) The largest number is larger than 1, so the number range must be increased from [-1,1[to [-2,2[.

x_1 x_2 x_3	ROM value
0 0 0	00.000_{2C} (0_{10})
0 0 1	00.111_{2C} (0.875_{10})
0 1 0	11.101_{2C} (-0.375_{10})
0 1 1	00.100_{2C} (0.5_{10})
1 0 0	00.010_{2C} (0.25_{10})
1 0 1	01.001_{2C} (1.125_{10})
1 1 0	11.111_{2C} (-0.125_{10})
1 1 1	00.110_{2C} (0.75_{10})