Exam solutions ASIC (TSTE81) 000316

1. a) Theorem 6.1: Every directed loop in the signal-flow graph must contain at least one delay element.

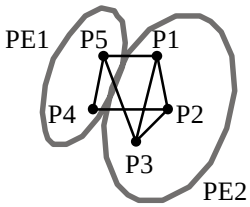
   b) Addition can be made using constant time (independent on the word length) as shown in Example 11.4. Extraction of the sign requires the detection of the first non-zero digit from the left, which requires a sequential scan of the bits. This is as costly as a ripple carry addition, and for larger wordlengths is this time longer than the addition time.

   c) Carry-Look-Ahead, Carry-Select, Carry-Skip, Conditional Sum.

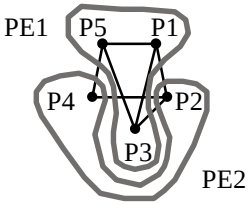
   d) An exclusion graph should be used when there are few processes (operations or variables) that can not share a resource. The graph will then contain few arcs. The opposite (few processes that can share a resource) will generate a graph with many arcs. It is then harder to find a good set of subgraphs that covers exclusion graph.

   e) Moore and Mealy machines.

2. a) Two alternatives:

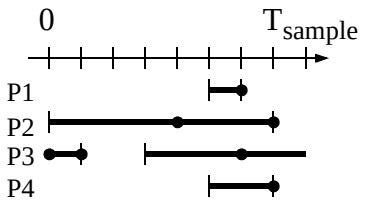


or

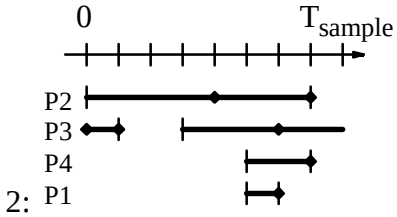


   b) 1: Extract the lifetime diagram for the variables.
   2: Create a sorted list of the variables according to starting time and length.
   3: Allocate a memory cell and assign the first variable in the list from left that fits into the cell. Remove the assigned variable from the list. Do this until no more variables fit the list. Allocate another memory cell if the list is not empty.

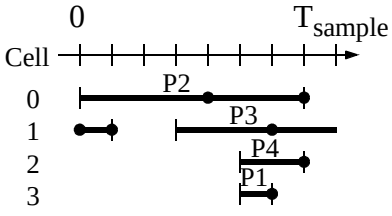
1:



2:



3:



3. a) Name delay element outputs from left to right in the figure (v_1 to the left, v_4 to the right).

$v_1(n+1) = x(n)$
$v_2(n+1) = v_1(n)$
$v_3(n+1) = v_4(n)$
$v_4(n+1) = \alpha\, x(n)-(v_2(n) + v_3(n))) = \alpha\, x(n) - \alpha\, v_2(n) - \alpha\, v_3(n)$
$y(n) = \alpha\, x(n) + v_1(n) + (1- \alpha)v_2(n) + (1- \alpha)v_3(n)$

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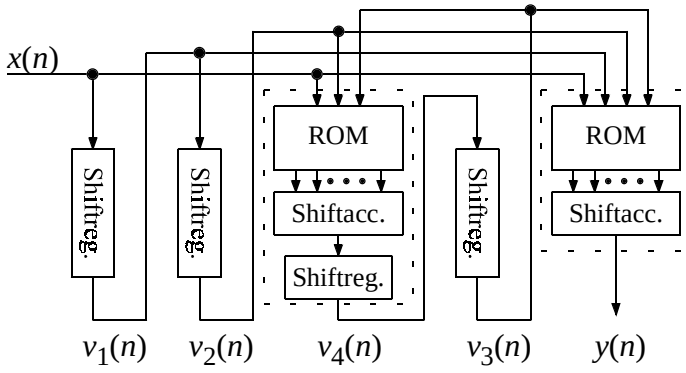


The shiftregister after the shiftaccumulator is really a shimming delay and is included in the Distributed Arithmetic unit.

$x(n)$	$v_2(n)$	$v_3(n)$	$v_4(n+1)$
0	0	0	0 = 0.000
0	0	1	-0.125 = 1.111
0	1	0	-0.125 = 1.111
0	1	1	-0.25 = 1.110
1	0	0	0.125 = 0.001
1	0	1	0 = 0.000
1	1	0	0 = 0.000
1	1	1	-0.125 = 1.111

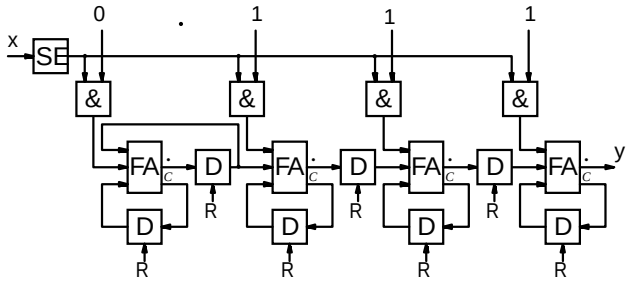
b)

In the $v_4(n+1)$ ROM is it enough to store 2 bit words.

Only positive values are store in the $y(n)$ ROM. Bits 2 and 3 are also identical. It is therefore enough with 4 bit words.

$x(n)$	$v_1(n)$	$v_2(n)$	$v_3(n)$	$y(n)$
0	0	0	0	0 = 00.000
0	0	0	1	0.875 = 00.111
0	0	1	0	0.875 = 00.111
0	0	1	1	1.75 = 01.110
0	1	0	0	1 = 01.000
0	1	0	1	1.875 = 01.111
0	1	1	0	1.875 = 01.111
0	1	1	1	2.75 = 10.111
1	0	0	0	0.125 = 00.001
1	0	0	1	1 = 01.000
1	0	1	0	1 = 01.000
1	0	1	1	1.875 = 01.111
1	1	0	0	1.125 = 01.001
1	1	0	1	2 = 10.000
1	1	1	0	2 = 10.000
1	1	1	1	2.875 = 10.111

4. a) $0.875 = 0.111_2$. The signal R resets the flip-flops before the first bit of the input arrives. A sign extension signal should also be used to sign extend the input data.



b) Simplifications: 1: Remove the first bitslice. 2: Simplify the second bitslice to a single flipflop. 3: Remove all AND-gates.

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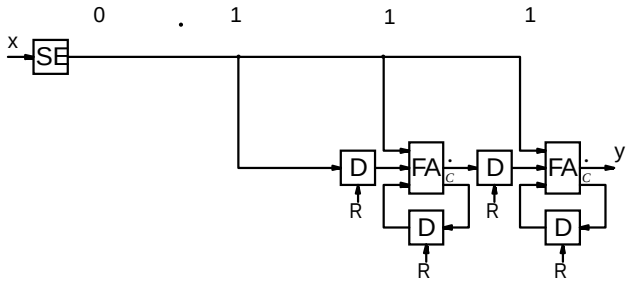
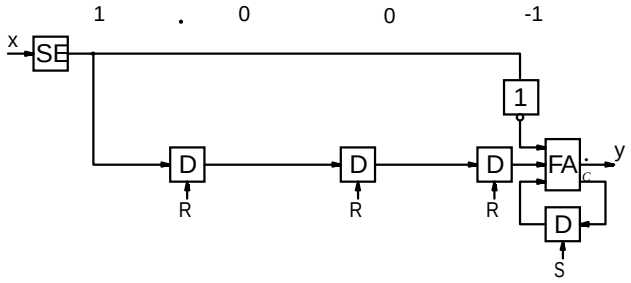
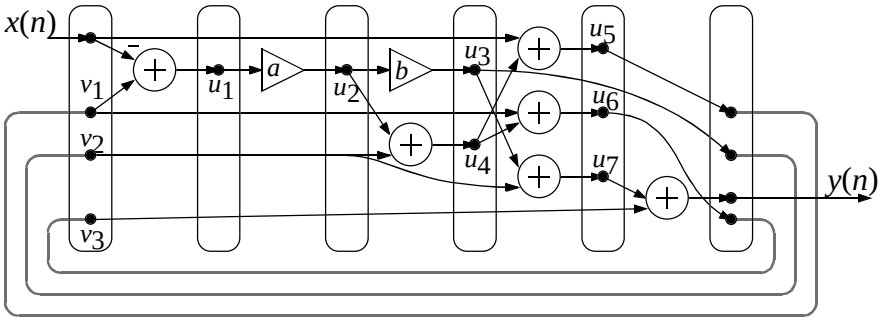


c) $0.111_2 = 1.00\text{-}1_{SDC}$. Note that the first 1 in an SDC is not a sign bit in the same way as for 2´s complement. It has a positive weight, so the sign extension feedback in the first bitslice must not be included. An additional set signal for the carry flipflop in the last bitslice is used to generate the LSB for the subtraction in the last bitslice.



5. a) $T_{min} = \max\{(T_{add} + T_a + T_{add} + T_{add})/1 , (T_{add} + T_a + T_b + T_{add} + T_{add})/2 \} = \max\{(1+3+1+1)/1 , (1+3+4+1+1)/2 \}) = \max(6, 5) = 6$ time units.

b)



c) Move the last two additions to the next sample period.