9.15 a) The number of adaptors per second is

$$N_{op} = 2\cdot(8 + 4\cdot 2 + 2\cdot 2^2 + 2\cdot 2^3) = 80$$

The sample rate is 44.1 kHz. The number of processors is

$$N_p = \frac{80\cdot 44.1\ 10^3\cdot 24}{120\ 10^6} \approx 0.706 < 1$$

The processor schedule is sequential since only one processor is used.

b) See Problem 9.13.

c) We execute $80\cdot 44.1\ 10^3$ adaptor operations per second. The I/O bit rate for the processor is: $80\cdot 44.1\ 10^3\cdot 24 \approx 85$ MHz

d) The number of bit/s through the cut A-A' is

$$(2 + 2)\cdot 80\cdot 44.1\ 10^3\cdot 24 = 338.7 \text{ Mbit/s}$$

and through the cut B-B': $\frac{N_m\cdot W_m}{T_{RAM}} = \frac{N_m\cdot W_m}{17\ 10^{-9}} \Rightarrow$

$$\Rightarrow \quad N_m = \frac{338.7\ 10^6\cdot 17\ 10^{-9}}{W_m}$$

We select $W_m = 22 \Rightarrow N_m \approx 0.26 < 1$

e) The memory requirement is less than the number of outputs, i.e., less than 64 × 22-bit words or 1408 bits. An lower estimate of the memory requirement is equal to the number of delay elements, i.e., 32 × 22-bit words or 704 bits.

f) We select one RAM with at least 32 × 22-bit or jet better 64 × 22-bit words.

g) We have already selected W_m = 22. The access rate for the RAM is selected so that a balanced architecture is obtained.

$338.7\ 10^6 = 1\cdot 22\cdot f_m$

$\Rightarrow f_m \approx 15$ MHz

-Oj, ni har helt rätt Sir Dwayne. När jag knackar här börjar han surra och han är ARG!

O yes, you are correct Sir Dwayne. When a knock he starts to buzz and he is really angry.