9.10 a) A shared-memory architecture is selected.

b) The number of bits/s to and from the processors are $\dfrac{2N_{PE}}{T_{PE}}$

The number of bits/s to and from the memories are:

$$\frac{W_{RAM} \, N_{RAM}}{T_{RAM}}$$

These transmission rates should be equal for an ideal architecture. Hence, we have

$$N_{RAM} = \frac{2N_{PE} \, T_{RAM}}{W_{RAM} \, T_{PE}}$$