2.5 Determine the largest current through both of the transistors during switching. We have the same current $I_{Dn} = -I_{Dp}$ and gate-source voltage for the n-device is V_m and $(V_m - V_{DD})$ for the p-device, respectively. V_m is the gate-source voltage when the current is maximum. Since, both devices are in the saturation region we get:

$$\frac{\mu_n C_{ox} W_n}{2 L_n} (V_m - V_{Tn})^2 = \frac{\mu_p C_{ox} W_p}{2 L_p} (V_{DD} - V_m + V_{Tp})^2$$

Solving for V_m we get $V_m = \dfrac{V_{DD} + V_{Tp} + \sqrt{a}\, V_{Tn}}{1 + \sqrt{a}}$

where $a = \dfrac{\mu_n W_n}{\mu_p W_p}$

Now, assume that $a = 1$, i.e., symmetric switching

$$\Rightarrow V_m = \frac{V_{DD} + V_{Tp} + V_{Tn}}{2} = \frac{V_{DD}}{2} \quad \Rightarrow$$

$$I_{Dn} = \frac{\mu_n C_{ox} W_n}{2 L_n} \left(\frac{V_{DD}}{2} - V_{Tn}\right)^2 =$$

$$= \frac{(5.6\ 10^{-2})(3.9)(8.85\ 10^{-12}) W_n}{(2)(100\ 10^{-10})\ L_n} \left(\frac{5}{2} - 0.75\right)^2 \approx 332 \frac{W_n}{L_n} \quad [\mu\text{A}]$$

where $C_{ox} = \dfrac{\varepsilon_r\, \varepsilon_0}{T_{ox}}$

Rumors has it that the n- and p-transistors in the inverter that drives the global clock in the *Alpha*™ chip (Digital Equipments) has a combined widths of about 10 cm and 14 cm, respectively. The minimum feature size in the CMOS process is a 0.75 µm, but the channel length is 0.5 µm. The chip runs at 200 MHz and consumes about 30 W at 3.3 V. The number of devices is $1.68\ 10^6$ on a 16.8×13.9 mm chip. Current high-performance chips consume 40 to 80 W at 1.8 V.

We guess that $T_{ox} \approx 100$ Å. We have

$$\beta = \frac{\mu_n\ \varepsilon\, W}{T_{ox} L} = \frac{(5.6\ 10^{-2})(3.9)(8.85\ 10^{-12}) W}{(100\ 10^{-10}) L} = 193\ 10^{-6} \frac{W}{L} \quad [\text{A}]$$

The resulting drain current becomes

$$I_{Dn} \approx 193\ 10^{-6} \frac{10\ 10^{-2}}{0.5\ 10^{-6}} = 38.6 \text{ Amperes}$$

Obviously, it is not possible to have such a large current! Special measures must be employed in order to avoid such large currents.