11.33 A bit-parallel implementation of complex multiplier using distributed arithmetic is implemented in Alcatel Mietec™ 0.35μm standard CMOS technology. In this bit-parallel complex multiplier, the shift-accumulator in Figure 11.48 is replaced with adder trees.

The main differences between the bit-parallel complex multiplier are: not need serial/parallel or parallel/serial interface is needed in bit-parallel implementation, the clock frequency is much more slower in bit-parallel implementation than that of bit-serial implementation, the glitch inside the bit-parallel multiplier is much larger than the bit-serial one, the accumulation of partial products can use, for example, tree structures for the bit-parallel implementation, the bit-serial implementation occupy obviously less area than the bit-parallel counterpart etc. The most important in the implementation style discussion is to know the advantages and disadvantages for bit-serial and bit-parallel (possible digit-serial) implementations.