11.1 Assume that the input data are prescaled so that no overflow exits, assume also that the bit-parallel adder are two ripple-carry-adders.

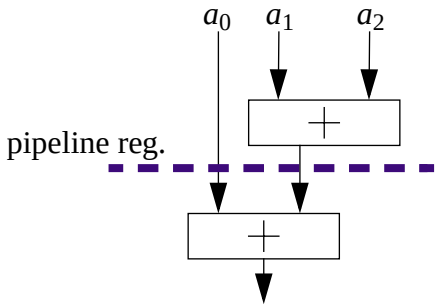
(a) The addition time for adder 1 and 2 is $(N-1)t_{carry} + t_{sum}$. Note that the addition for adder 2 can start as the LSB in the sum of a_1 and a_2 is available, i.e., the delay time is only t_{sum}.

The total addition time is $((N-1)t_{carry} + t_{sum}) + t_{sum} = 19t_{carry} + 2t_{sum} = 42$ ns

(b) The pipelining can be inserted at both word-level and bit-level.

The latency is two clock periods, where one clock period must be larger than $(N-1)t_{carry} + t_{sum}$, or 40 ns.

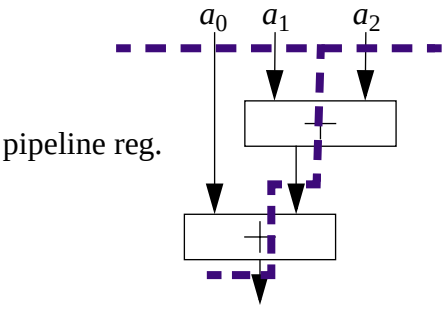
For the word-level, the new throughput is $\frac{1}{(N-1)t_{carry} + t_{sum}} = \frac{1}{40 \times 10^{-9}}$ (sample/s), or 25 Msample/s.



Word-level pipelining

The bit-level pipelining is more efficient.

Set the pipeline register at the $\left\lceil \frac{N}{2} \right\rceil$ th full adder of the first adder and the $\left\lceil \frac{N}{2} + 1 \right\rceil$ th full adder of the second adder.



Bit-level pipelining

The addition time is

$$max\left\{\left(\left\lceil \frac{N}{2} - 1 \right\rceil\right)t_{carry} + 2t_{sum}, \left(N - \left\lceil \frac{N}{2} \right\rceil - 1\right)t_{carry} + t_{sum}\right\} = 22 \text{ ns.}$$

The new throughput is about 45 Msample/s.

The latency in this case is to clock periods with clock period no less than 22 ns.