Linköping Institute of Technology
Department of Electrical Engineering, Division of Integrated Circuits and Systems

Exam TEN1 in TSTE86 Digital Integrated Circuits

Time:	Monday 21 October 2019, 14:00–18:00
Place:	TER4, TERE
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aid:	Calculator
Maximum score:	60 points
Grades:	45 points for 5 35 points for 4 25 points for 3
Solutions:	Posted on the course web
Result:	Posted through LADOK by Wednesday 6 November 2019

1. The function $F = AB + \overline{CD}$ shall be implemented. Complements to the inputs are *not* available.

   a) Implement the function with a static CMOS gate and static CMOS inverters. (5 p)

   b) Size all transistors so that the worst-case output resistance of the gate and inverters is the same as that of an inverter with an NMOS W/L = 3 and PMOS W/L = 5. (5 p)

2. Given the data in Fig. 1 for a short channel NMOS transistor with V_{DSAT} = 0.58 V and k' = 122 µA/V^2, calculate the parameters below.

   a) V_{T0} (3 p)

   b) γ (3 p)

   c) $2|\phi_F|$ (3 p)

   d) W/L (3 p)

Data set	V_{GS} (V)	V_{DS} (V)	V_{BS} (V)	I_D (µA)
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	–1	1146
5	2	1.8	–2	1039

Figure 1. Measured NMOS transistor data.

3. A precharged 2-input NAND gate shall be designed.

   a) Draw the transistor schematic of the gate. (4 p)

   b) Explain the operation of the gate. (4 p)

   c) Explain how charge sharing may occur. (4 p)

4. Consider a *static random-access memory* (SRAM) with full-VDD precharge of the bit-lines and sense amplifiers connected to the bit-lines.

   a) Draw the transistor schematic of a six-transistor CMOS SRAM cell. (3 p)

   b) Describe a write operation of the SRAM cell. (2 p)

   c) Describe a read operation of the SRAM cell. (2 p)

   d) Briefly discuss considerations in sizing the cell's MOSFETs. (3 p)

5. A chip floorplan with a metal wire connecting the five fixed nodes A-E is shown in Fig. 2. The wire characteristics are C_{area} = 0.060 fF/μm2 and R_{sheet} = 0.25 Ω/square. Assume a uniform wire width W_{wire} = 4.0 μm and neglect inductance.

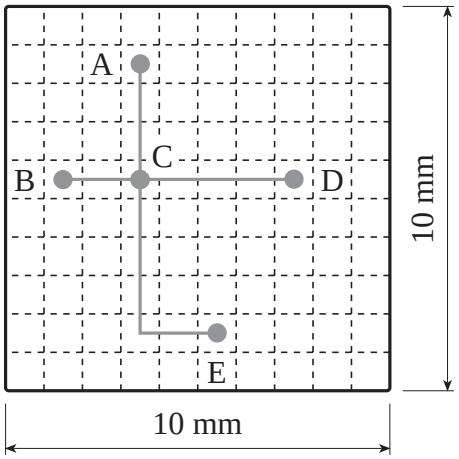

Figure 2. Chip floorplan with a metal wire connecting five nodes

a) Calculate the resistance and capacitance of the segments A-C, B-C, C-D, and C-E. (2 p)

b) Model the entire interconnect using simple π-models of the segments. (2 p)

c) Model the entire interconnect using simple T-models of the segments. (2 p)

d) How much do the results differ between the two different models in b) and c) if the Elmore delay model is used to calculate the propagation delay from node A to E? (2 p)

6. Describe the steps of the semicustom design flow below with one or two sentences per step.

a) Logic synthesis. (2 p)

b) Placement. (2 p)

c) Routing. (2 p)

d) Tape out. (2 p)

Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***V_{DSAT}* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{V}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq}C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.