Linköping Institute of Technology
Department of Electrical Engineering, Division of Integrated Circuits and Systems

Exam TEN1 in TSTE86 Digital Integrated Circuits

Time:	Friday 30 August 2019, 8:00–12:00
Place:	TER4
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aid:	Calculator
Maximum score:	60 points
Grades:	45 points for 5 35 points for 4 25 points for 3
Solutions:	Posted on the course web
Result:	Posted through LADOK by Tuesday 17 September 2019

1. The function $F = A\bar{S} + BS$ shall be implemented. Complements to the inputs are *not* available.

   a) Implement the function with a static CMOS gate and two inverters. (5 p)

   b) Size all transistors so that the worst-case output resistance of the gate and inverters is the same as that of an inverter with an NMOS $W/L = 3$ and PMOS $W/L = 4$. (5 p)

2. A resistive-load inverter connected to a capacitive load C_L is shown in Fig. 1. Calculate values on R_L that yield the properties below.

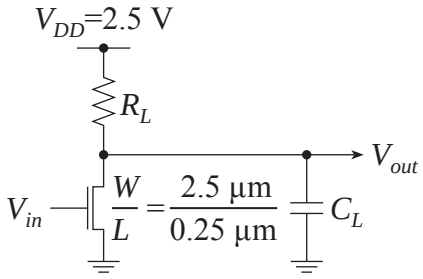

Figure 1. Resistive-load inverter with a capacitive load.

   a) An inverter switching threshold V_M equal to $V_{DD}/2$. (4 p)

   b) Equal rise and fall time ($t_{pHL} = t_{pLH}$). (6 p)

3. A uniform wire has the total resistance R and capacitance C.

   a) Make an RC-chain model of the wire consisting of N identical segments. (2 p)

   b) Calculate the dominant time constant of the wire model using the Elmore formula. (4 p)

   c) Calculate the dominant time constant of the wire for large N. (2 p)

   d) Calculate the propagation delay of for large N. (2 p)

4. State five circuit techniques for reducing the problems with capacitive cross talk in circuit design. (10 p

5. A positive edge-triggered master-slave D flip-flop shall be designed.

a) Use inverters and transmission gates to design a D flip-flop that transfers the logical value at the input *D* to the output *Q* when the clock rises from low to high. (5 p)

b) Sketch a timing diagram that illustrates the transfer of both a low and a high logical value from *D* to *Q*. Include the clock, input, and output nodes, as well as the intermediate node between the two latches. Define the *setup time*, *hold time* and *clock-to-output delays* (high-to-low and low-to-high). What can happen if the setup time or hold time is violated? (5 p)

6. Draw block schematics of the adders below. Indicate critical paths in your drawings.

a) Ripple-carry adder. (2 p)

b) Ripple-carry adder with inverter elimination in carry path. (2 p)

c) Carry-bypass (carry-skip) adder. (3 p)

d) Carry-select adder. (3 p)

Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***V_{DSAT}* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{V}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq}C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.