Linköping Institute of Technology
Department of Electrical Engineering, Division of Integrated Circuits and Systems

Exam TEN1 in TSTE86 Digital Integrated Circuits

Time:	Monday 7 January 2019, 14:00—18:00
Place:	TER1
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aid:	Calculator
Max score:	60 points
Grades:	45 points for 5 35 points for 4 25 points for 3
Solutions:	Posted on the course web
Results:	Posted through LADOK by 23 January 2019

1. A transistor schematic of a static CMOS gate is shown in Figure 1.

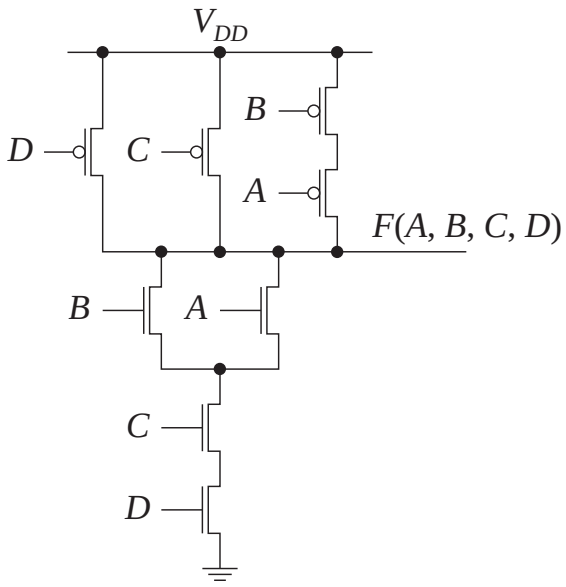

Figure 1. Static CMOS gate.

a) What logic function has been implemented? (2 p)

b) Show that the pull-up net and the pull-down net are complementary. (2 p)

c) Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 3$. (6 p)

d) What input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance? (4 p)

2. A precharged NOR gate shall be designed.

a) Draw the transistor schematic of the gate. (4 p)

b) Explain the operation of the gate. (4 p)

c) Explain how charge leakage may impose a limitation on the operation. (2 p)

3. Figure 2 shows a clock distribution network. Each segment of the clock network is 5 mm long, 3 μm wide, and is implemented in metal. At each terminal node (such as X) resides a load capacitance of C_L = 100 fF. Assume a 0.25 μm process with the following metal properties: parallel plate capacitance C_p = 0.088fF/μm^2, fringing capacitance C_f = 0.054 fF/μm, and sheet resistance R_{sq} = 0.1 Ω/square.

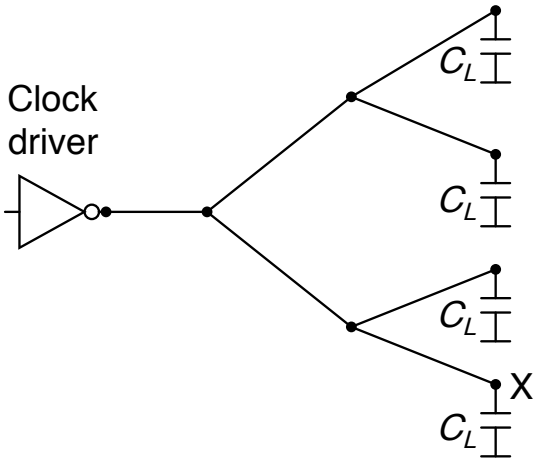

Figure 2. Clock distribution network.

a) Determine the average current of the clock driver, given a voltage swing on the clock lines of 2.5 V and a maximum delay of 1.25 ns between clock source and node X. For this part, you may ignore the resistance and inductance of the network. (3 p)

b) Unfortunately, the resistance of the metal cannot be ignored. Assume that each segment of the network can be modeled with a simple π model. Draw the equivalent circuit and annotate the values of resistors and capacitors. (3 p)

c) Determine the dominant time-constant of the clock response at node X using the Elmore delay formula. (4 p)

4. Draw the transistor schematic of a C^{2}MOS latch and explain its operation. (6 p)

5. Consider the signed, two's complement 4x4 bit array multiplier shown in Figure 3.

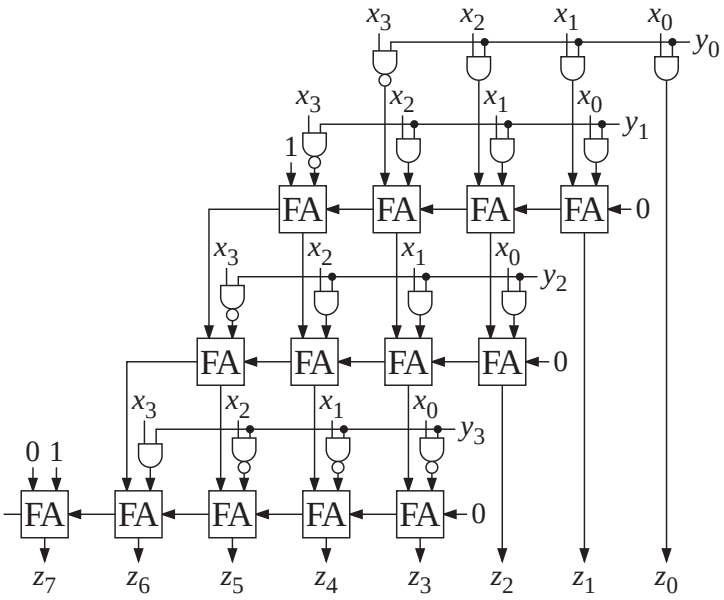

Figure 3. Two's complement multiplier.

a) Calculate the partial products in squaring the two's complement number 1001_{2C}. (4 p)

b) Estimate the delay of the critical path if a full adder has the propagation delay 0.7 ns, an AND gate 0.3 ns, and a NAND gate 0.2 ns. (3 p)

c) What full adders can be simplified in the multiplier above and how? (3 p)

6.

a) Define the terms controllability and observability. How are these properties related to an ad-hoc test? (6 p)

b) For the circuit given in Figure 4, find all test patterns *abc* for which stuck-at-0 fault at node *m* can be detected from the output *z*. (4 p)

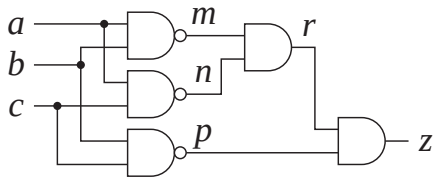

Figure 4. Combinational circuit.

Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***V_{DSAT}* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{V}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq}C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.