TSTE86 Homework 5: Solution

The clock skew between register 1 and 2 is $\delta = \Delta_{\mathbf{1}} - \Delta_{\mathbf{0}}$.

Constraint on minimum clock period

$$T_{clk} + \delta = T_{clk} + \Delta_{\mathbf{1}} - \Delta_{\mathbf{0}} \geq t_{c\text{-}q} + t_{logic} + t_{su}$$

$$\Rightarrow$$

$$\Delta_{\mathbf{0}} \leq T_{clk} + \Delta_{\mathbf{1}} - t_{c\text{-}q} - t_{logic} - t_{su} = 1000 + 300 - 250 - 500 - 150 \text{ ps} = 400 \text{ ps}$$

Constraint on minimum propagation delay

$$\delta + t_{hold} = \Delta_{\mathbf{1}} - \Delta_{\mathbf{0}} + t_{hold} < t_{c\text{-}q,cd} + t_{logic,cd}$$

$$\Rightarrow$$

$$\Delta_{\mathbf{0}} > \Delta_{\mathbf{1}} + t_{hold} - t_{c\text{-}q,cd} - t_{logic,cd} = 300 + 100 - 200 - 450 \text{ ps} = -250 \text{ ps}$$

However, for plain delay $\Delta_{\mathbf{0}} \geq 0$ ps

Range of delay Δ_0

Assuming normal clock and delay: $0 \text{ ps} \leq \Delta_0 < 400 \text{ ps}$

Assuming special clocking arrangement: $-250 \text{ ps} \leq \Delta_0 < 400 \text{ ps}$