TSTE86 Homework 5: Synchronization

The following times apply to the pipelined datapath shown in Figure 1:

Clock period	T_{clk}	=	1000 ps
Register, setup	t_{su}	=	150 ps
Register, hold	t_{hold}	=	100 ps
Register, max clock-to-output	$t_{c\text{-}q}$	=	250 ps
Register, min clock-to-output	$t_{c\text{-}q,cd}$	=	200 ps
Logic, max propagation	t_{logic}	=	500 ps
Logic, min propagation	$t_{logic,cd}$	=	450 ps

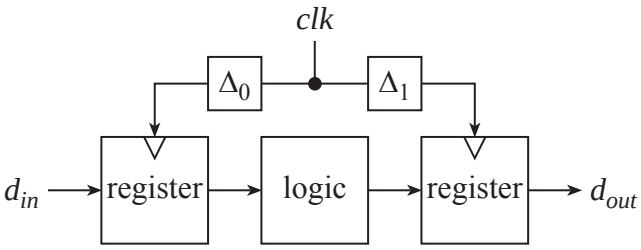

Figure 1. Pipelined datapath with clock delays Δ_0 and Δ_1.

The clock is delayed with Δ_1 = 300 ps to the right register. What range of delay Δ_0 is acceptable from the clock to the first register?