TSTE86 Homework 4: Interconnection

Consider a clock driver connected with a metal wire as shown in Figure 1. The wire has width W = 0.5 μm, sheet resistance r_W = 75mΩ/sq, area capacitance c_a = 30 aF/(μm)^2, and fringe capacitance c_f = 40 aF/μm.

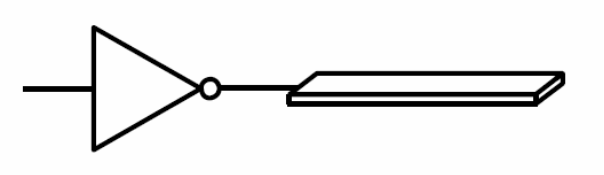

Figure 1. Clock driver loaded by metal wire.

a) Model the entire circuit. The driver is modeled with a voltage source V_{in}, a series resistor R_S, and a capacitor C_S to ground. The distributed wire is modeled with a lumped RC network (e.g. π model).

b) Use the Elmore model to find the wire length if the propagation delay in this circuit is twice the inherent propagation delay of the driver (delay without any load). Assume R_S = 7.25 kΩ and C_S = 6 fF.

c) What is the propagation delay of this circuit and what is the wire contribution in this case?

d) Assume the propagation delay of the wire is the same as the propagation delay of the driver when loaded by such a wire. Find the wire length and the propagation delay of this circuit.