TSTE 86 Digital IC Lecture 11: Manufacturing

Deyu Tu, PhD

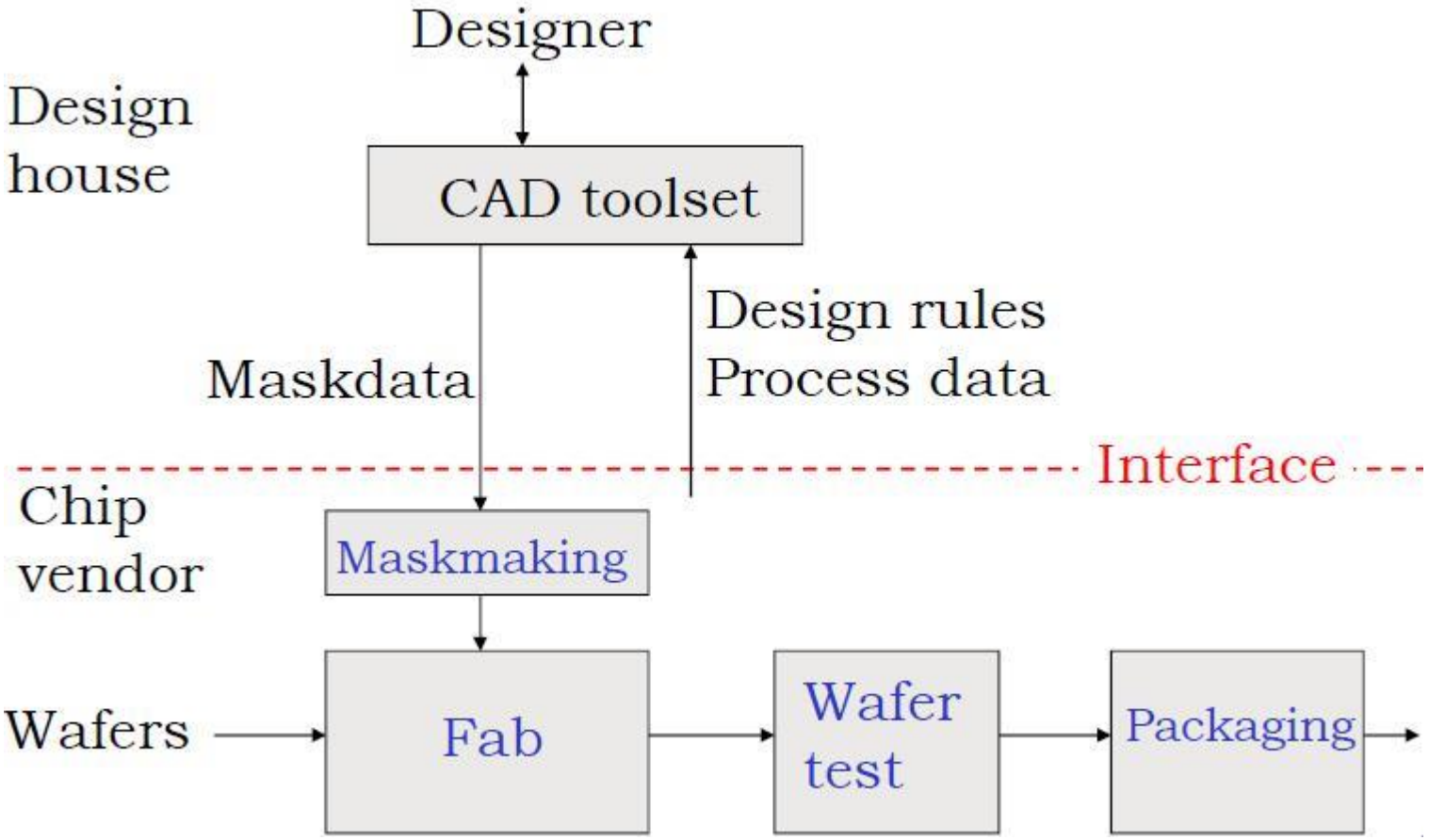
deyu.tu@liu.se
013-285851
Laboratory of Organic Electronics, Campus Norrköping

LINKÖPING UNIVERSITY

Outline

- Overview of the Full Process
- CMOS IC Manufacturing
- CMOS Process Enhancements
- Summary

Overview of the Full Process



Fab and Foundry

- *Fabs* (Fabrication plants) are expensive to develop and operate
- Some *Fabs* operate on a *foundry* model, selling space on the fab lines to fabless IC companies

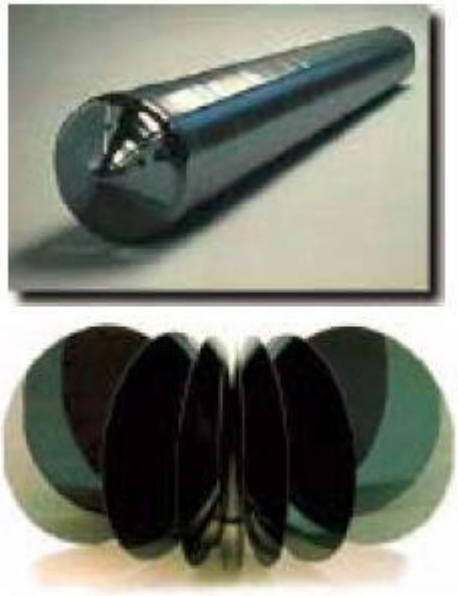
Cleanroom

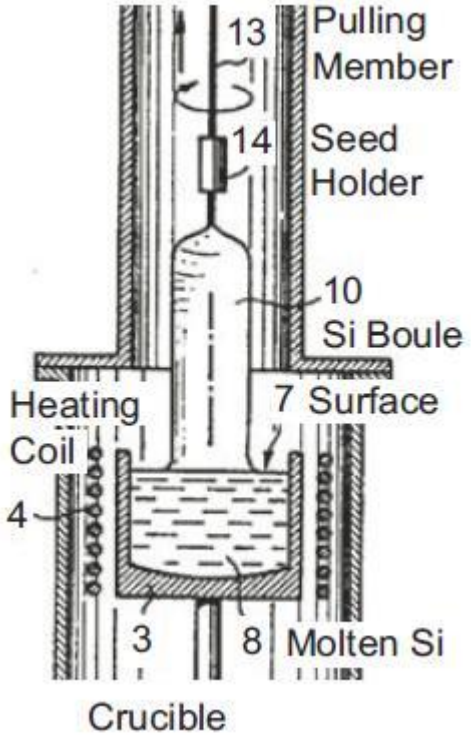
US FED STD 209E

Class	Maximum particles/ft^3					ISO equivalent
	≥0.1 µm	≥0.2 µm	≥0.3 µm	≥0.5 µm	≥5 µm	
1	35	7.5	3	1	0.007	ISO 3
10	350	75	30	10	0.07	ISO 4
100	3,500	750	300	100	0.7	ISO 5
1,000	35,000	7,500	3000	1,000	7	ISO 6
10,000	350,000	75,000	30,000	10,000	70	ISO 7
100,000	3.5×10^6	750,000	300,000	100,000	700	ISO 8

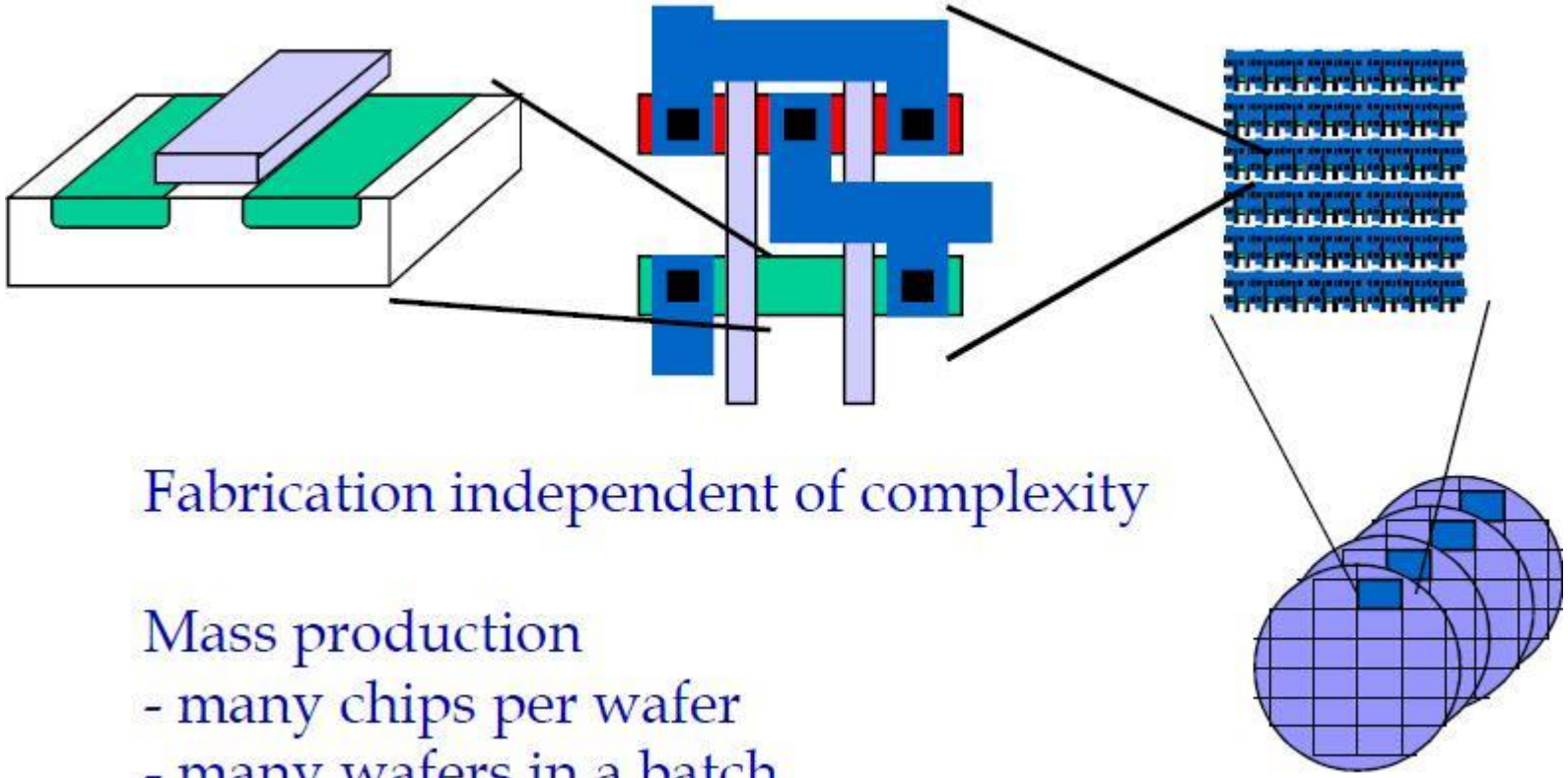
Wafer Formation-Czochralski Method

- Wafer diameter 100-300 mm (4'-12')
- Wafer thickness 525-775 μm





From Wafer to Transistors



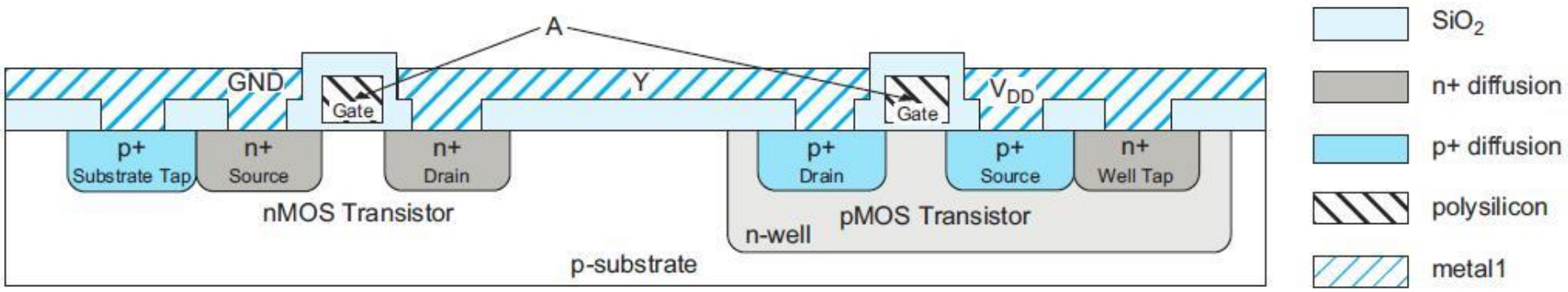
Fabrication independent of complexity

Mass production
- many chips per wafer
- many wafers in a batch

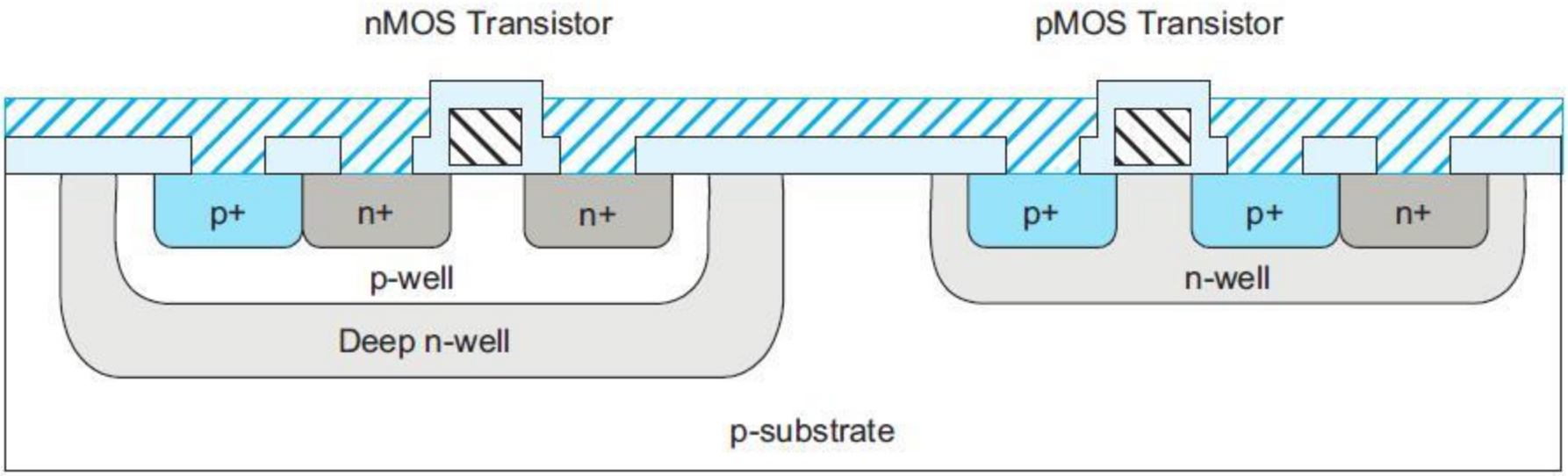
Well Formation

- n-well CMOS
- p-well CMOS
- Twin-well/dual-well CMOS
- Triple-well CMOS

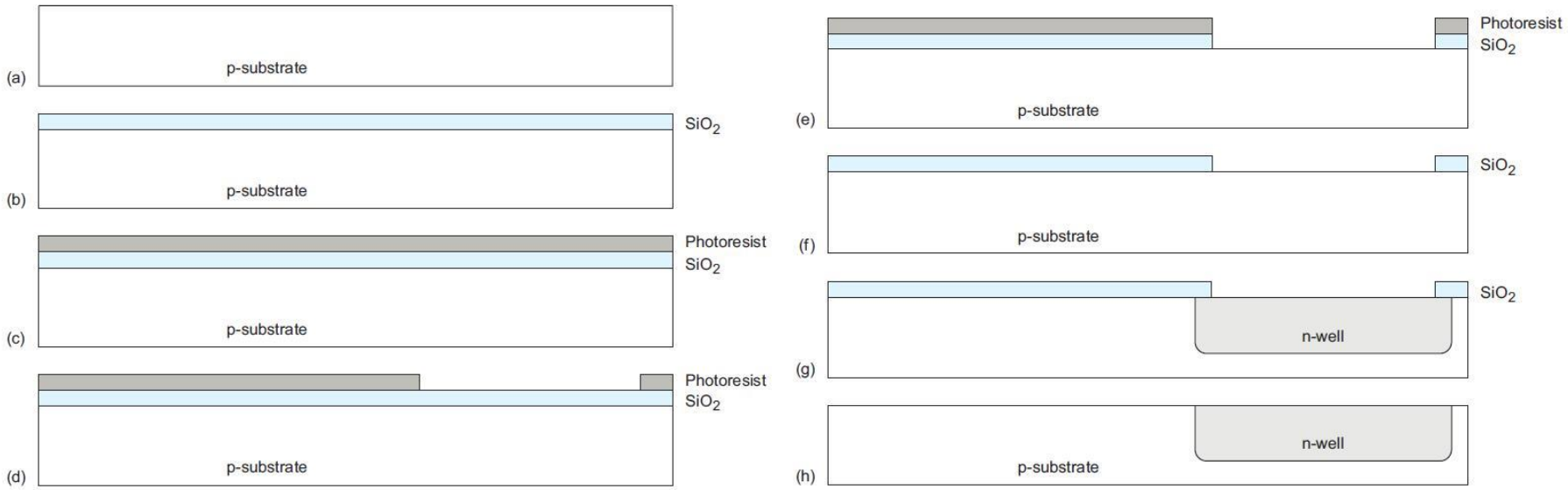
n-well CMOS


A
GND
Gate
Y
Gate
V_{DD}
p+
Substrate Tap
n+
Source
n+
Drain
p+
Drain
p+
Source
n+
Well Tap
nMOS Transistor
pMOS Transistor
n-well
p-substrate
SiO_2
n+ diffusion
p+ diffusion
polysilicon
metal1

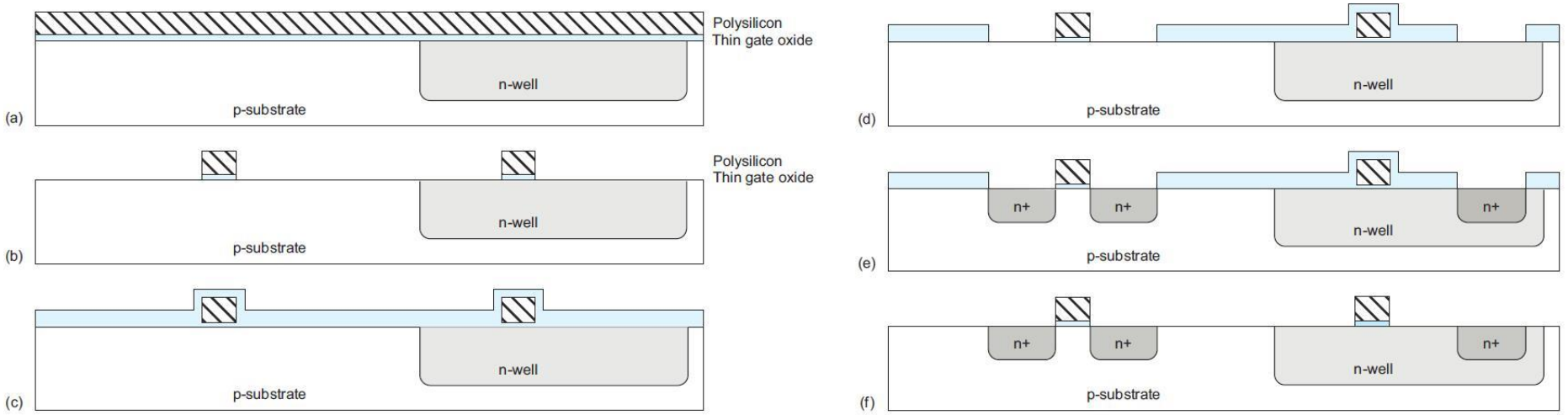
Tripe-well CMOS



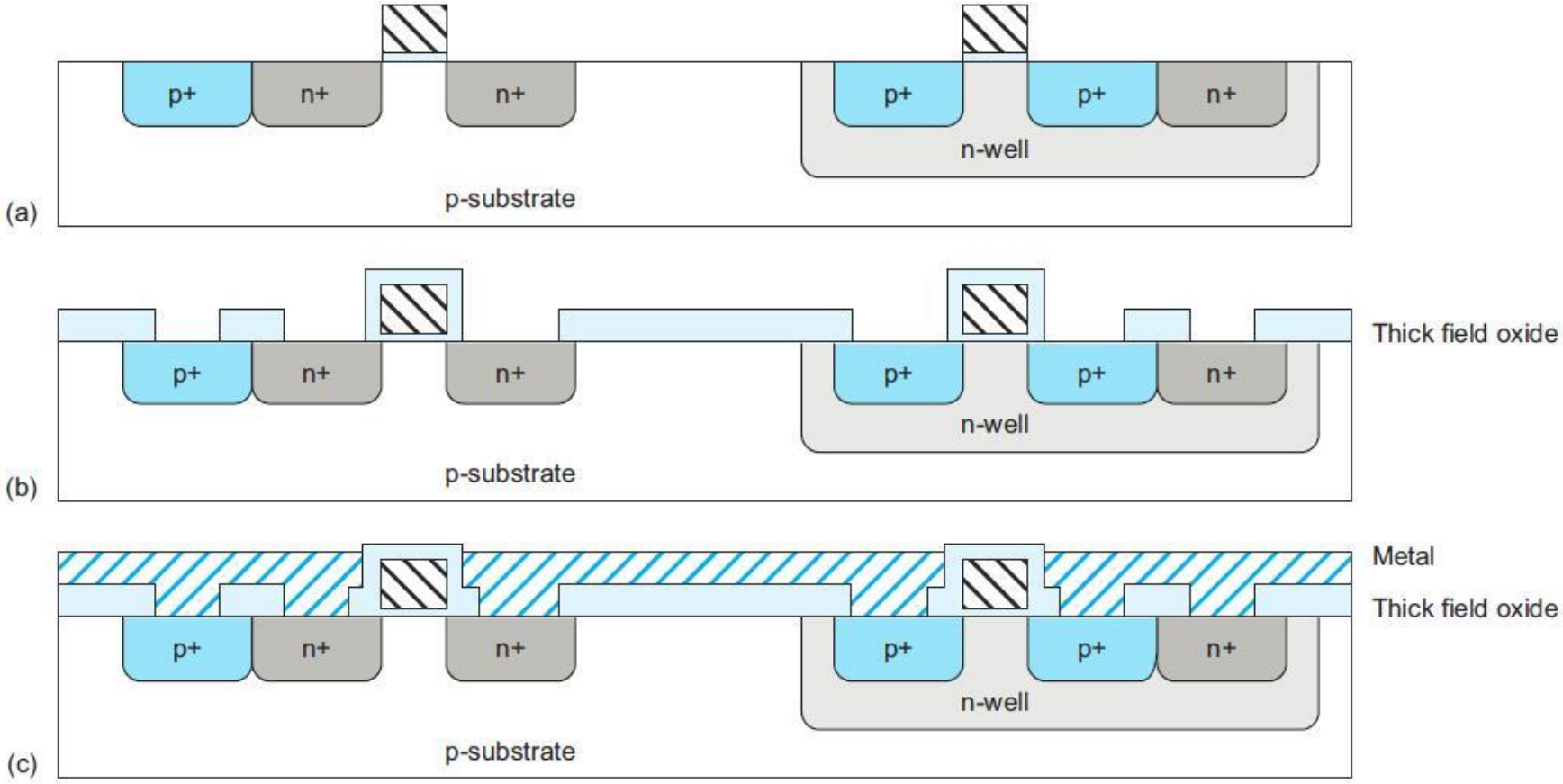
n-well CMOS Process



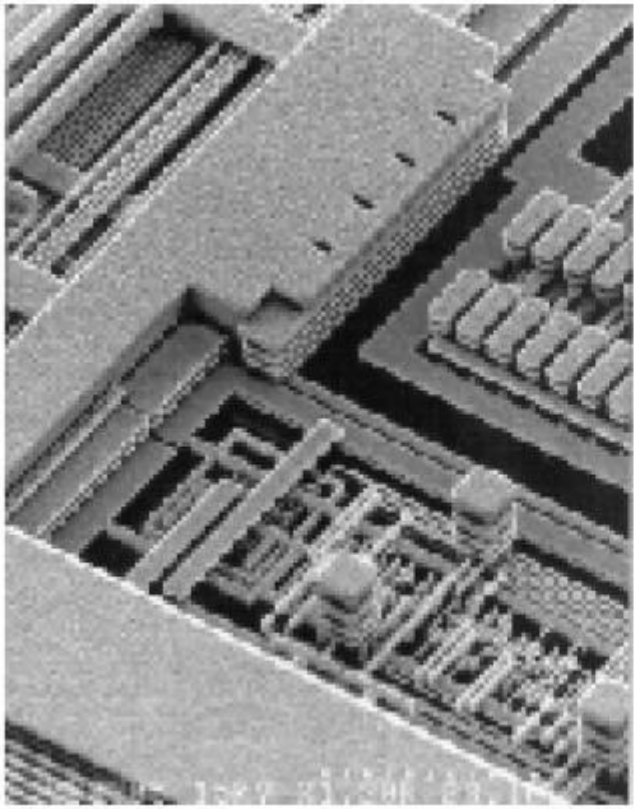
n-well CMOS Process 2

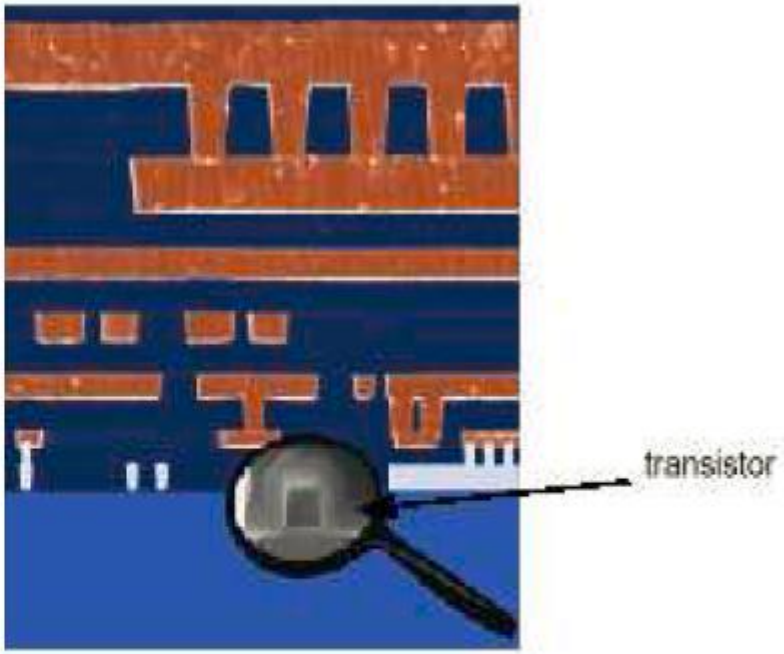


n-well CMOS Process 3



Micrographs

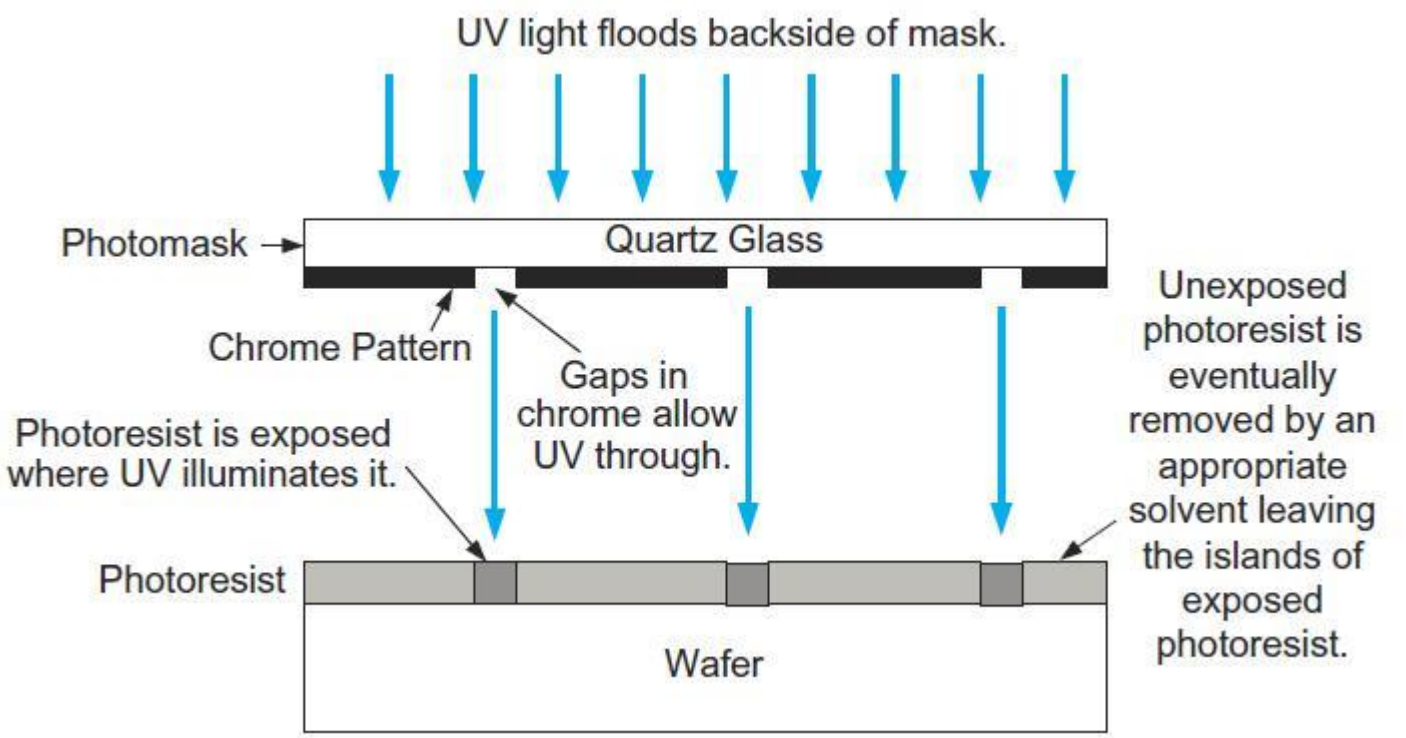




Key Proccesses

- Patterning – Lithography
- Etching
- Oxidation
- Isolation
- Implantation

Patterning-Photolithography



pitch: 2b

$$2b = k_1 \frac{\lambda}{\mathrm{NA}}$$

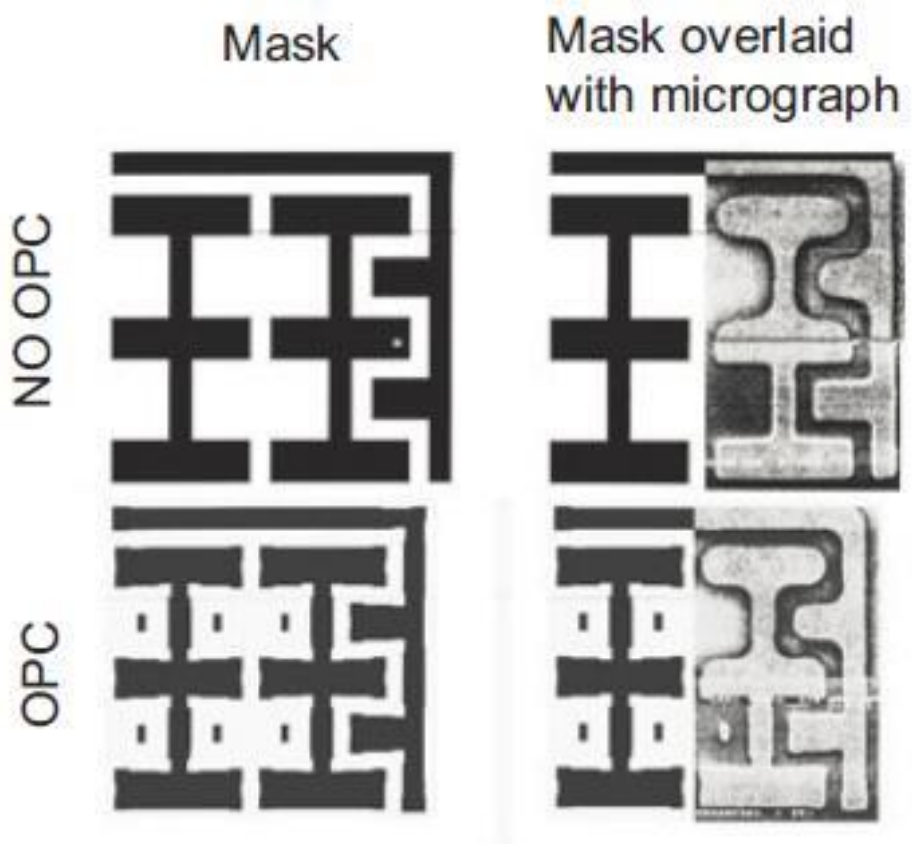
numerical aperture: NA

$$\mathrm{NA} = n \sin\alpha$$

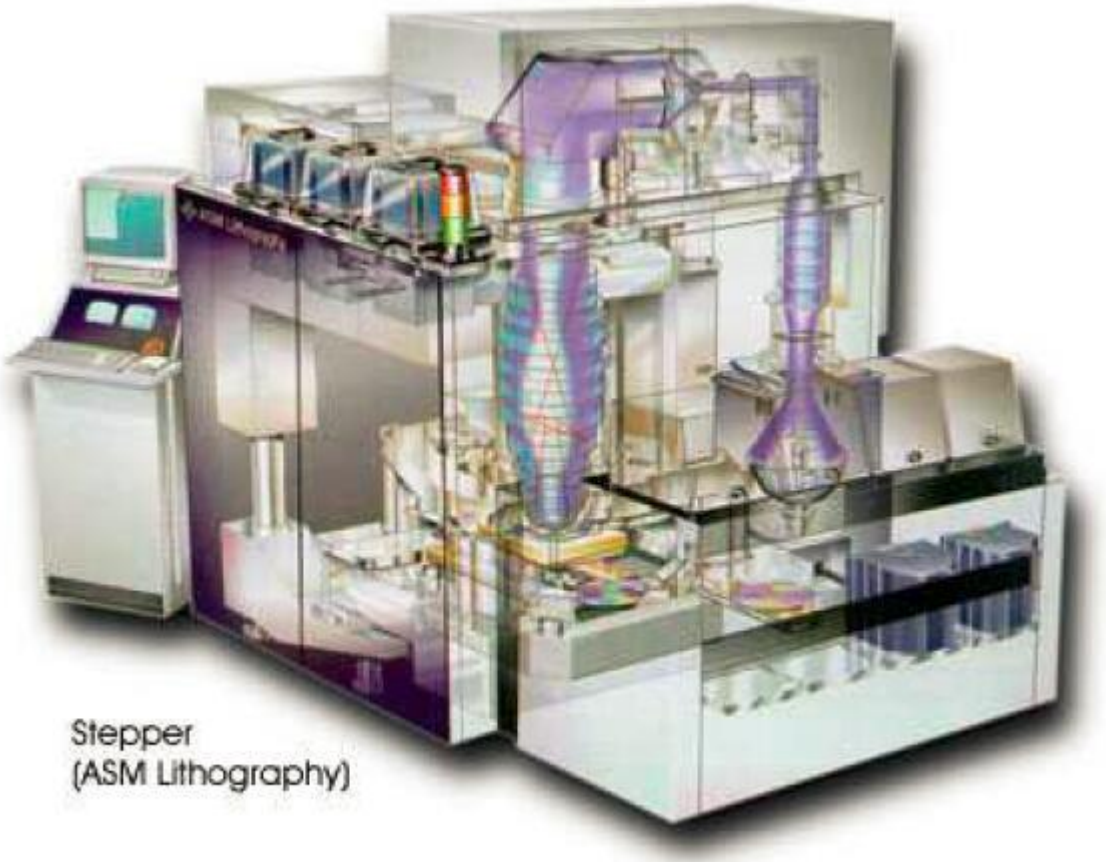
refractive index: n

Currently: 193 nm UV immersion lithography
13.5 nm EUV for 7nm and 5nm technology

Optical Proximity Correction (OPC)



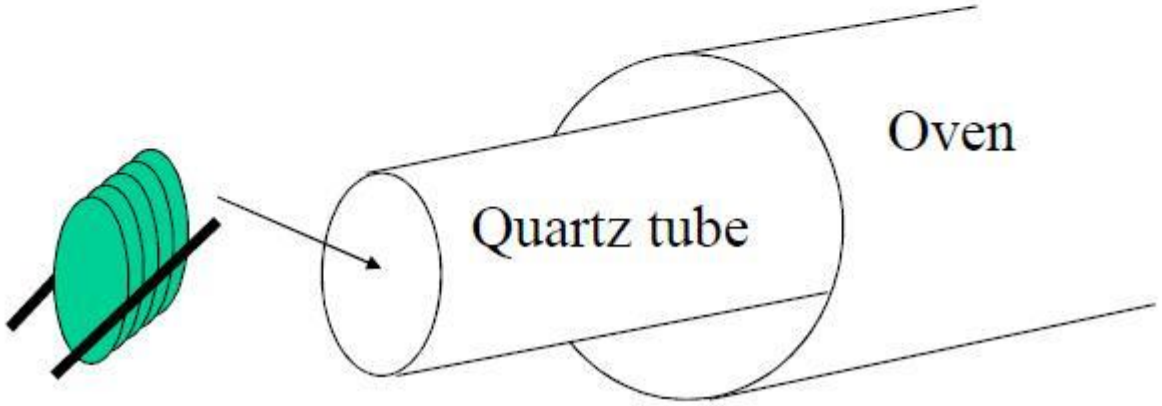
The Real Thing



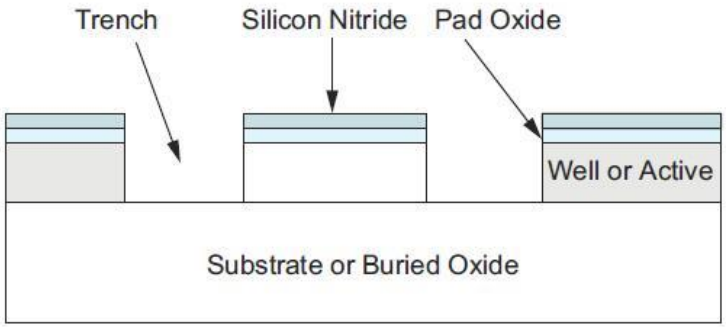
SiO_2 - Oxidation

1) Heat wafers in oxygen to 1000 °C for 15 min
O_2 diffuses through oxide layer and forms new oxide at Si surface $Si + O_2 \rightarrow SiO_2$

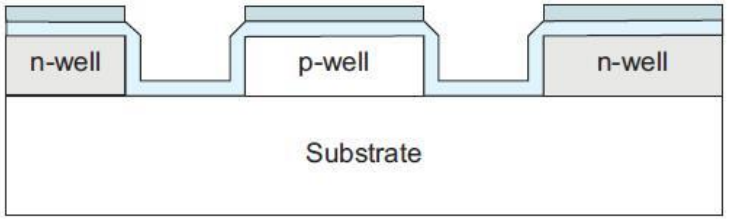
2) Heat wafers in a low pressure gas mixture SiH_4 and O_2 at 800°C. $SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$ (*water vapor*)
(Similar for polysilicon: $SiH_4 \rightarrow Si + 2H_2$ at 650°C)



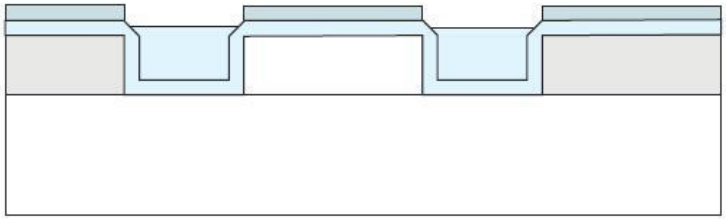
Isolation – Shallow Trench Isolation (STI)



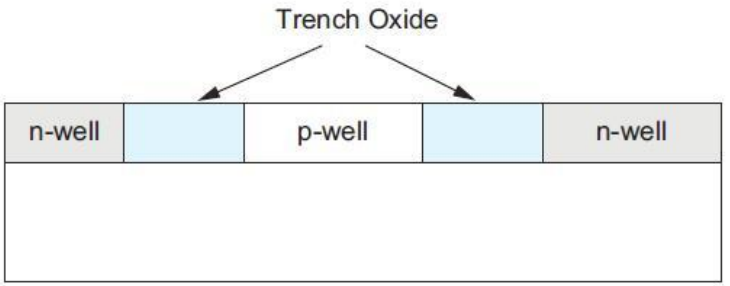
(a) Trench Etch



(b) Liner Oxidation

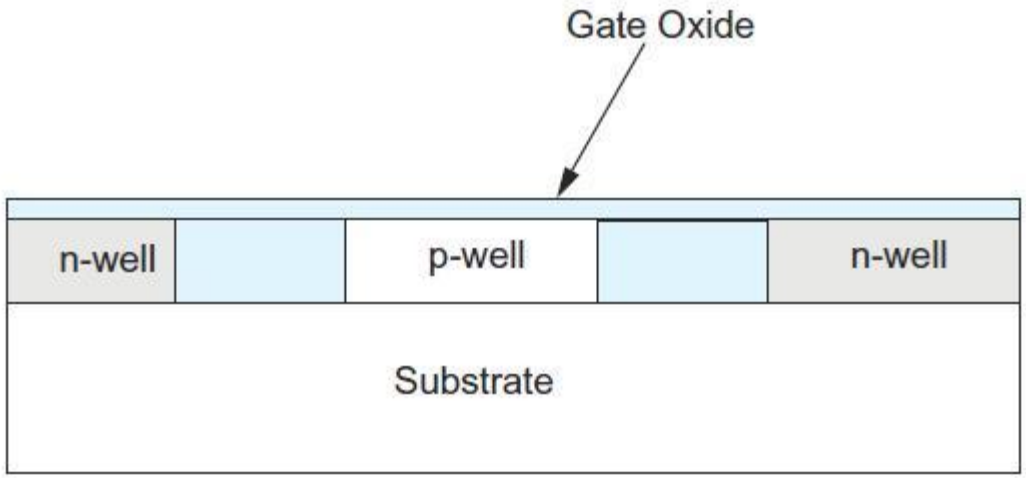


(c) Fill Trench with Dielectric



(d) CMP for Planarization

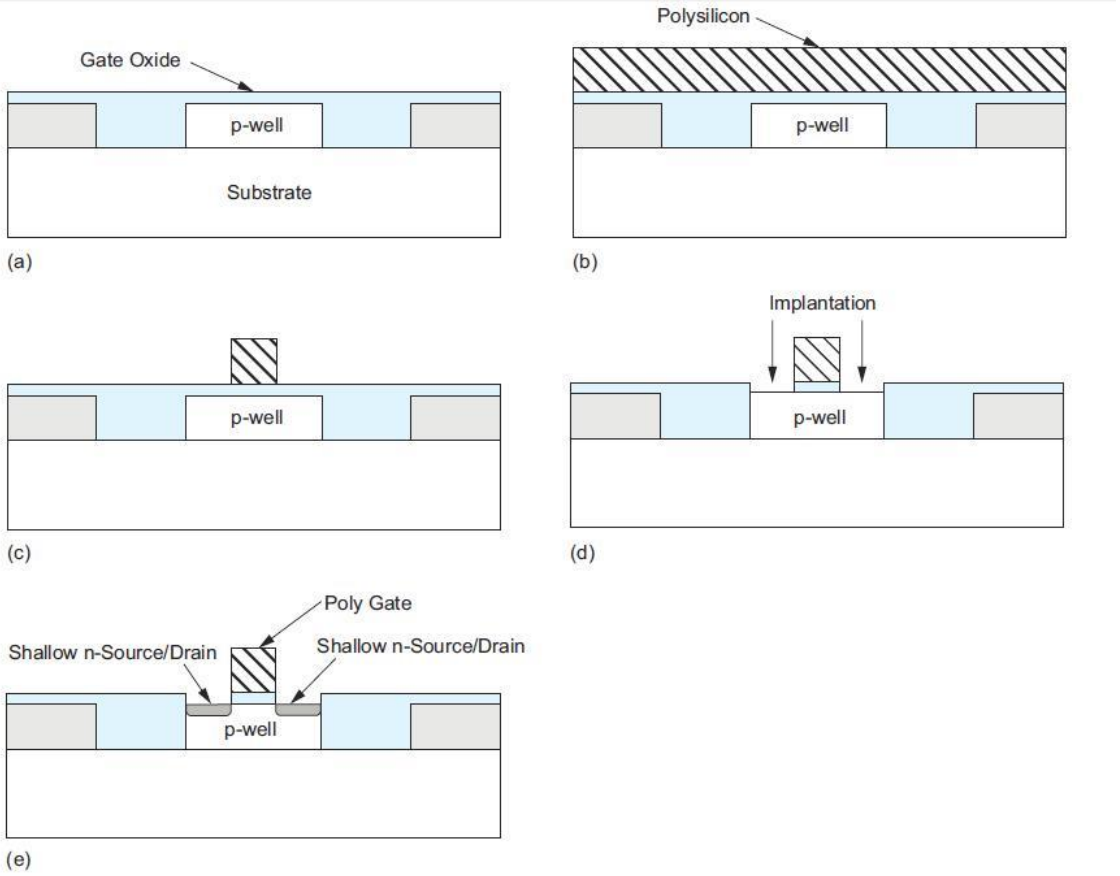
Gate Oxide



Gate stack:
$SiO_2/SiON$

EOT (effective oxide thickness) is ~10.5-15 for 65 nm process

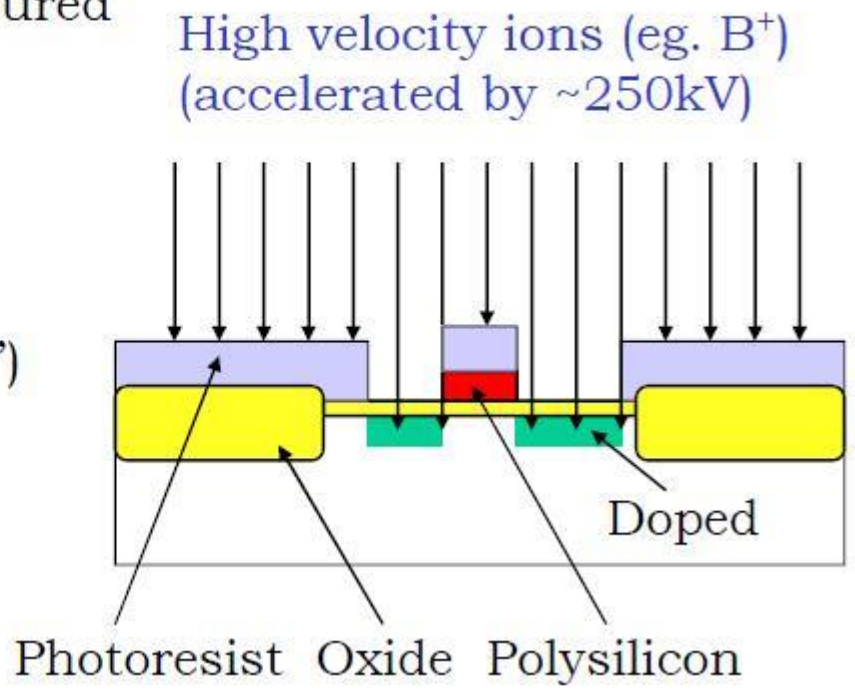
Gate, Source and Drain Formation



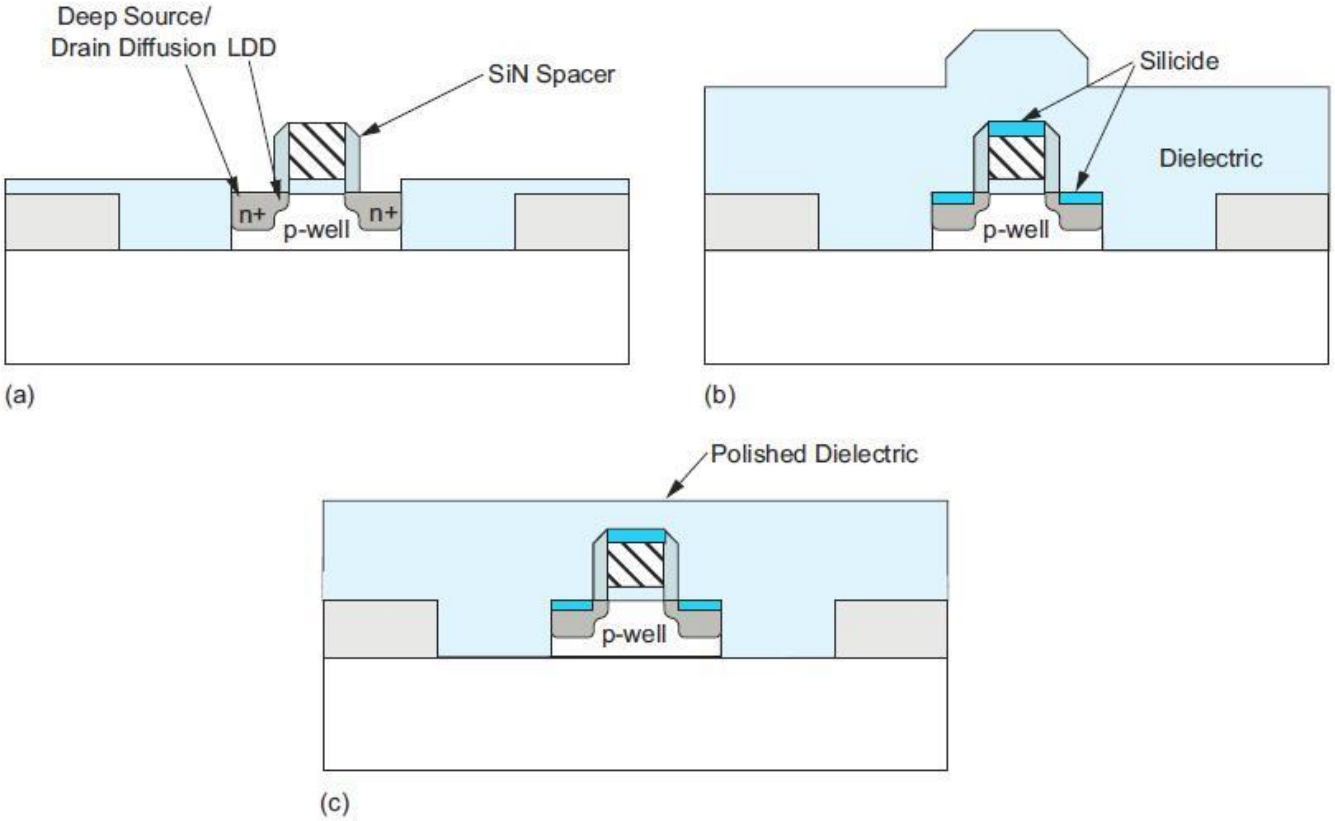
Doping by Ion Implantation

An ion beam hits the wafer (in vacuum, current measured gives the dose)

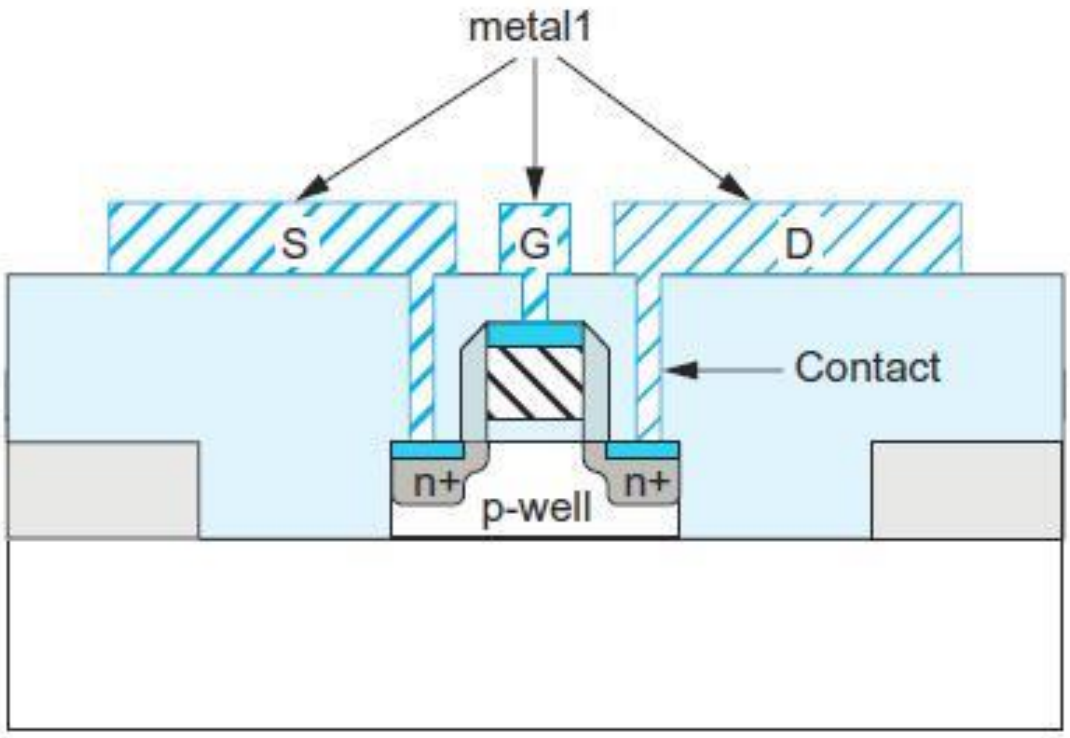
Wafer heated (after resist removal) to activate implanted atoms (place them in "silicon positions") and diffuse them further into material.



Lightly Doped Drain (LDD) and Deep Diffusion



Metallization and Contacts

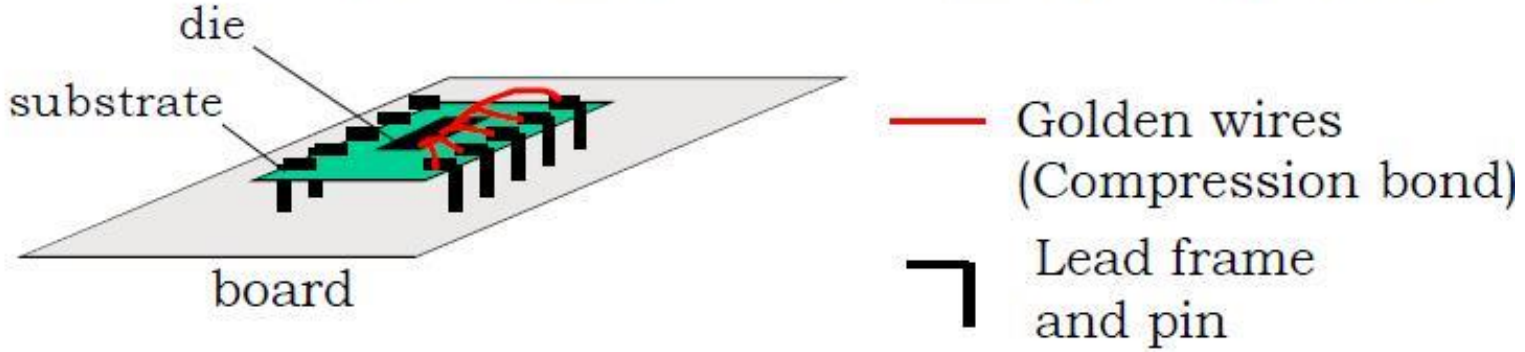


Packaging – Die to Chip

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

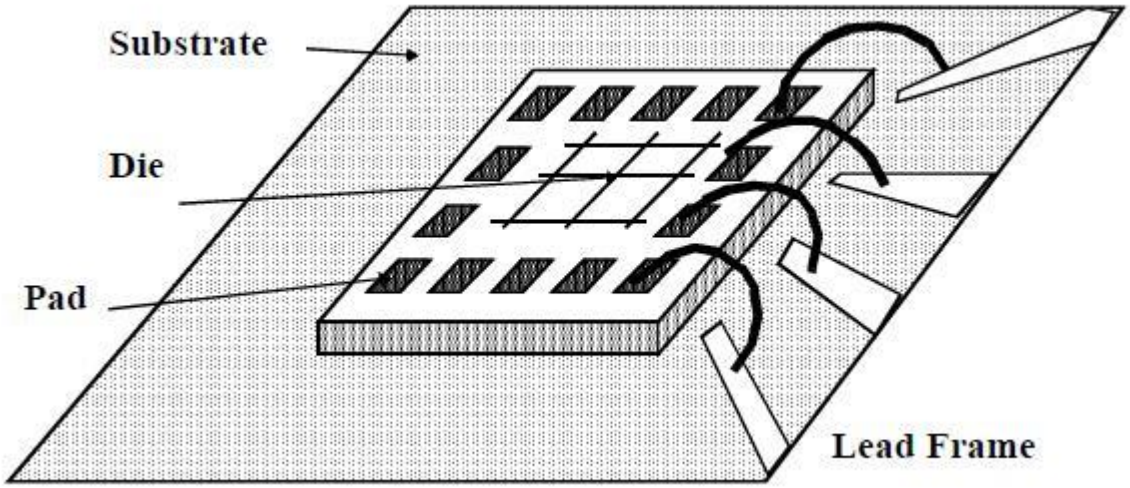
Packaging Techniques

Traditional: Plastic DIL (Dual in line), **bonding wires**
Through-hole or surface mounted on board

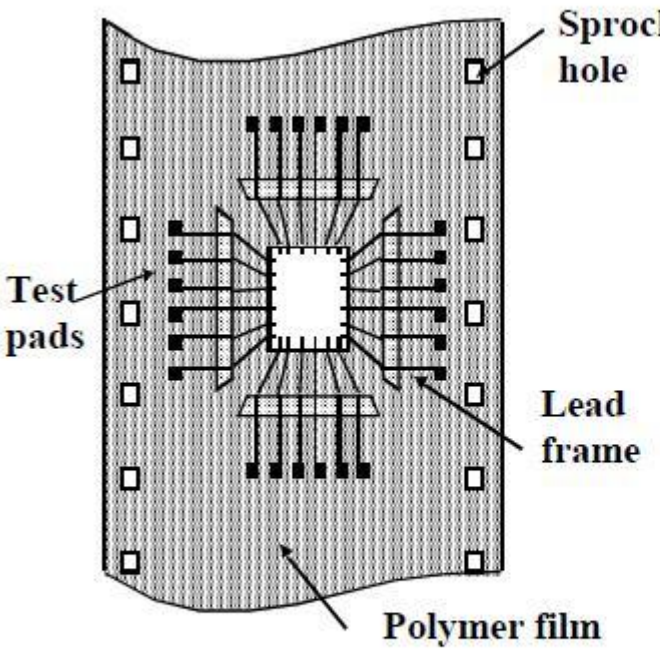


New: PLCC, PGA , … (with a number of pins)
Tape Automated Bonding,
Flip-chip bonding,
Ball grid array mounted on board

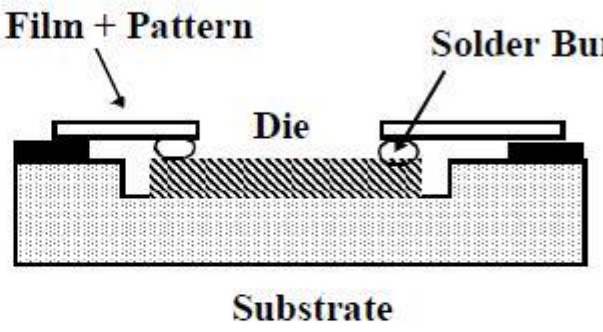
Wire Bonding



Tape Automated Bonding

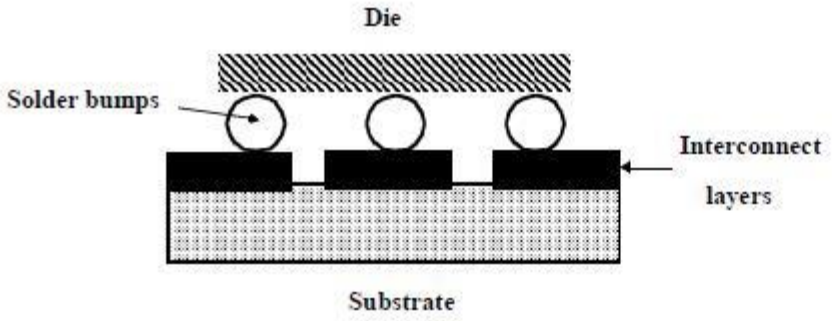


(a) Polymer Tape with imprinted wiring pattern.



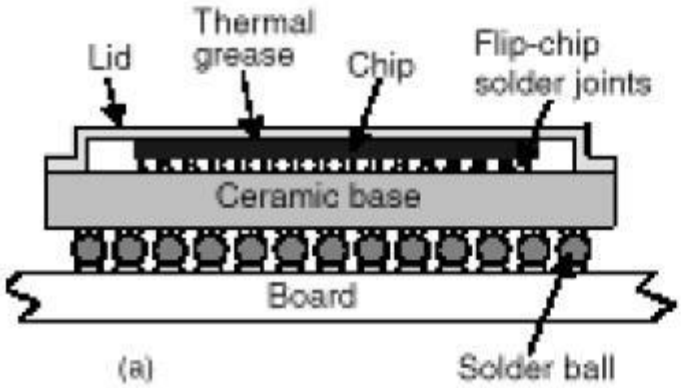
(b) Die attachment using solder bumps.

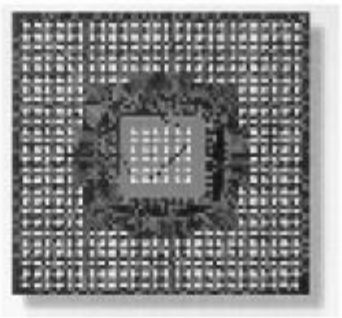
Flip-Chip Bonding and BGA



Flip-chip

BGA (Ball grid array), wire or solder ball bonds



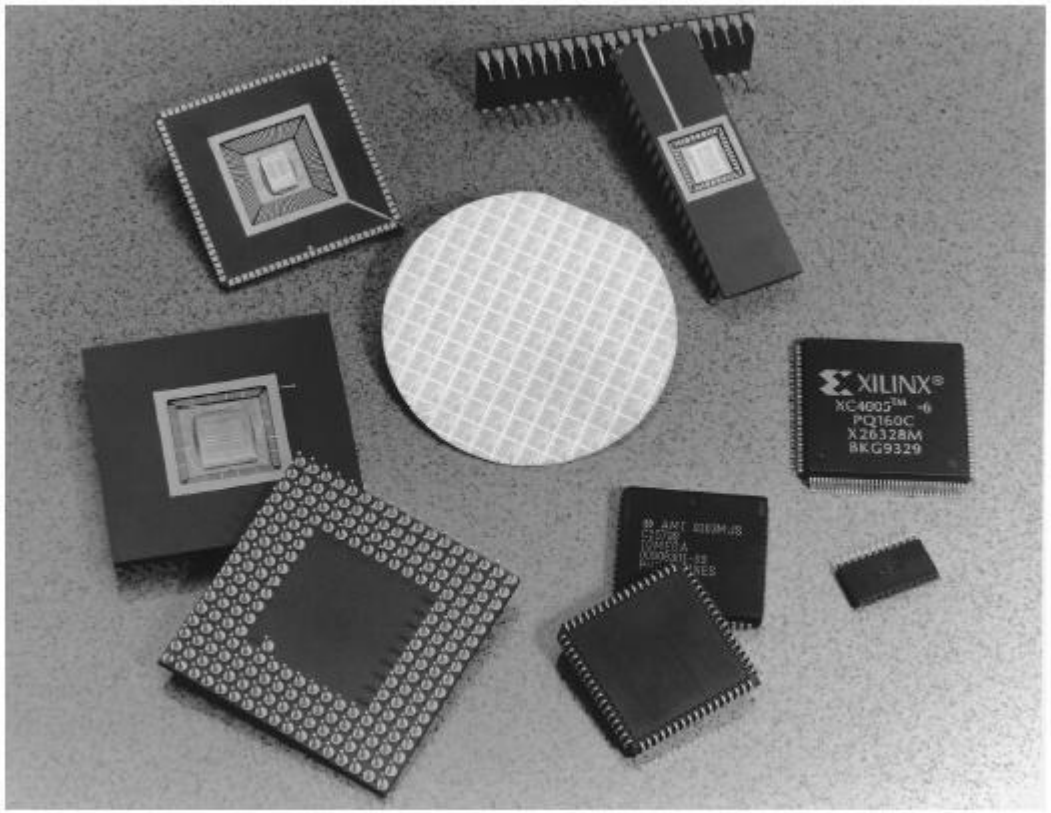


(b)

Ceramic or Polymer base

Solder ball bonded to chip and board

Package Types



Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

per 1 pin

per 1 mm

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Heat Dissipation

$$T_{chip} - T_{amb} = \Theta \cdot P$$

Power dissipated

Thermal resistance

Depends on case material and
air convection (natural or forced)

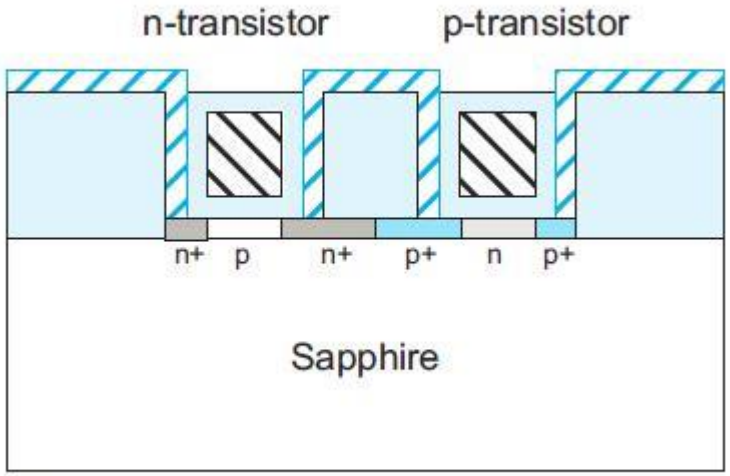
for DIL $\Theta = 25\ ^0C/W - 38\ ^0C/W$
for PGA $\Theta = 15\ ^0C/W - 30\ ^0C/W$

The chip must not be too hot !
usually $T_{chip} < 100\ ^0C$

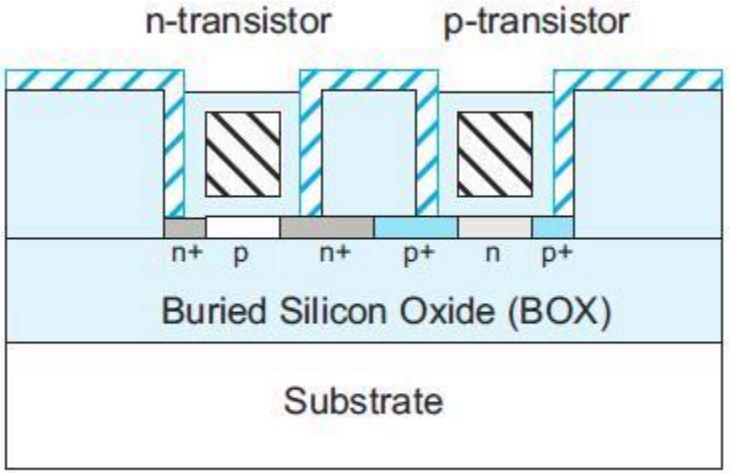
CMOS Process Enhancements

- Silicon on Insulator (SOI)
- High-k dielectrics
- Strained Silicon
- FinFETs

Silicon on Insulator (SOI)



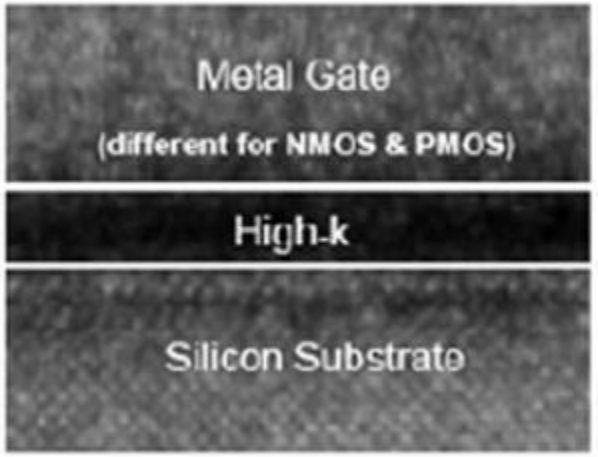
(a)



(b)

Advantages:
elimination of the capacitance between the S/D and body for high-speed circuits
low subthreshod leakage
Disadvantage:
threshold variation caused by floating body

High-k Gate Dielectrics

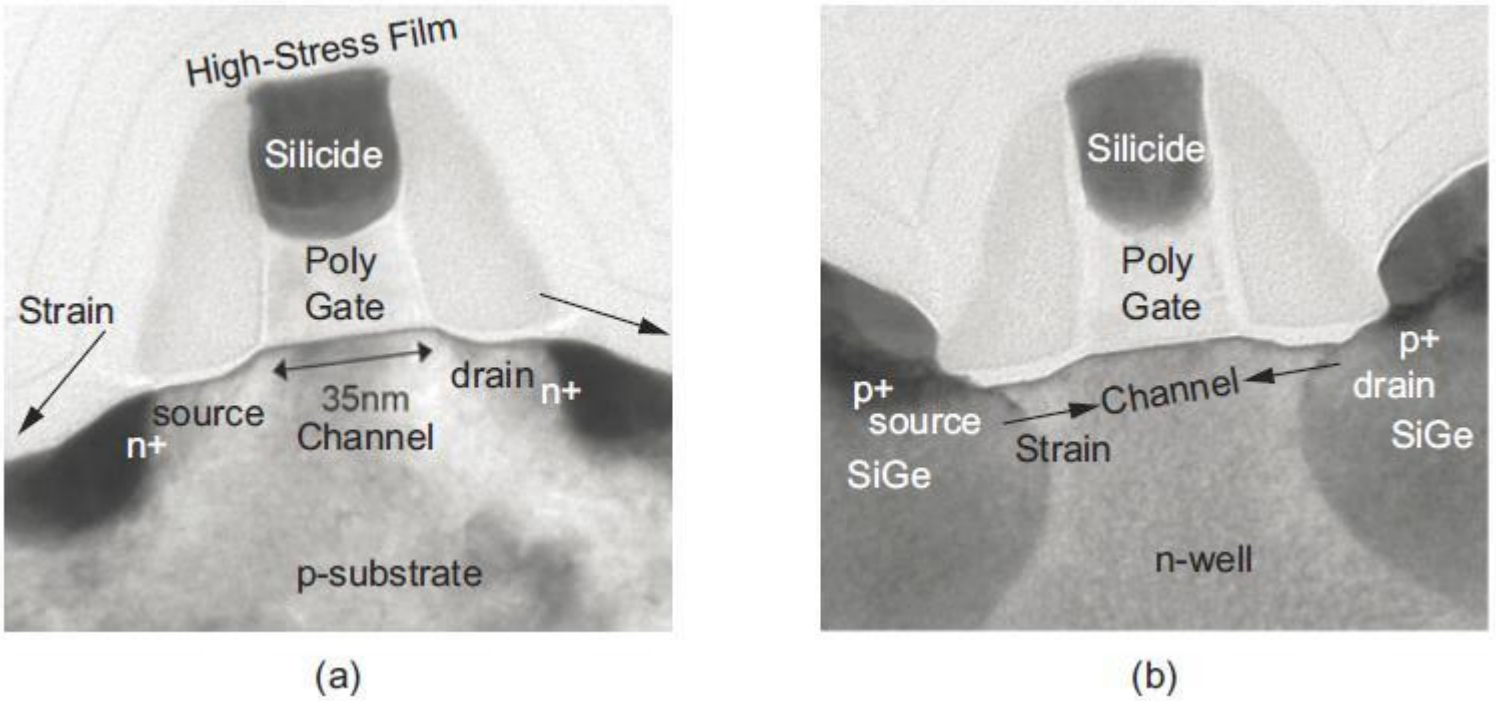


- SiON k=4.1-4.2 for 130 nm process

- Hafnium oxide (HfO_2) k = 20 for 45 nm process

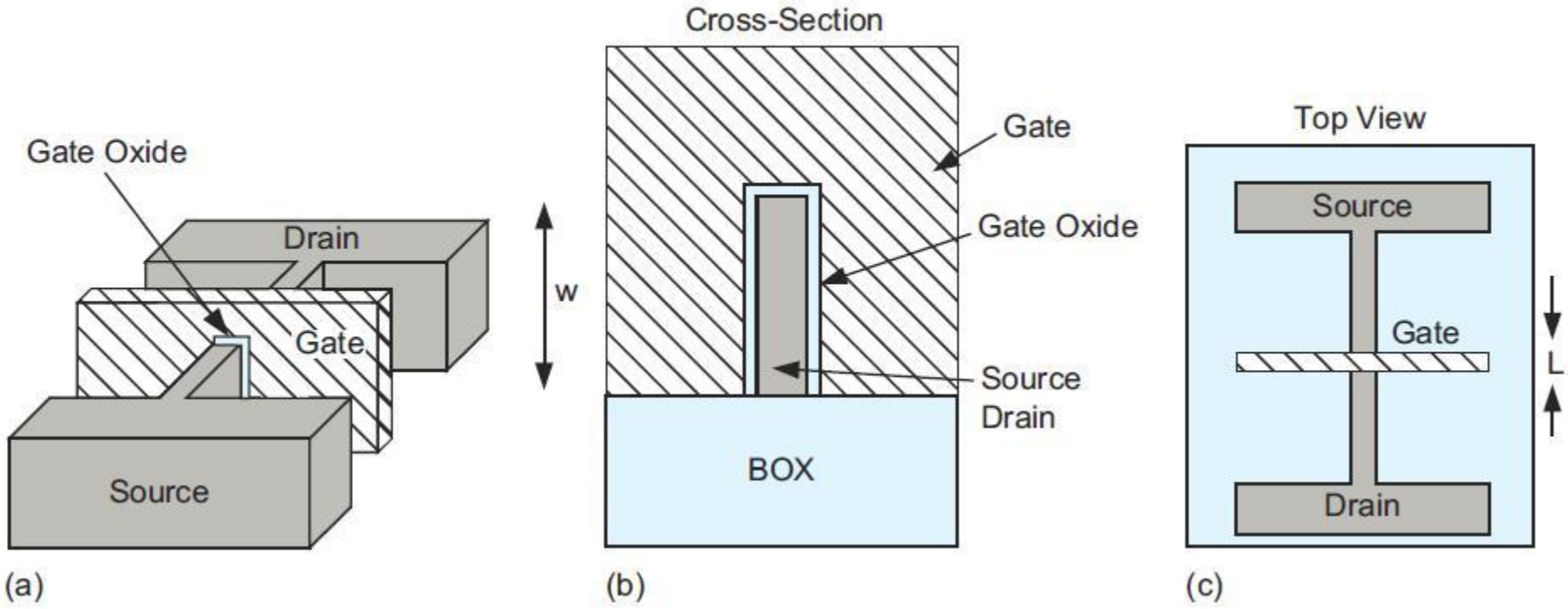
thicker dielectrics and less leakage

High Mobility – Strained Silicon



strained nMOS and pMOS transistors 40% and 100% higher mobility than unstrained transistors (Intel 65 nm process)

FinFETs


Gate Oxide
Drain
Gate
Source
(a)
w
Cross-Section
Gate
Gate Oxide
Source
Drain
BOX
(b)
Top View
Source
Gate
Drain
L
(c)

Summary

- Fabrication process is complex and expensive
- Understanding the process helps us to design chips with the performance expected from simulation
- Analog and mixed-signal designs need special care
- New techniques enhance performance of high-speed circuits

Reference

- *Digital Integrated Circuits*, by Jan M. Rabaey, et al.
- *CMOS VLSI Design*, by David Harris, et al.

www.liu.se

LINKÖPING UNIVERSITY