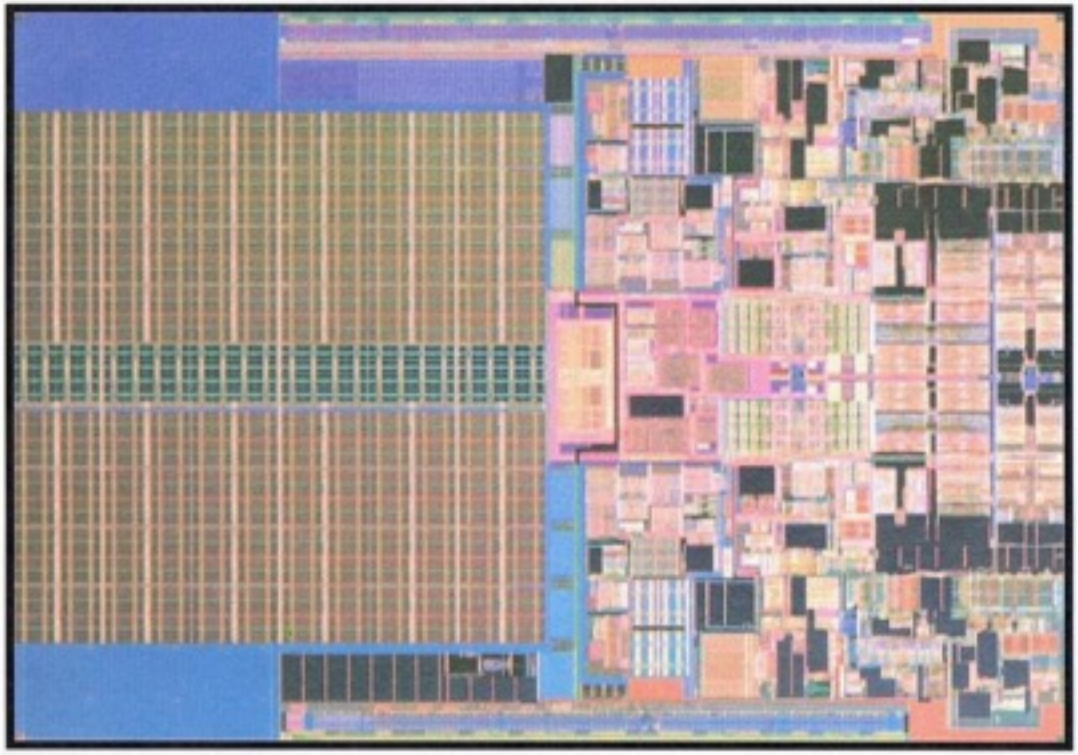
Digital ICs — Lectures

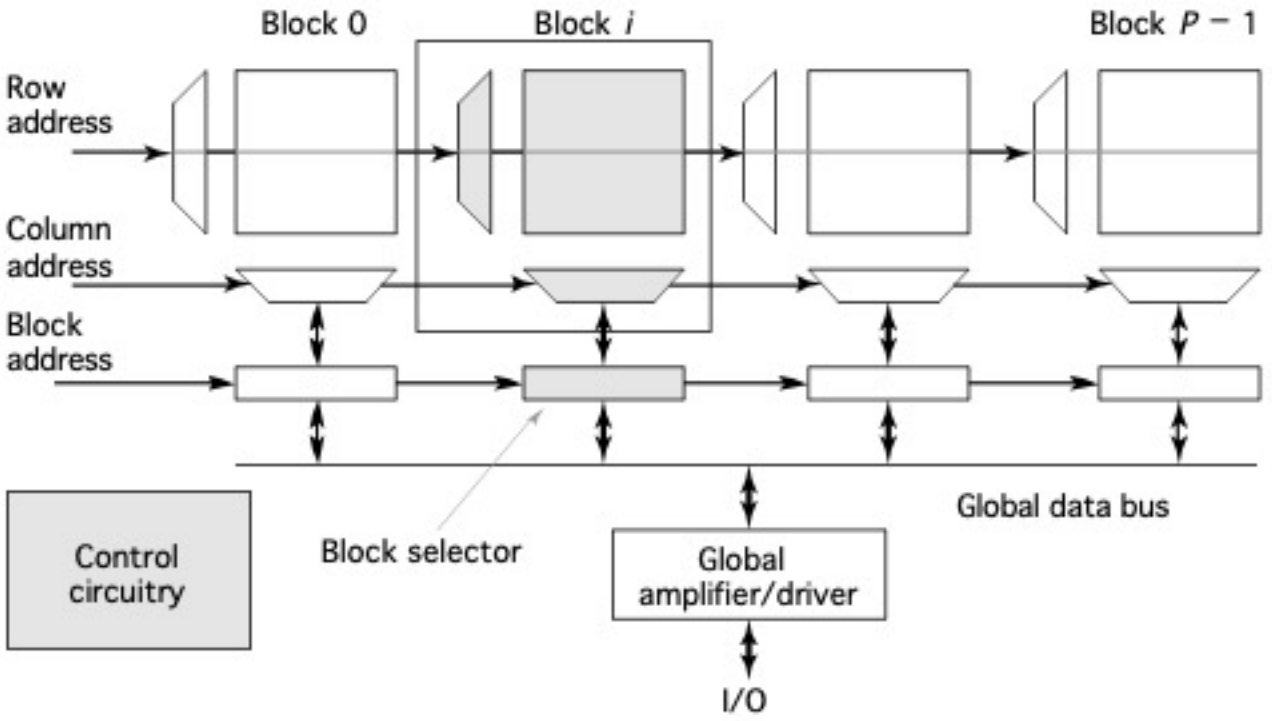
1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
4) **Circuits** [Ch. 5]	*TSEI03/TSTE86*
5) **Combinational logic** [Ch. 6]	*TSEI03/TSTE86*
6) **Sequential circuits** [Ch. 7]	*TSEI03/TSTE86*
7) **Synchronization** [Ch. 10]	*TSTE86*
8) **Adders** [Ch. 11]	*TSEI03/TSTE86*
9) **Multipliers** [Ch. 11]	*TSTE86*
10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
11) **Manufacturing** [Ch. 2]	*TSTE86*
12) **System design** [Ch. 8]	*TSTE86*

Cache Memory



Intel 45 nm Core 2

Hierarchical Memory Architecture



Advantages:

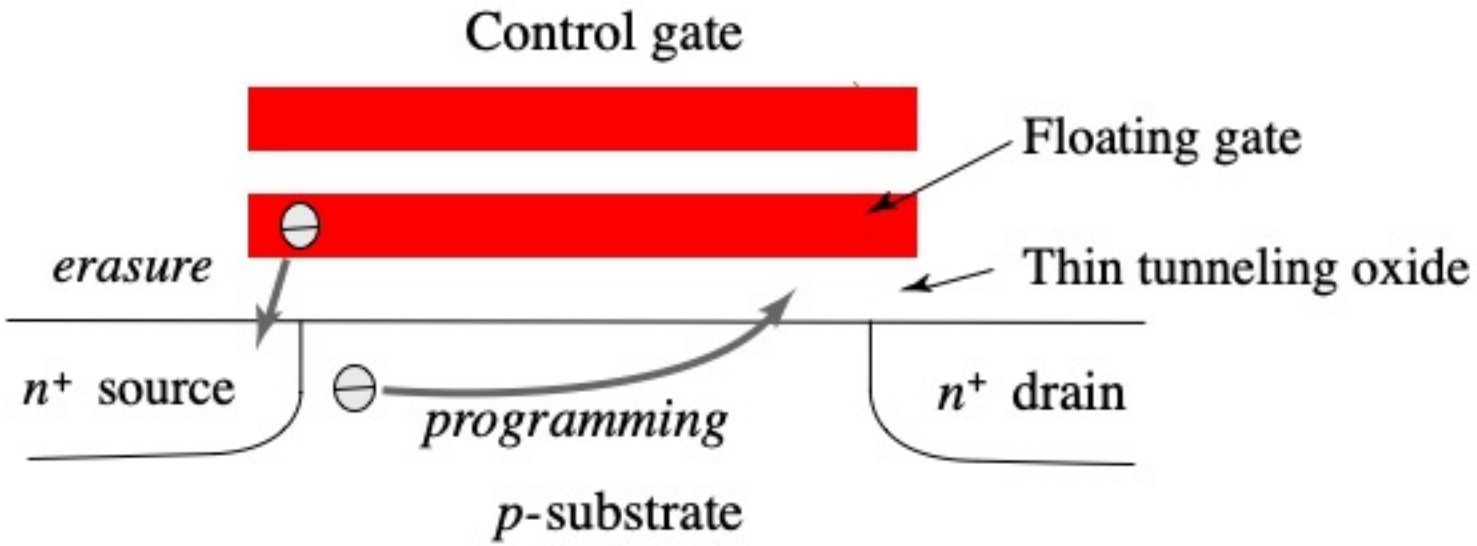
1. Shorter wires within blocks
2. Block address activates only 1 block ⇒ power savings

Example: ROM Content

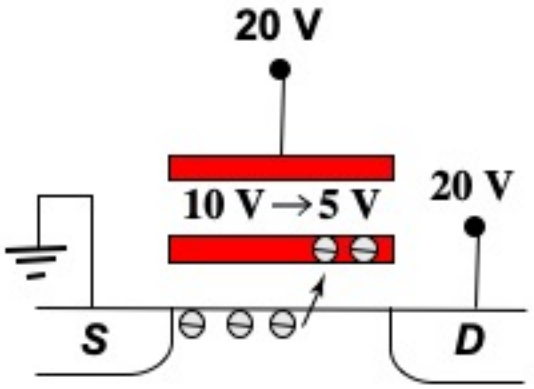
Row adress	Column adress	ROM content
00	00	0
00	01	1
00	10	0
00	11	1
01	00	0
01	01	0
01	10	1
01	11	1

Row adress	Column adress	ROM content
10	00	1
10	01	0
10	10	0
10	11	1
11	00	0
11	01	1
11	10	1
11	11	0

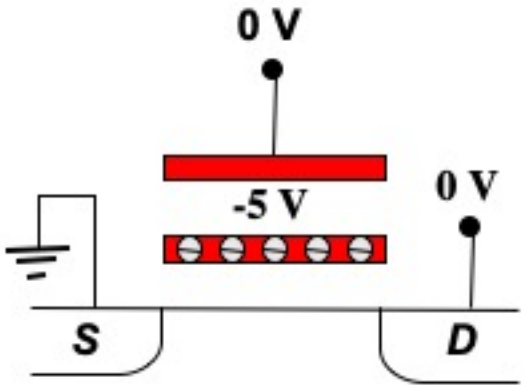
Floating Gate Transistor



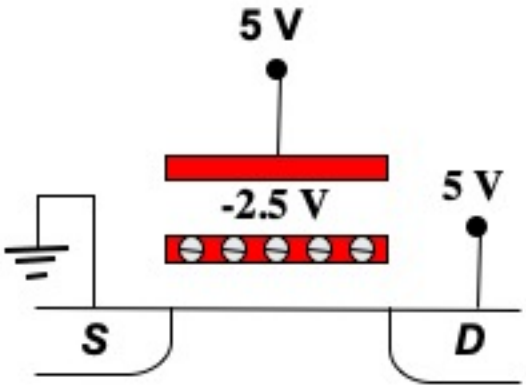
Programming V_T



Avalanche injection

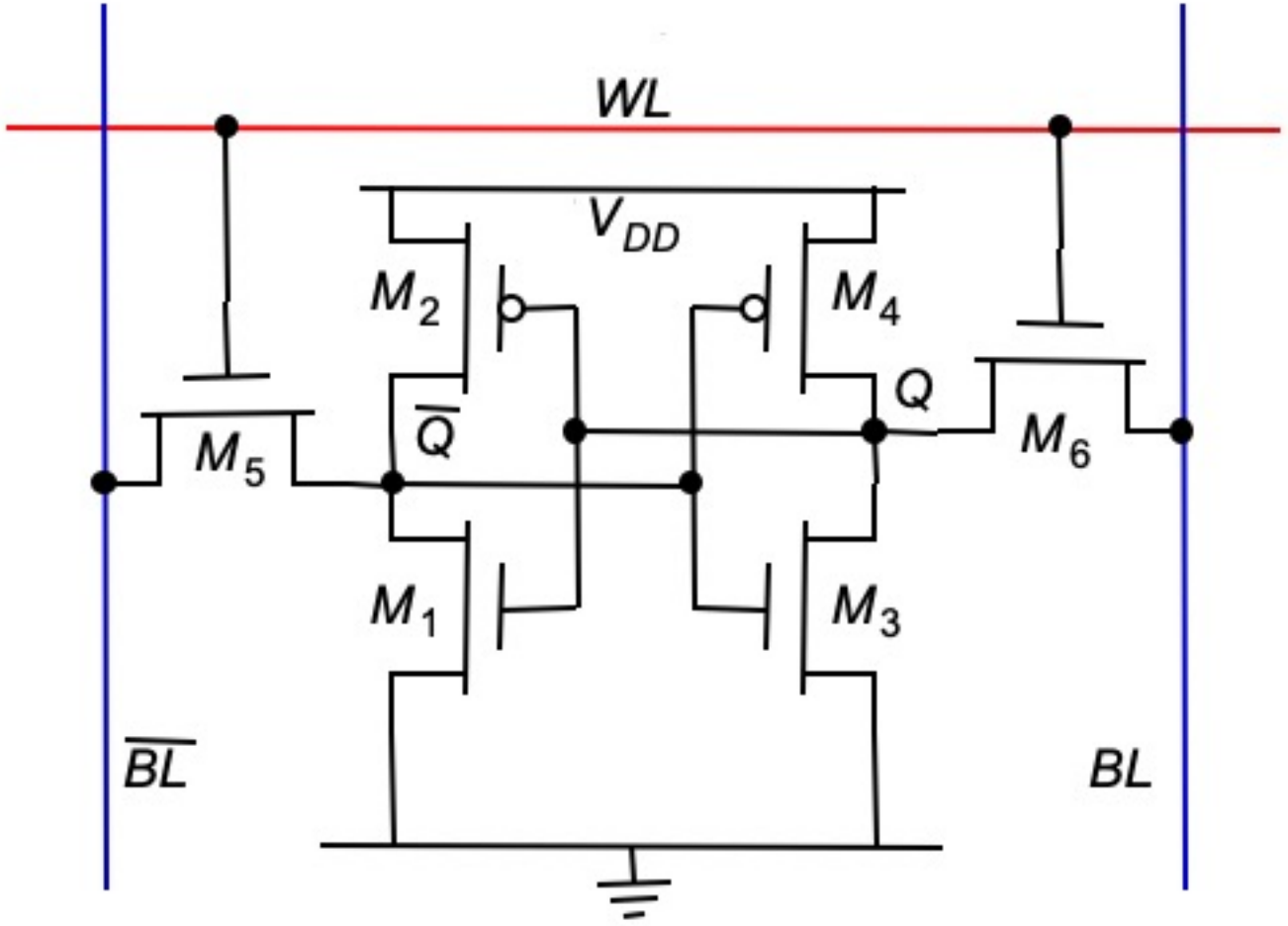


Removing programming voltage leaves charge trapped

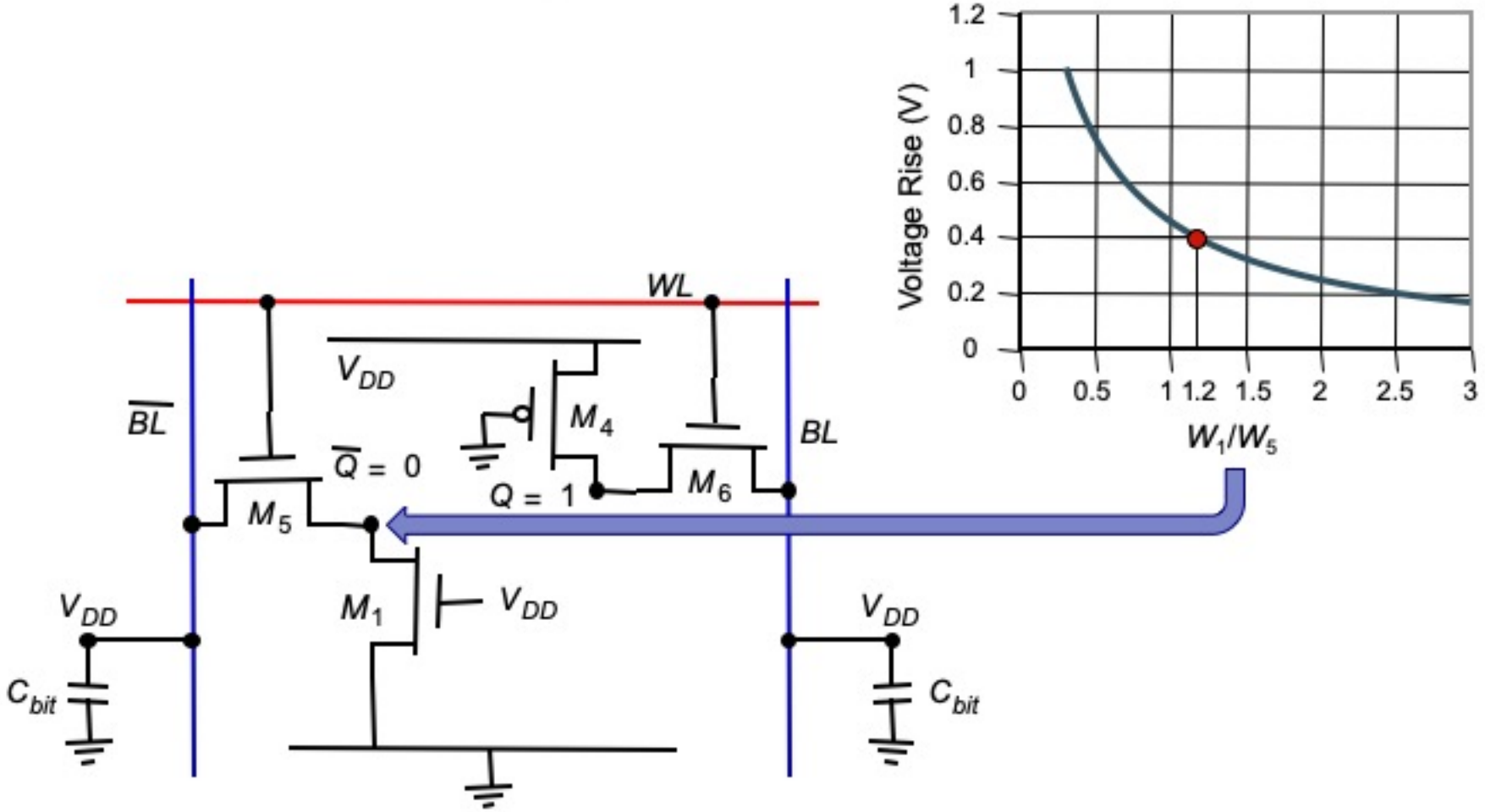


Programming results in higher V_T

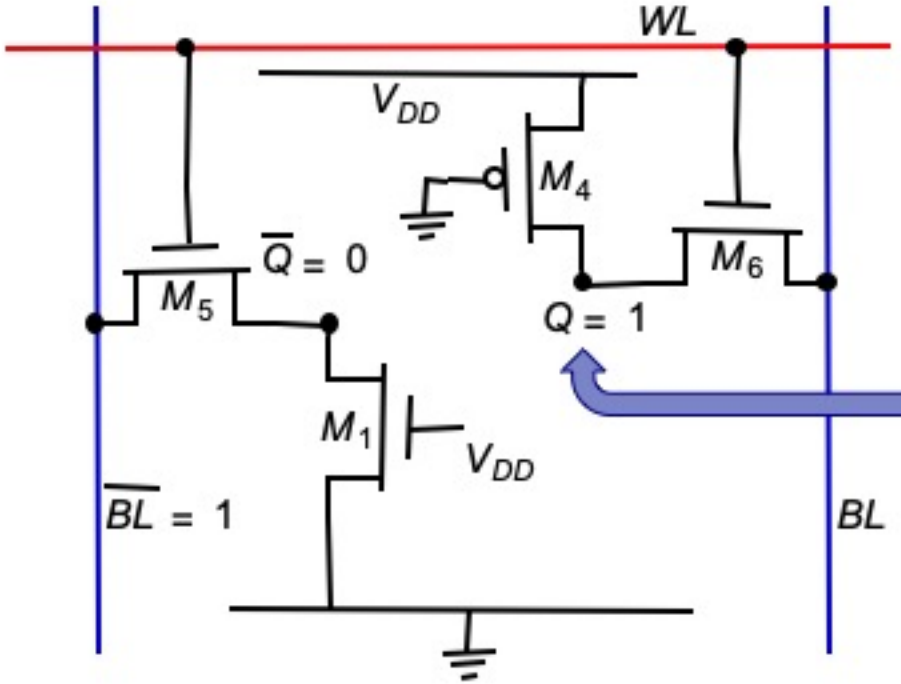
6T SRAM Cell

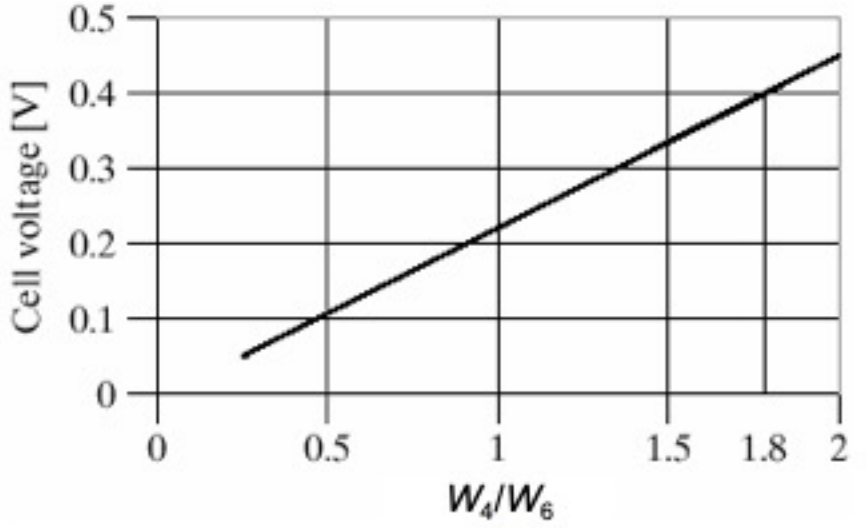


SRAM Read Operation

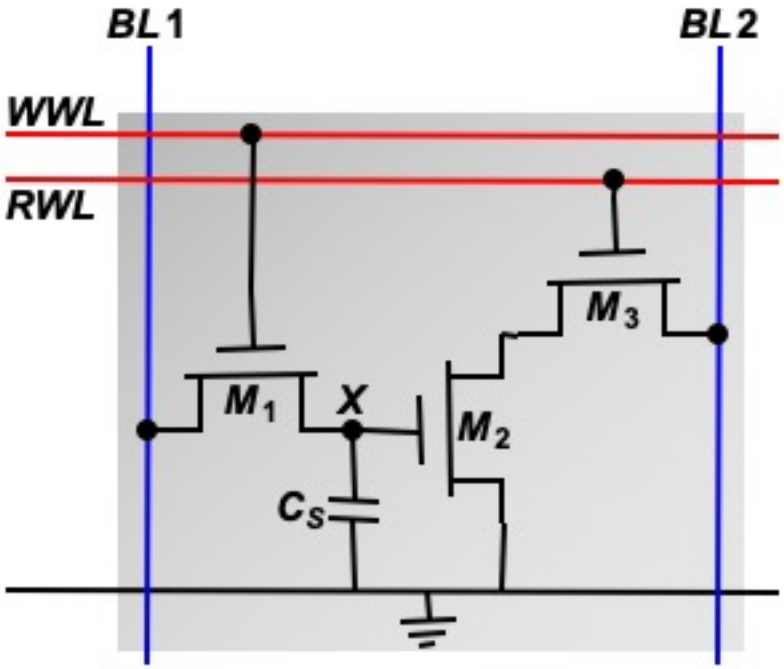


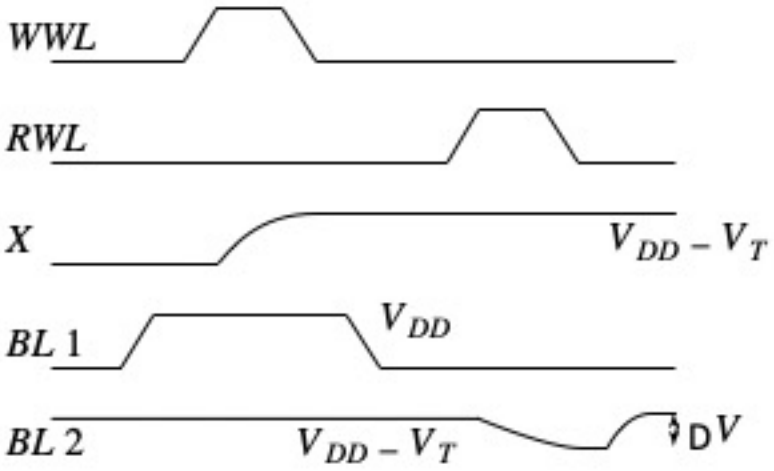
SRAM Write Operation





3T DRAM Cell



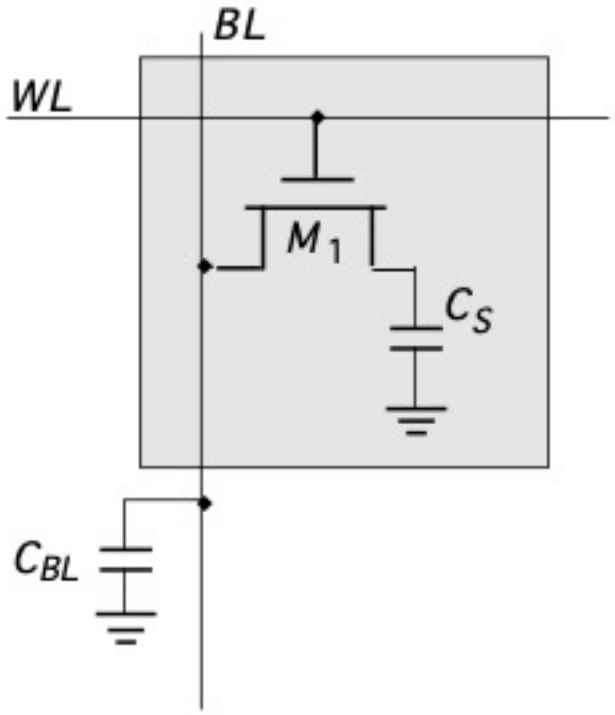


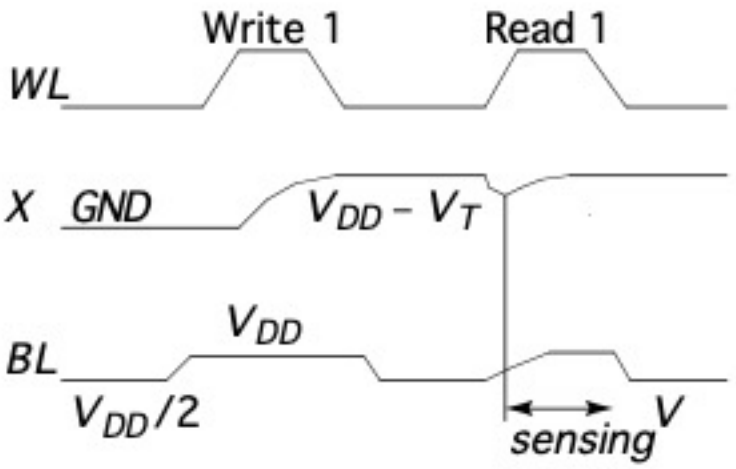
No constraints on device ratios

Reads are non-destructive

Value stored at node *X* when writing a "1" = $V_{WWL} - V_{Tn}$

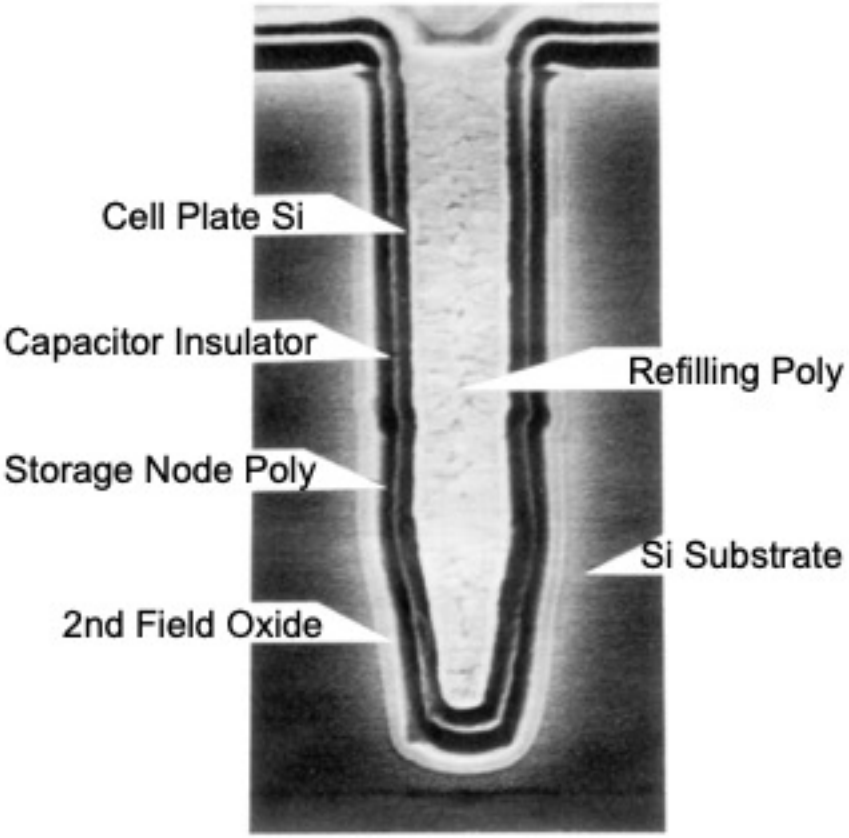
1T DRAM Cell



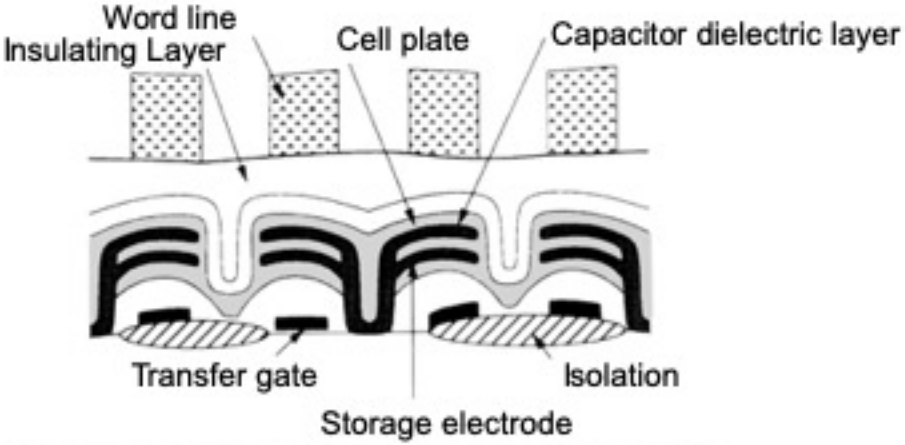


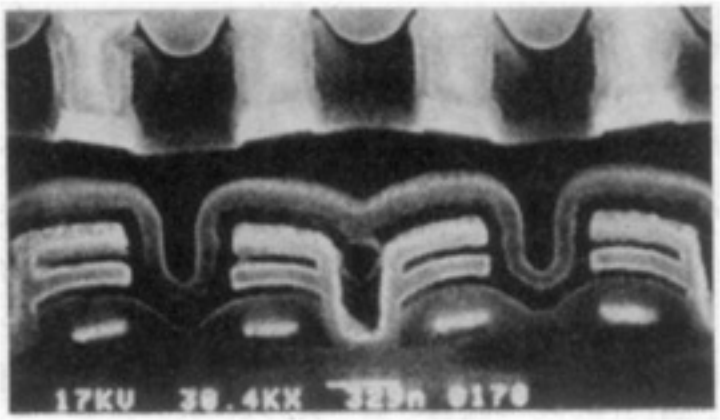
Voltage swing is small; typically < 200 mV

Implementation of DRAM Cells



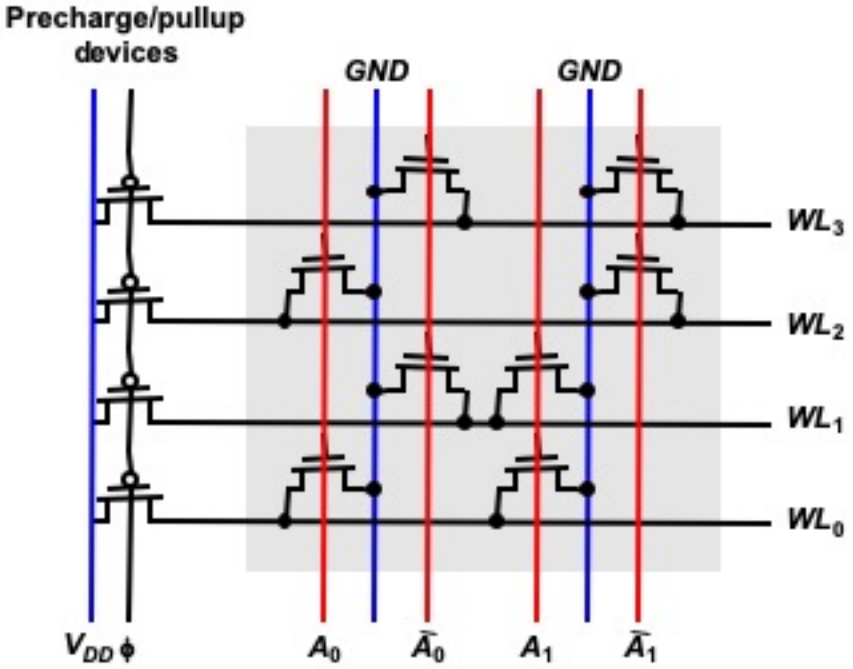
Trench cell



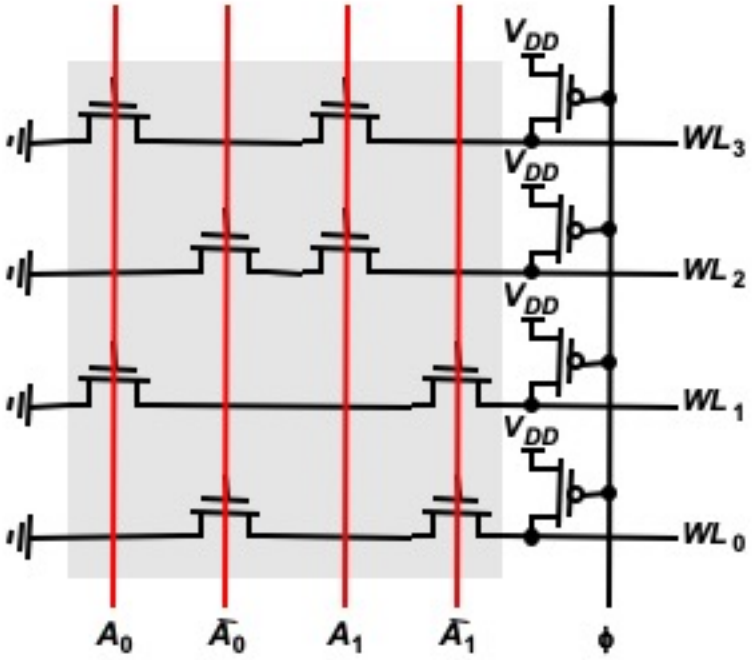


Stacked-capacitor cell

Row Decoders

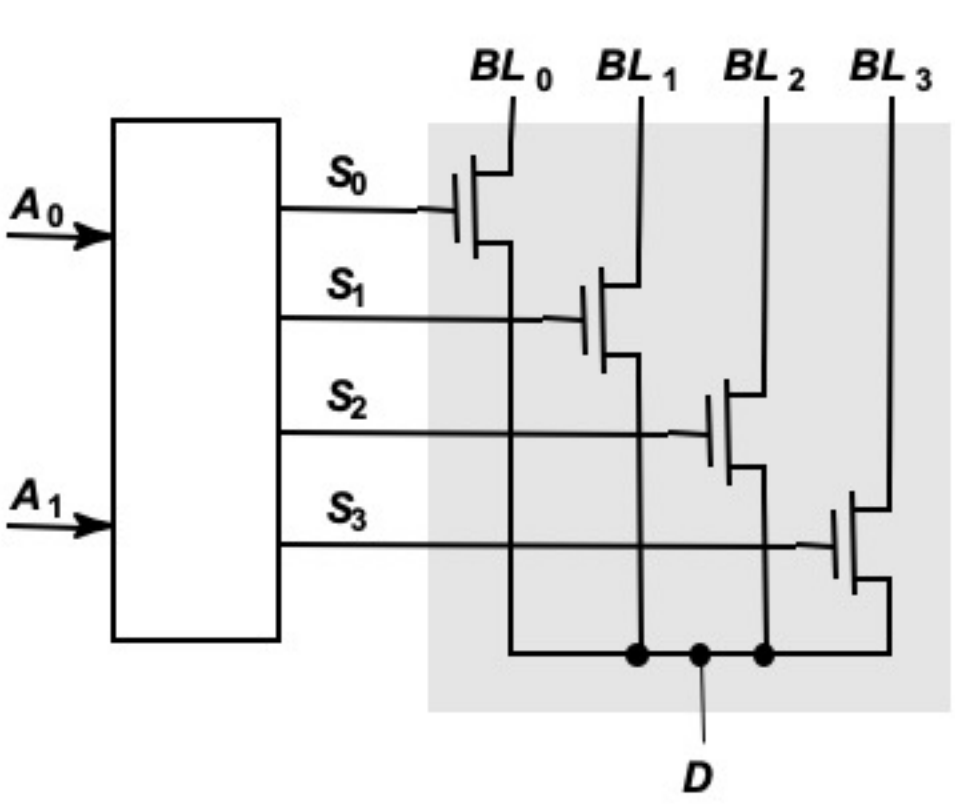


2-input NOR decoder

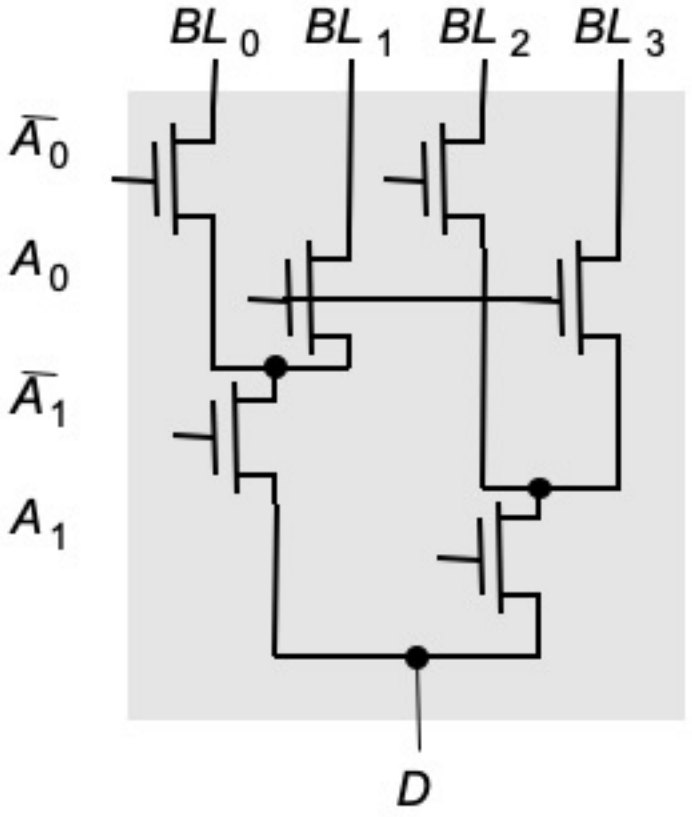


2-input NAND decoder

Column Decoders

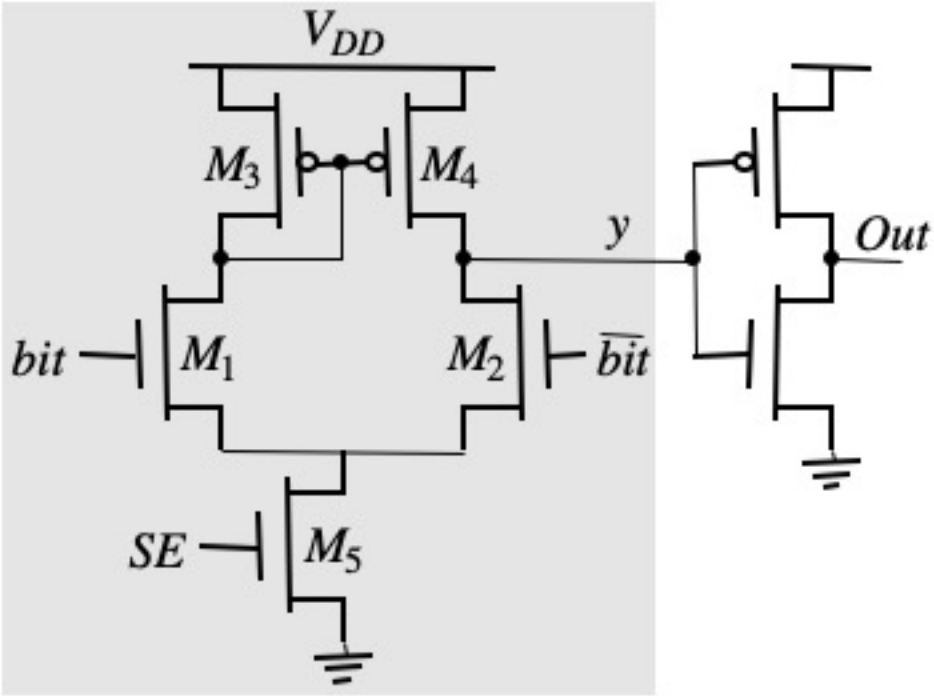


Pass-transistor with precoder

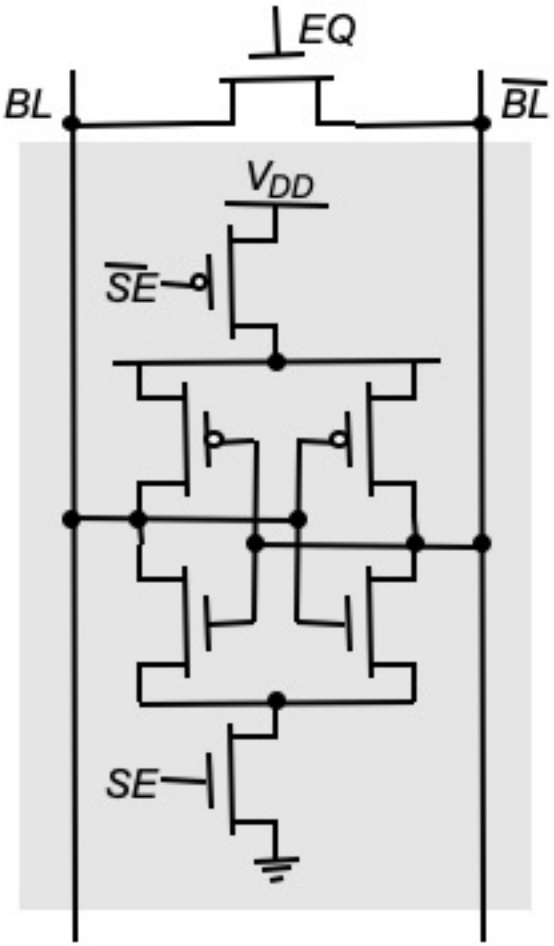


Tree

Sense Amplifier

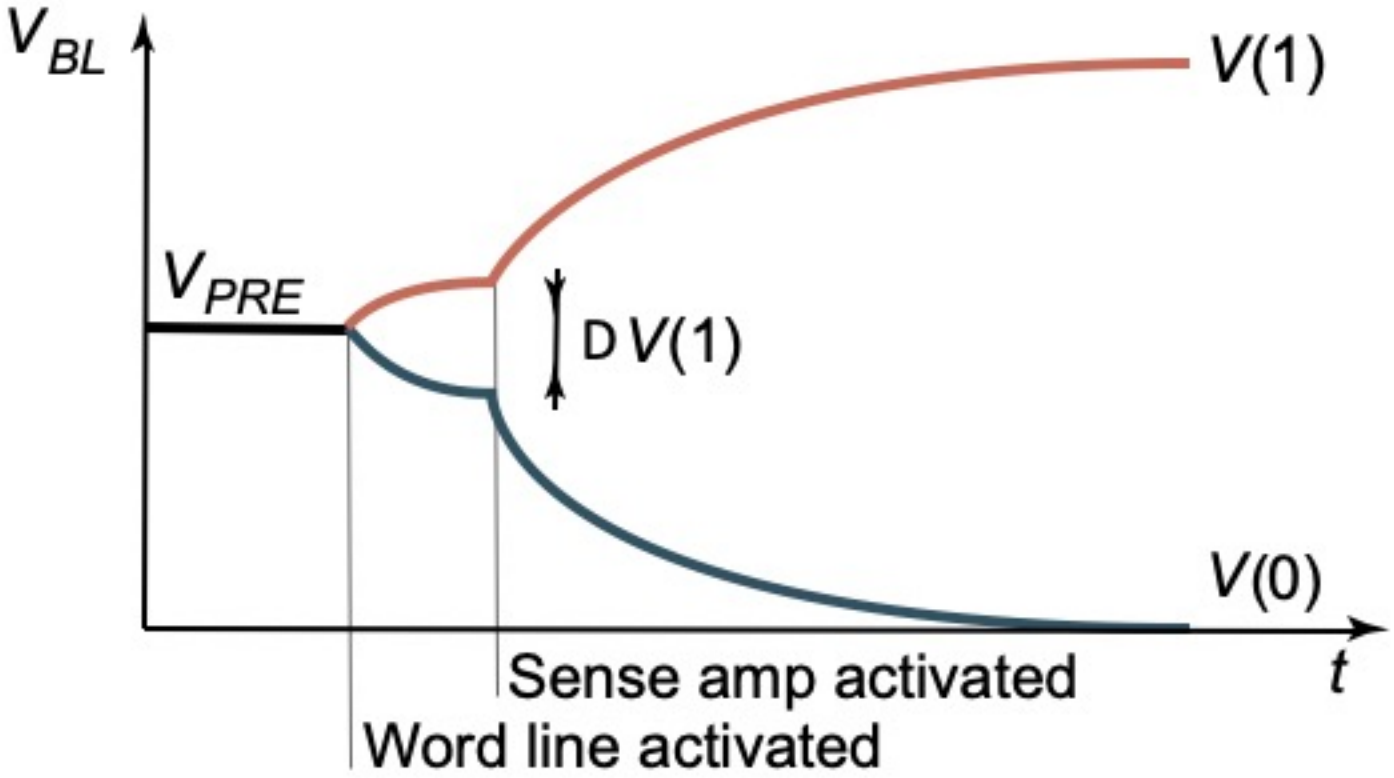


Differential amplifier



Latch-based

Sense Amplifier Operation



Open Bitline Architecture