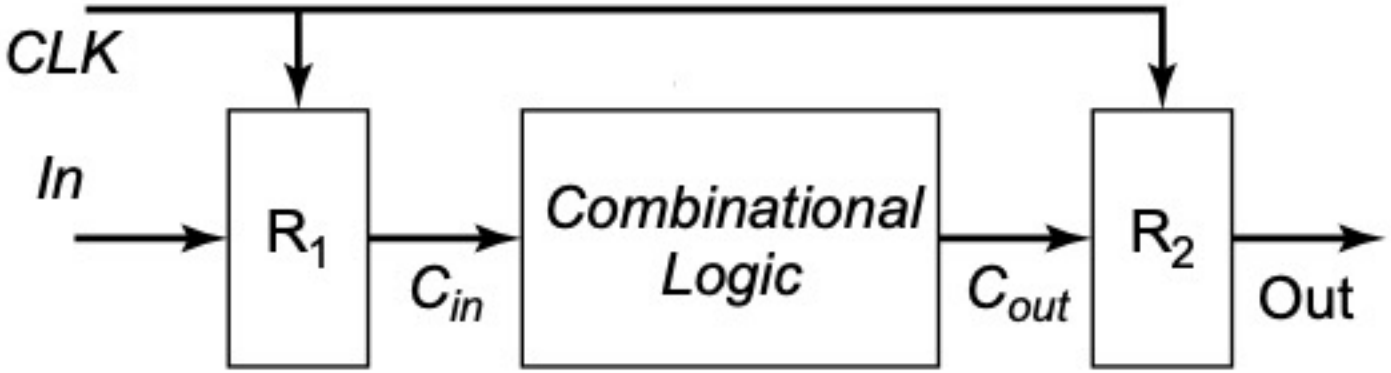
Digital ICs — Lectures

1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
4) **Circuits** [Ch. 5]	*TSEI03/TSTE86*
5) **Combinational logic** [Ch. 6]	*TSEI03/TSTE86*
6) **Sequential circuits** [Ch. 7]	*TSEI03/TSTE86*
7) **Synchronization** [Ch. 10]	*TSTE86*
8) **Adders** [Ch. 11]	*TSEI03/TSTE86*
9) **Multipliers** [Ch. 11]	*TSTE86*
10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
11) **Manufacturing** [Ch. 2]	*TSTE86*
12) **System design** [Ch. 8]	*TSTE86*

Synchronous System

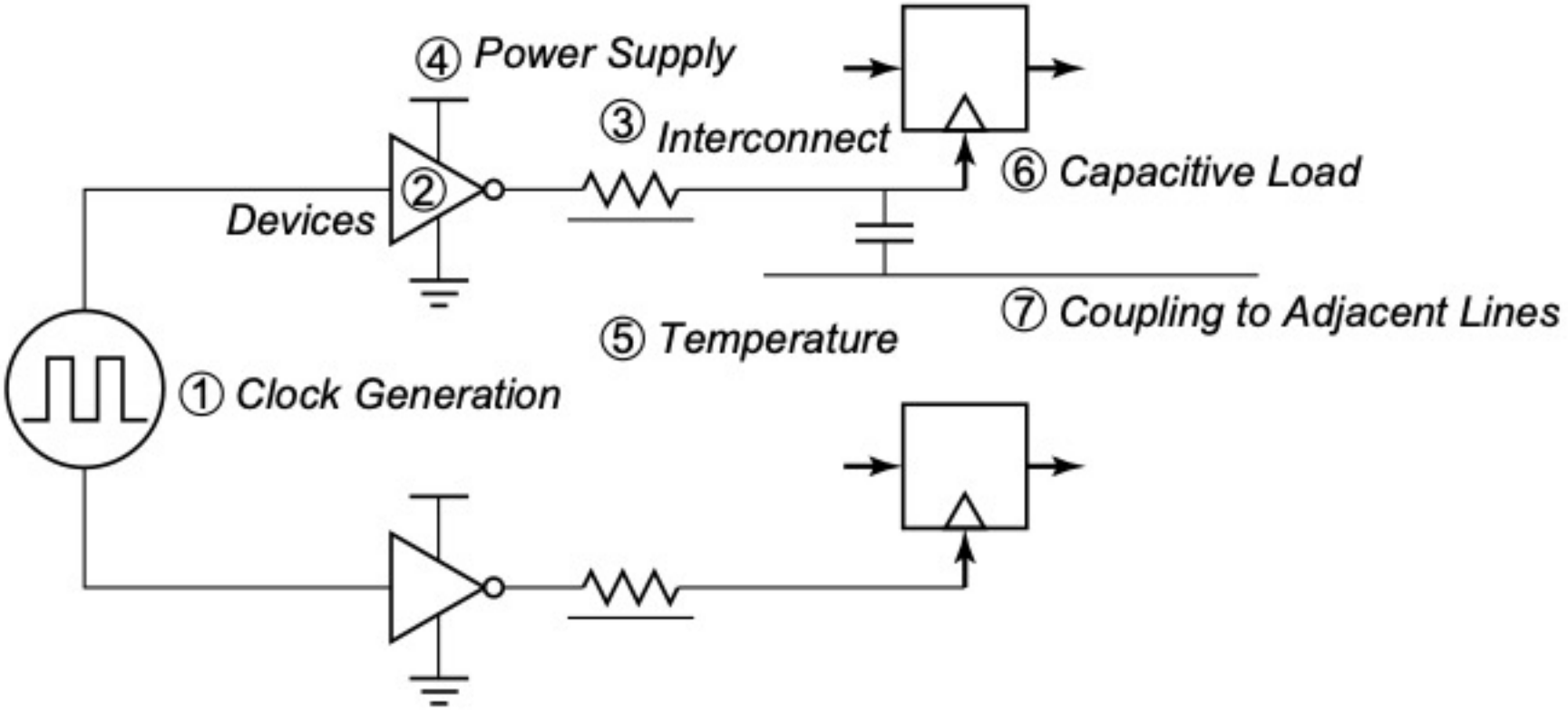


Timing parameters

$t_{c\text{-}q,cd} \ldots t_{c\text{-}q}$ $t_{logic,cd} \ldots t_{logic}$

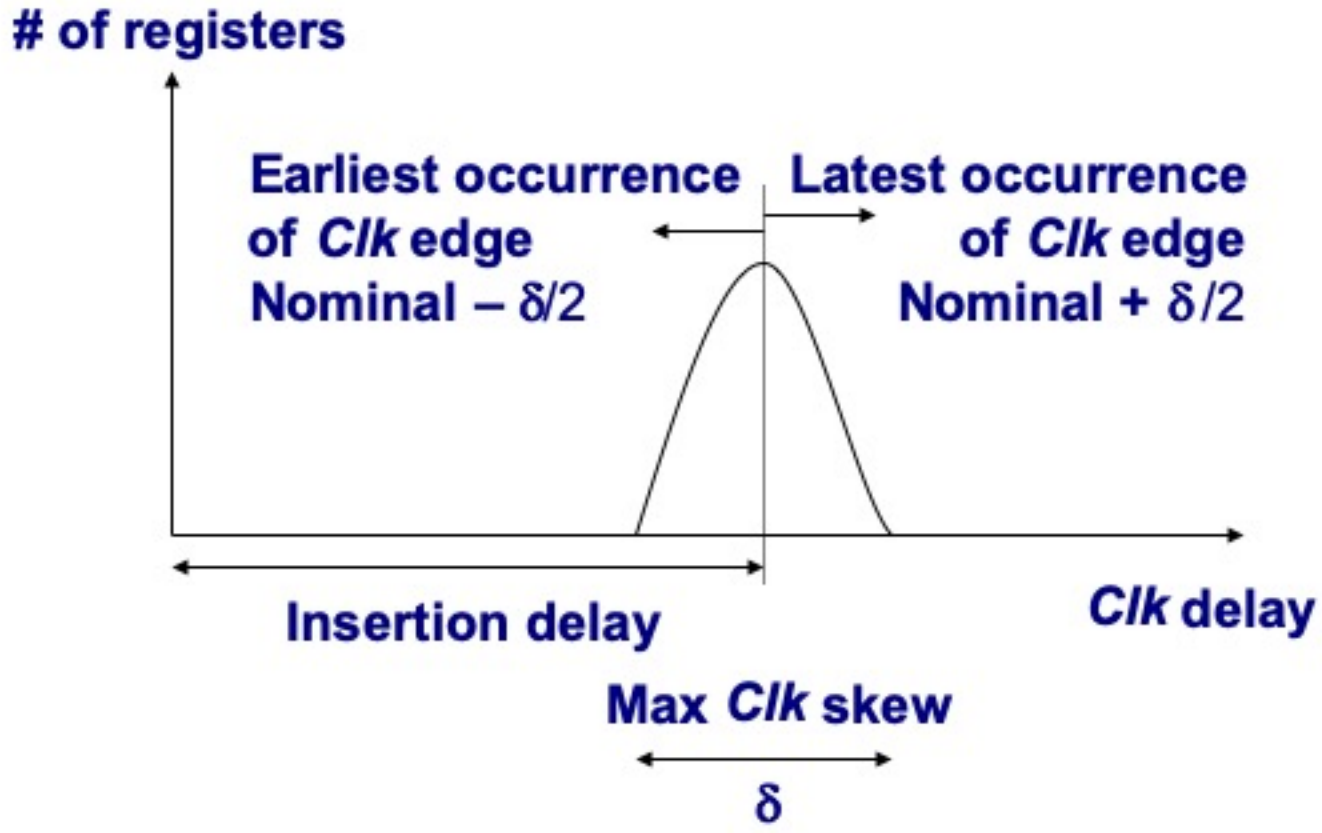
t_{su}, t_{hold}

Clock Uncertainties

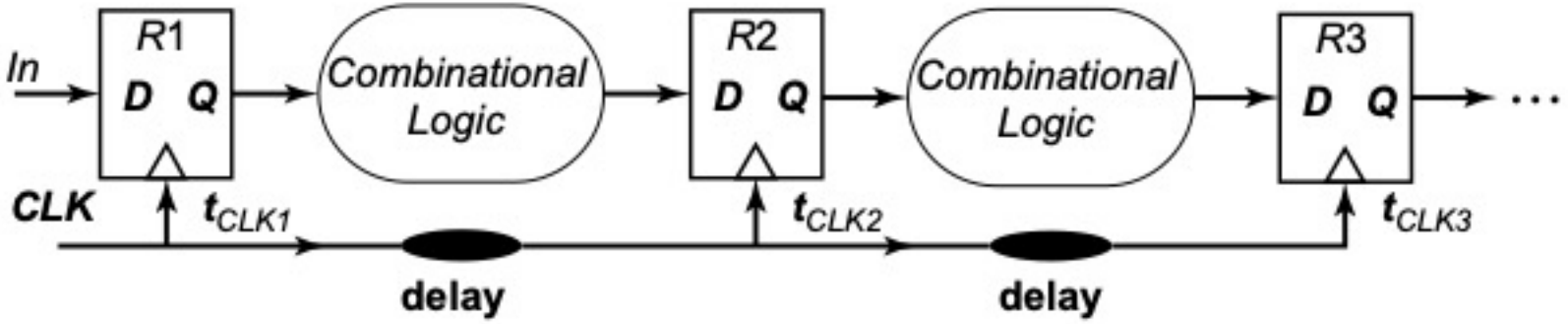


Sources of clock uncertainty

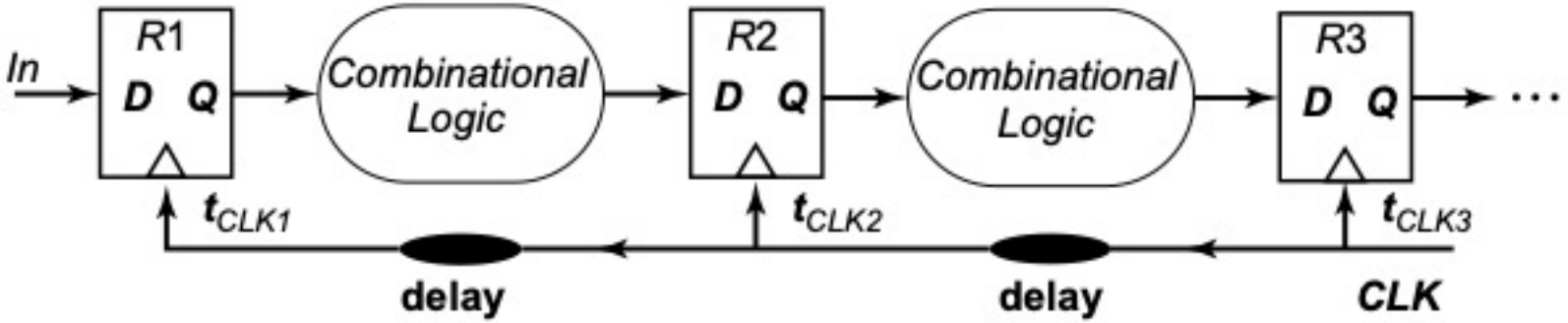
Clock Skew


# of registers
Earliest occurrence of *Clk* edge Nominal – δ/2
Latest occurrence of *Clk* edge Nominal + δ/2
Insertion delay
Clk delay
Max *Clk* skew
δ

Clock Skew

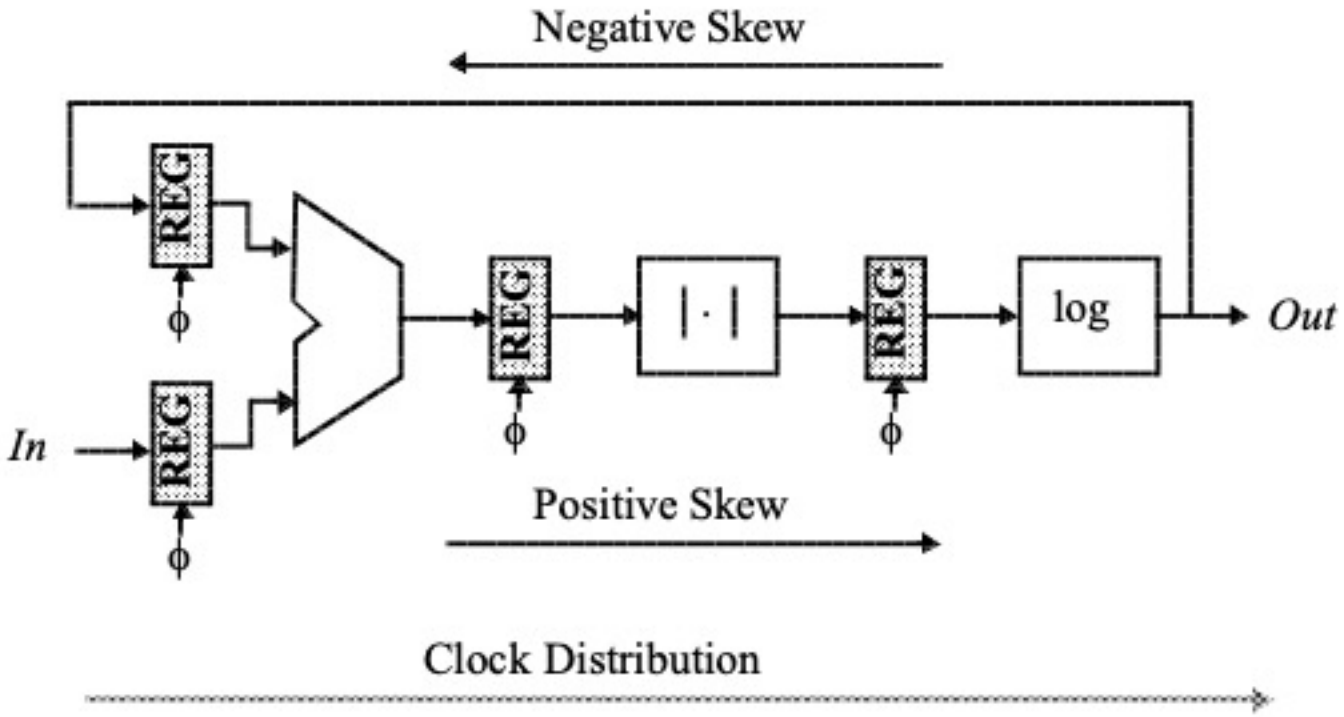


(a) Positive skew



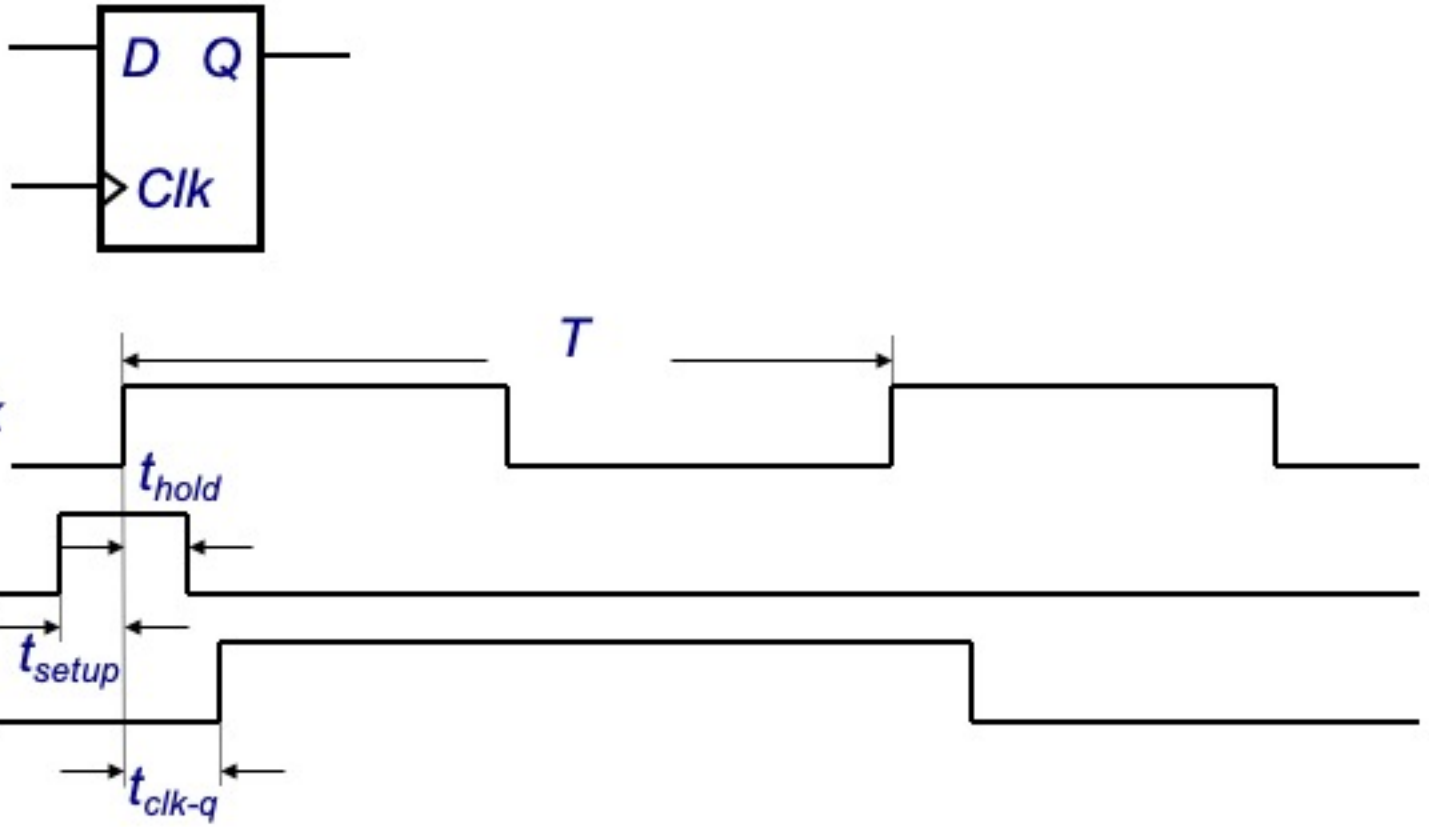
(b) Negative skew

Positive and Negative Skew

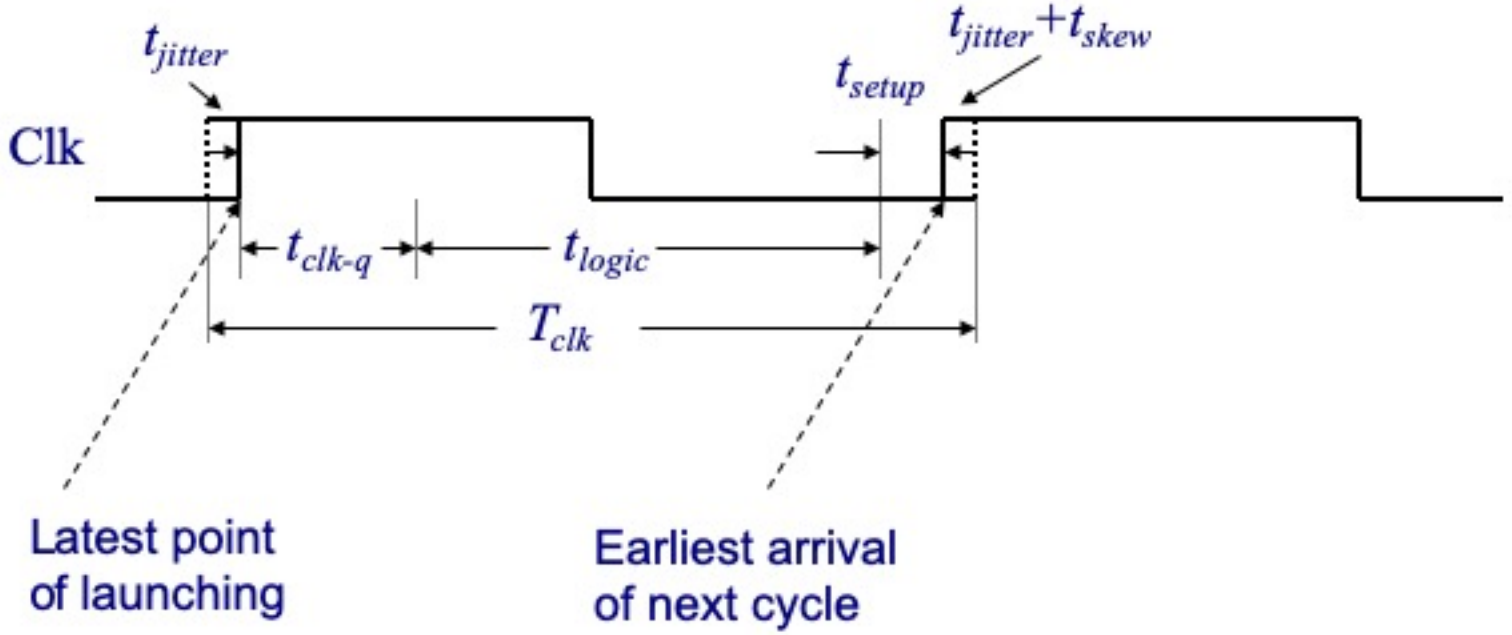


Data and Clock Routing

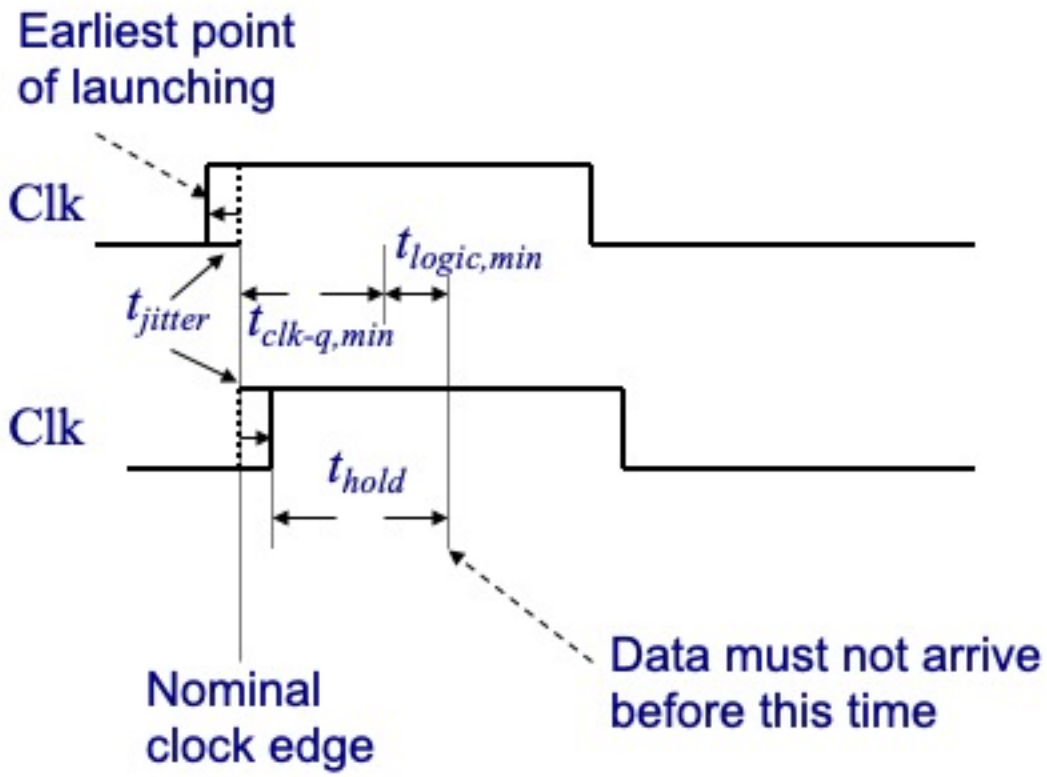
Register Parameters



Longest Path

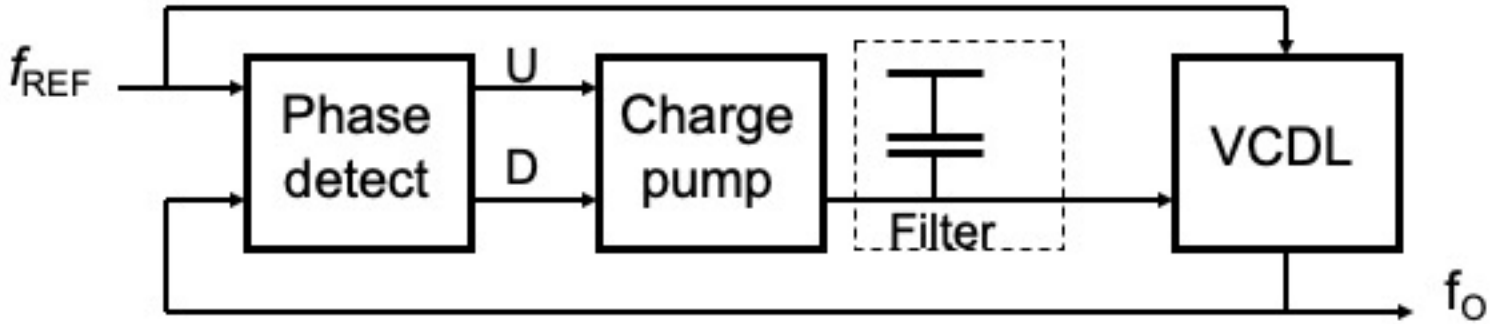


Shortest Path

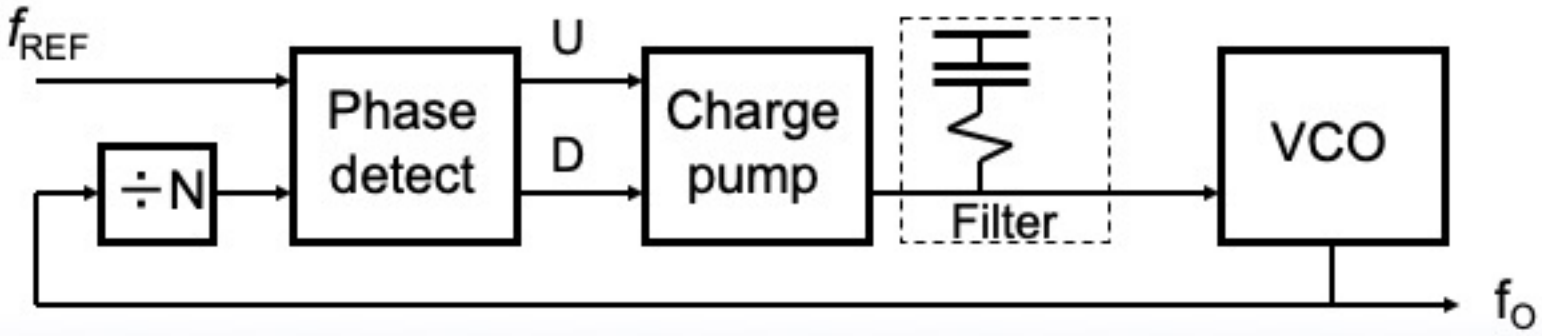


Clock Generation

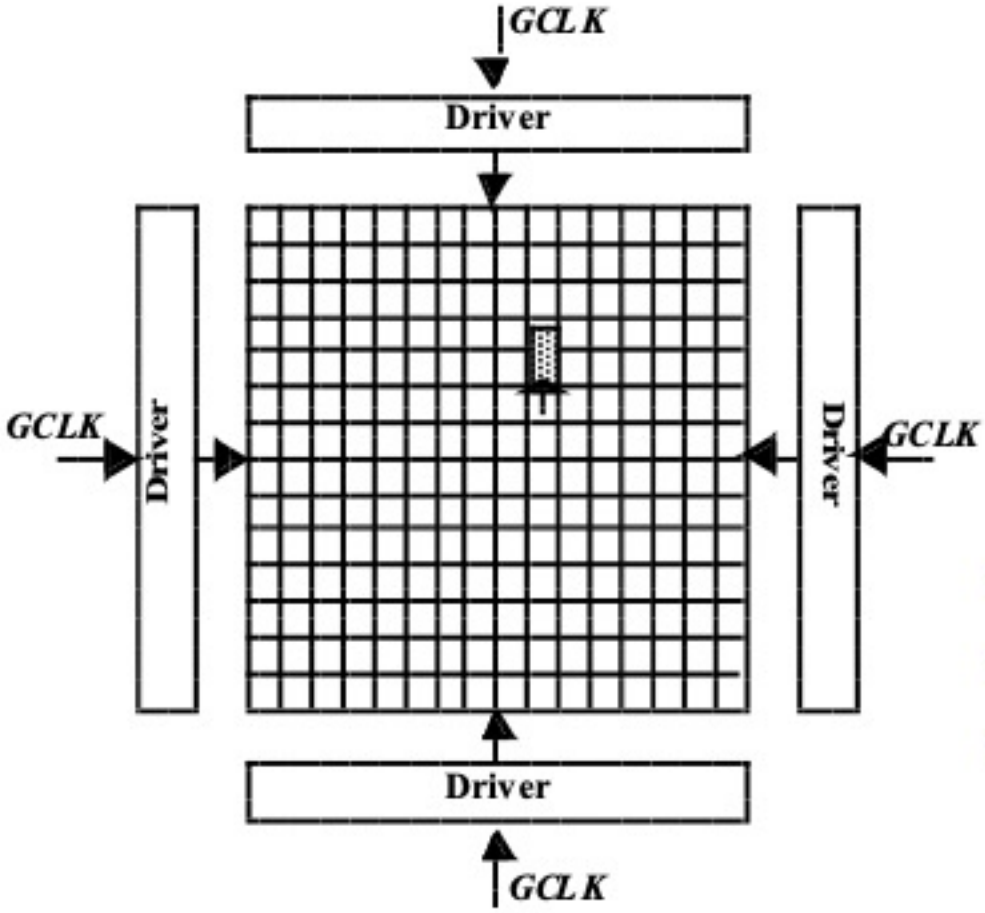
Delay-Locked Loop (Delay Line Based)



Phase-Locked Loop (VCO-Based)

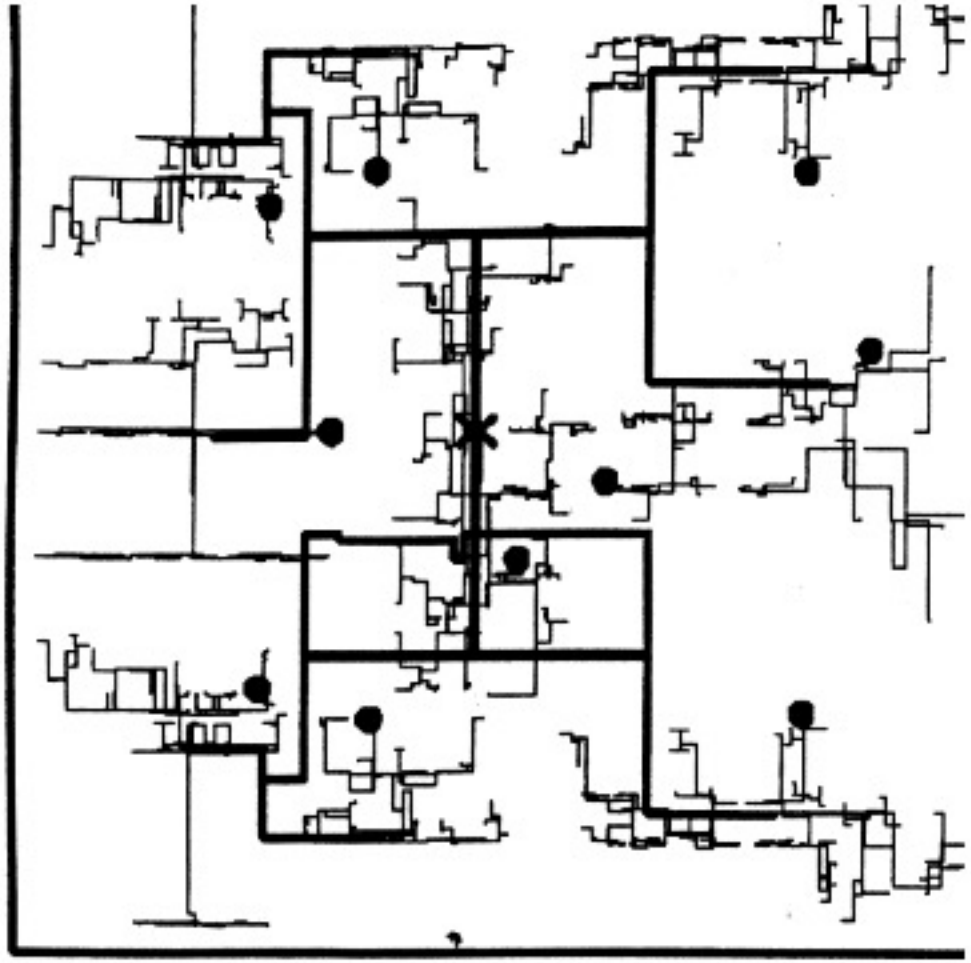


Clock Grid



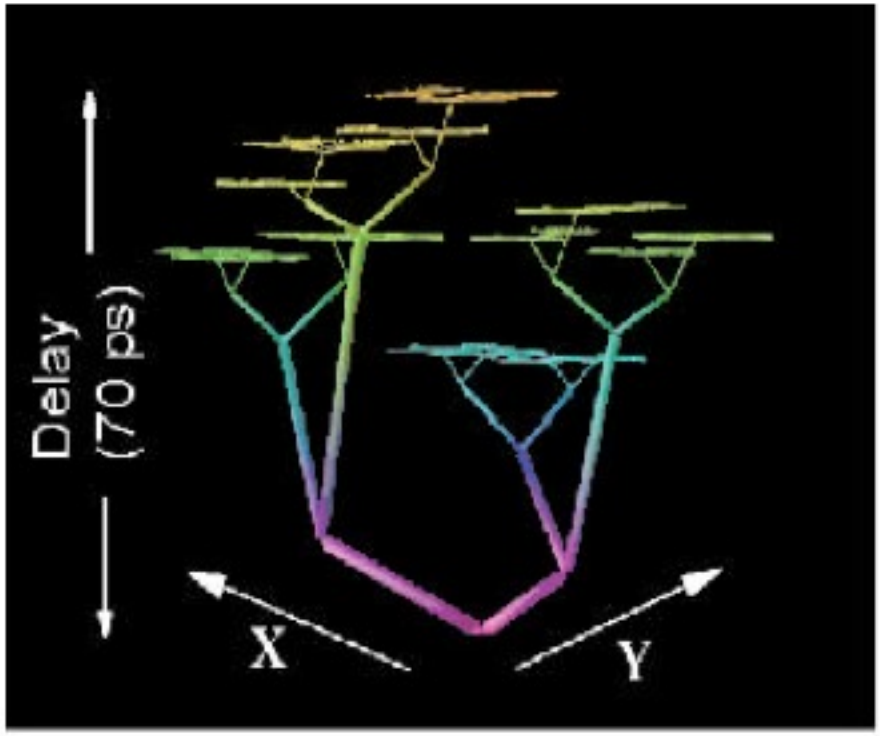
- Low skew
- No RC matching
- Huge power

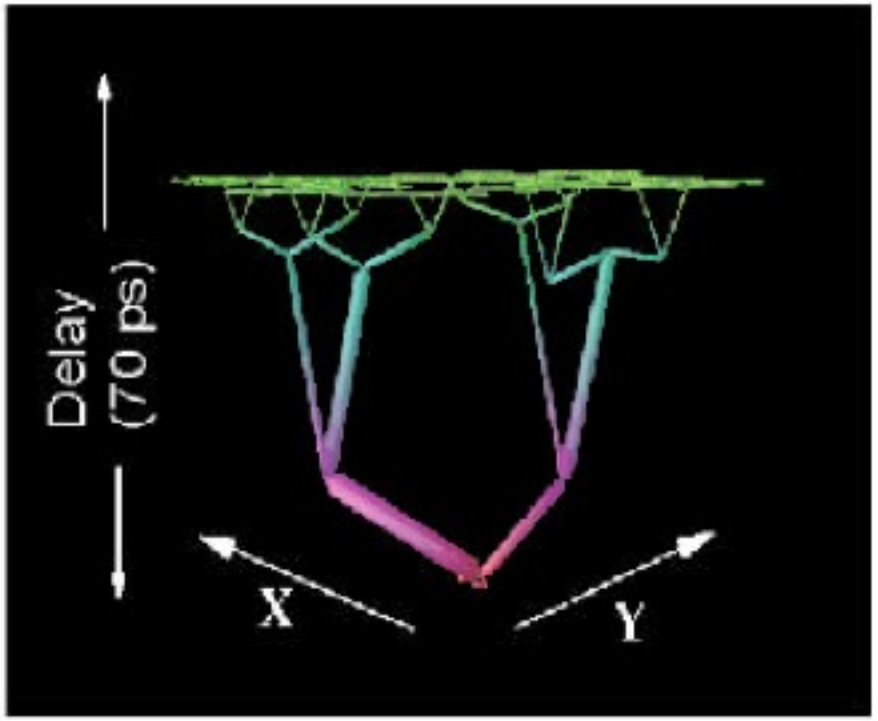
RC-matched H-tree



[Restle98]

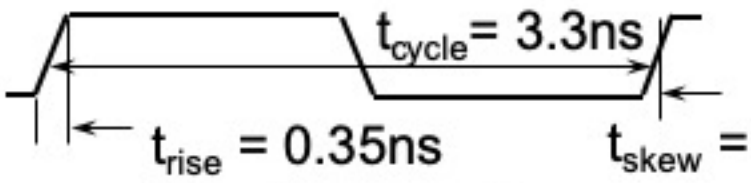
Tuning Tree with Wire Width



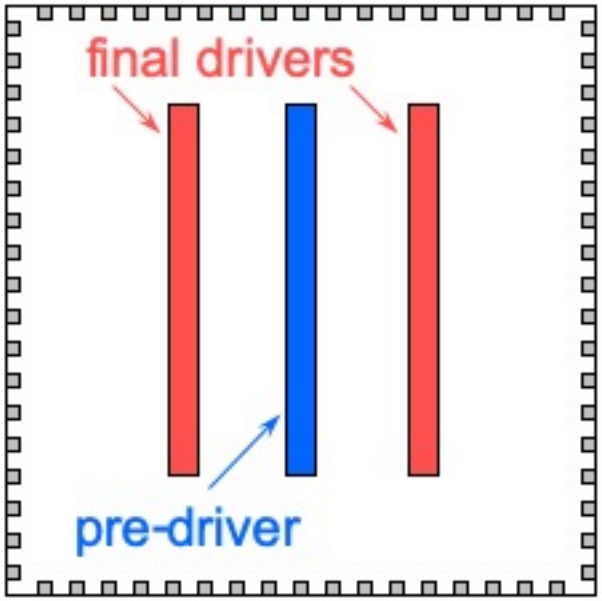


[Restle01]

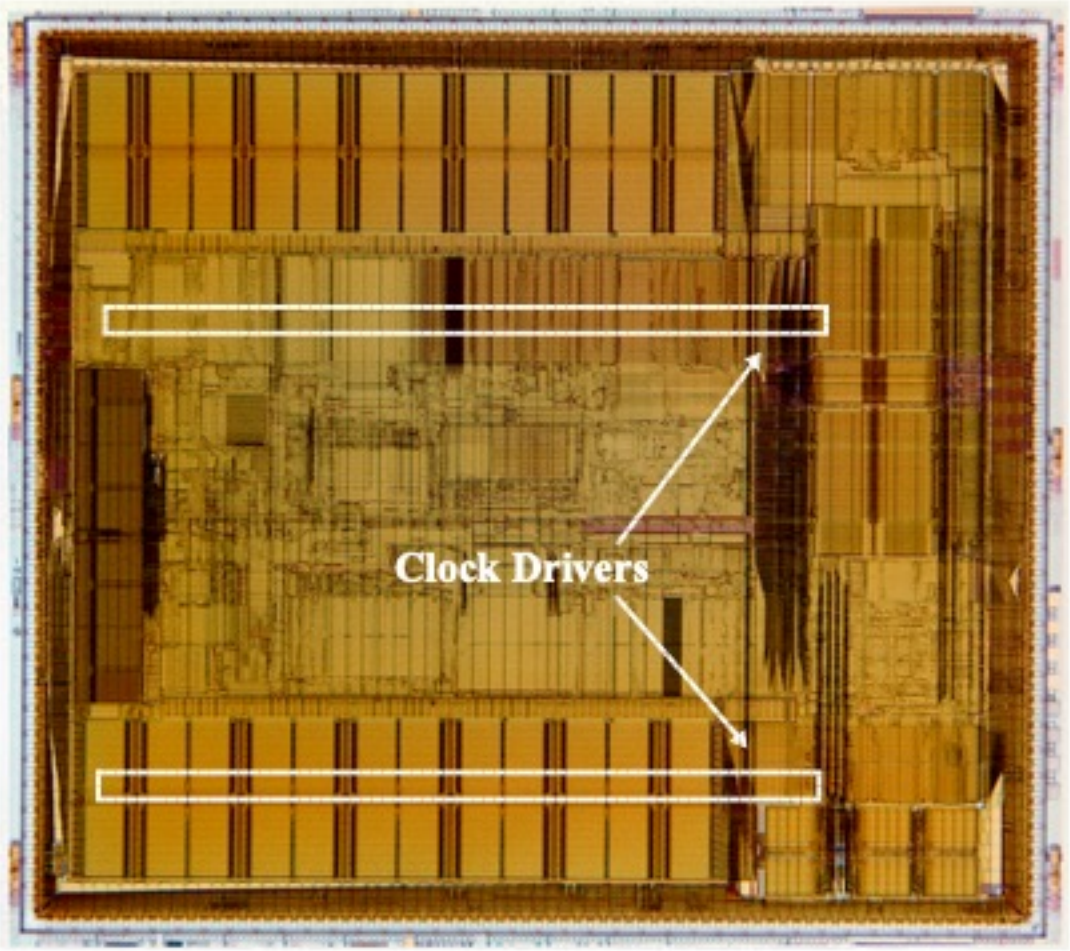
Example: DEC Alpha 21164



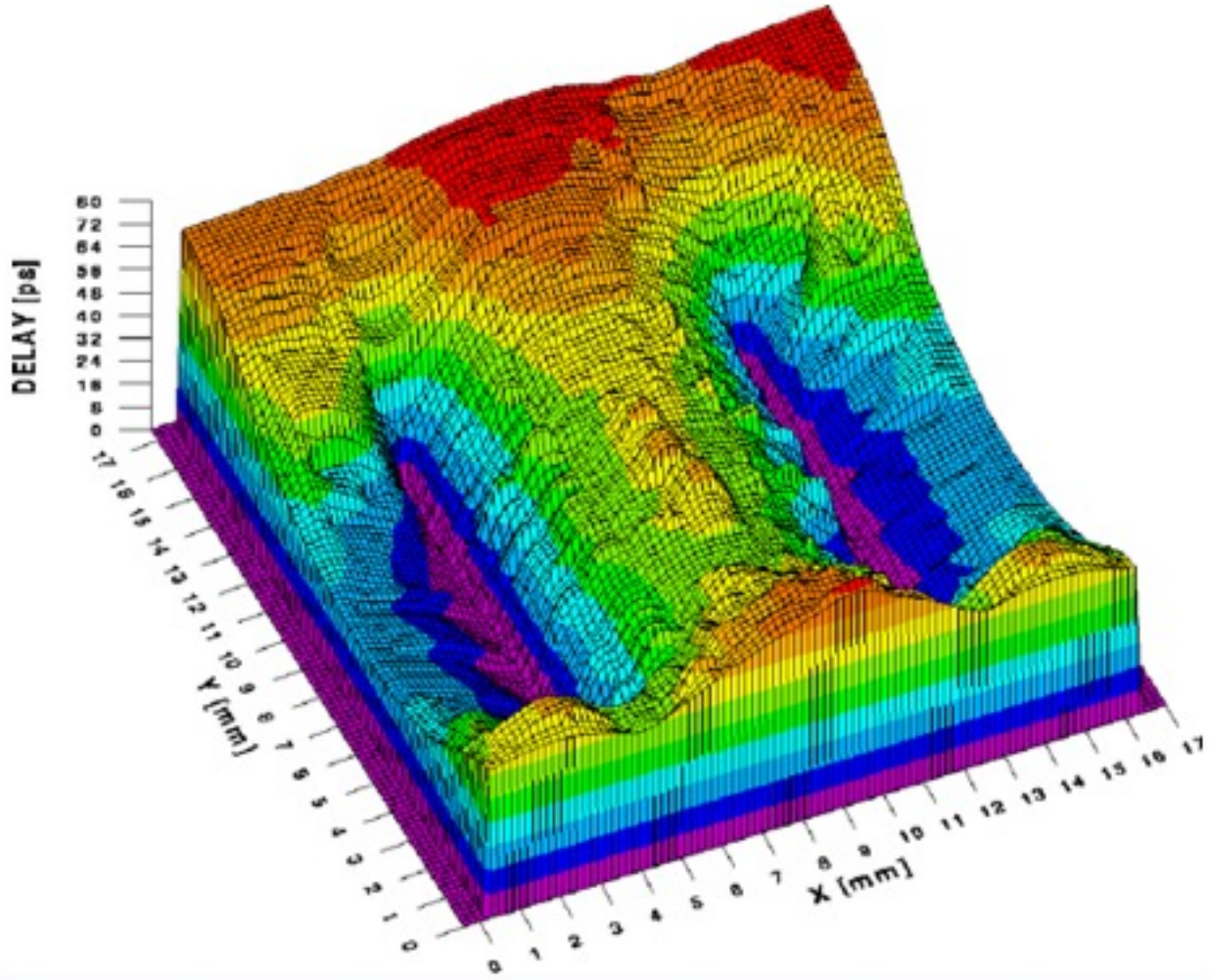
Clock waveform



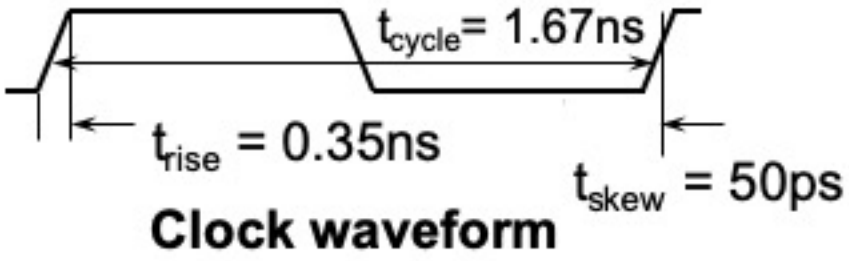
Clock driver



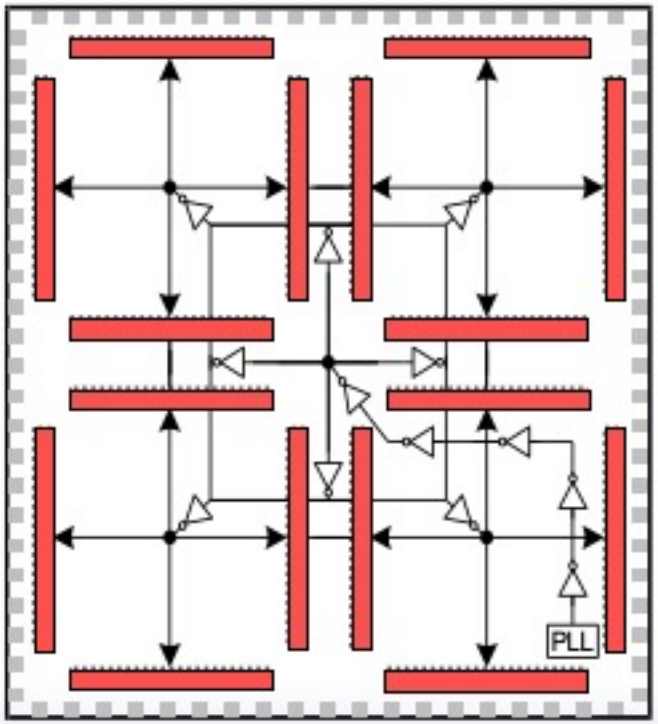
Clock Skew



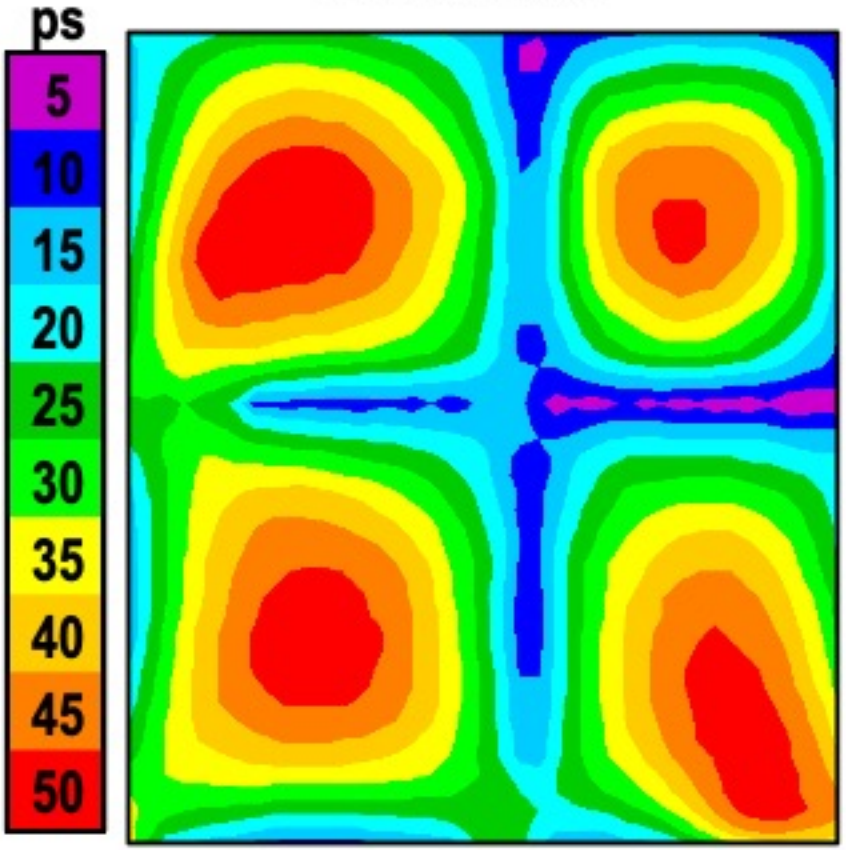
Example: DEC Alpha 21264



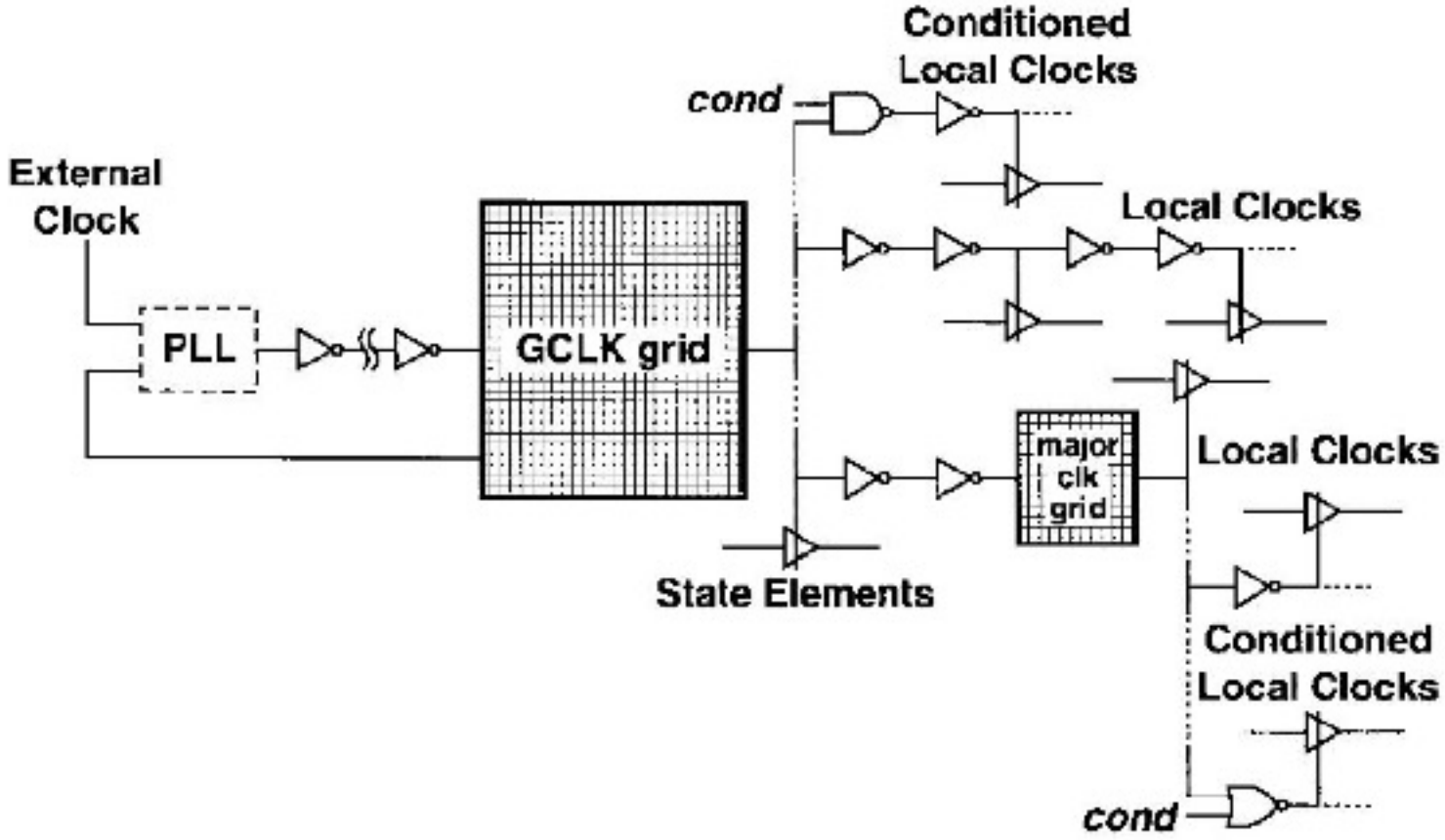
Clock waveform



Clock skew

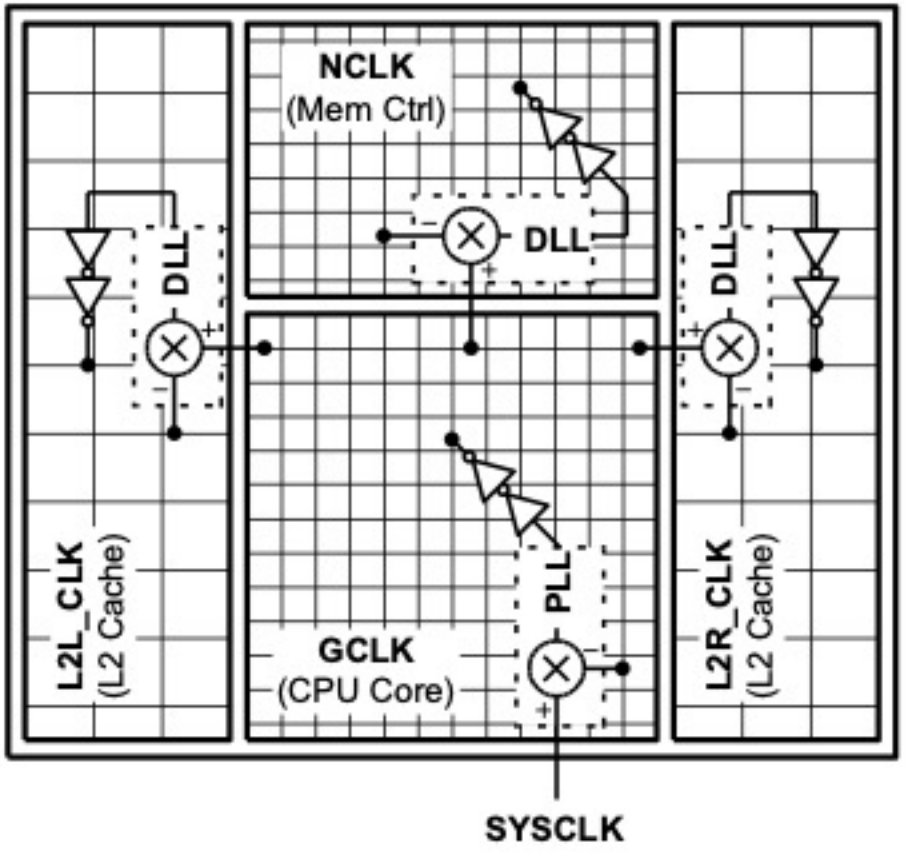


21264 Clocking



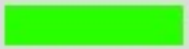
Example: DEC Alpha 21364

Active Skew Management and Multiple Clock Domains

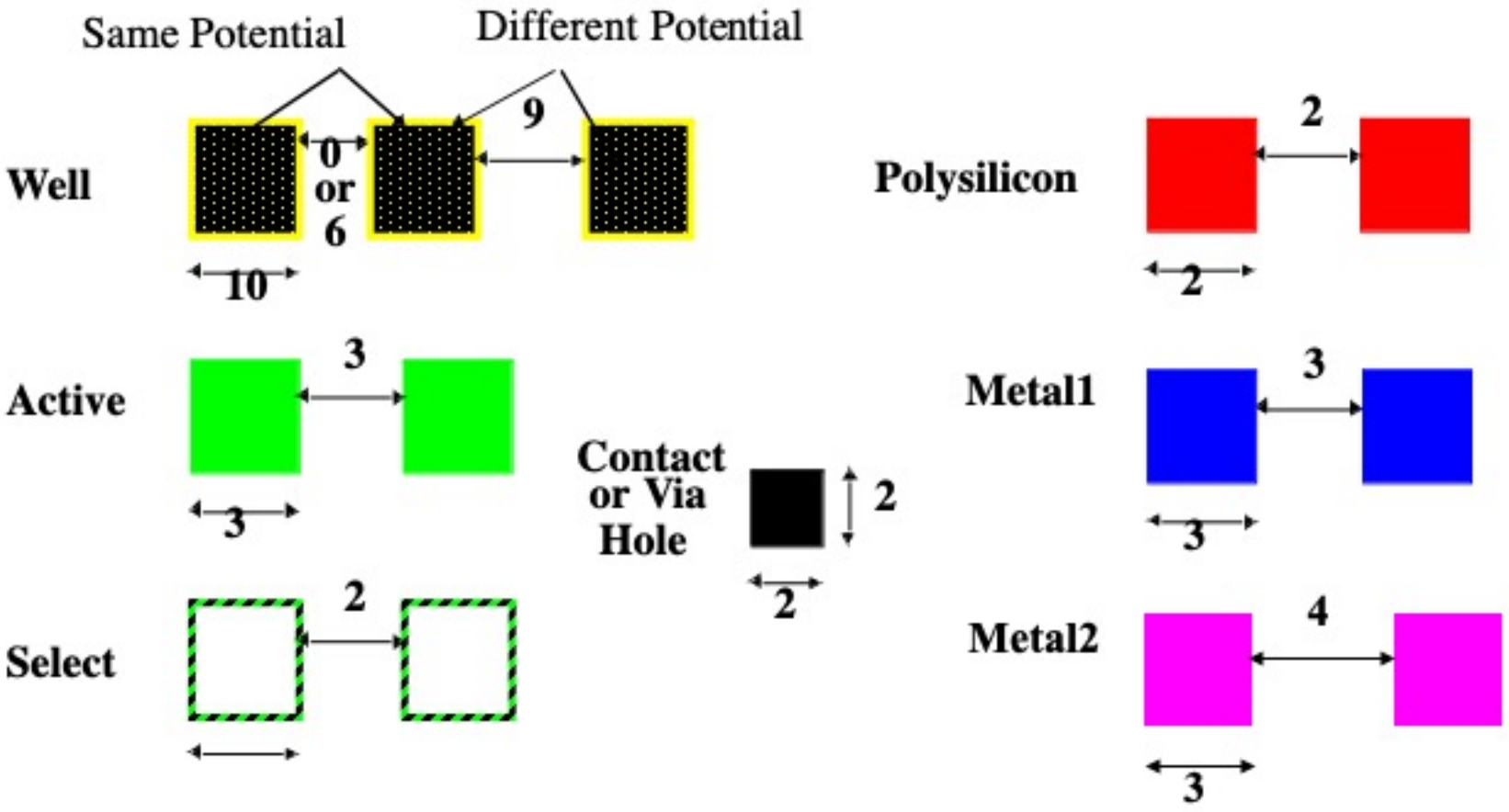


+ widely dispersed drivers
+ DLLs compensate static and low-frequency variation
+ divides design and verification effort
– DLL design and verification is added work
+ tailored clocks

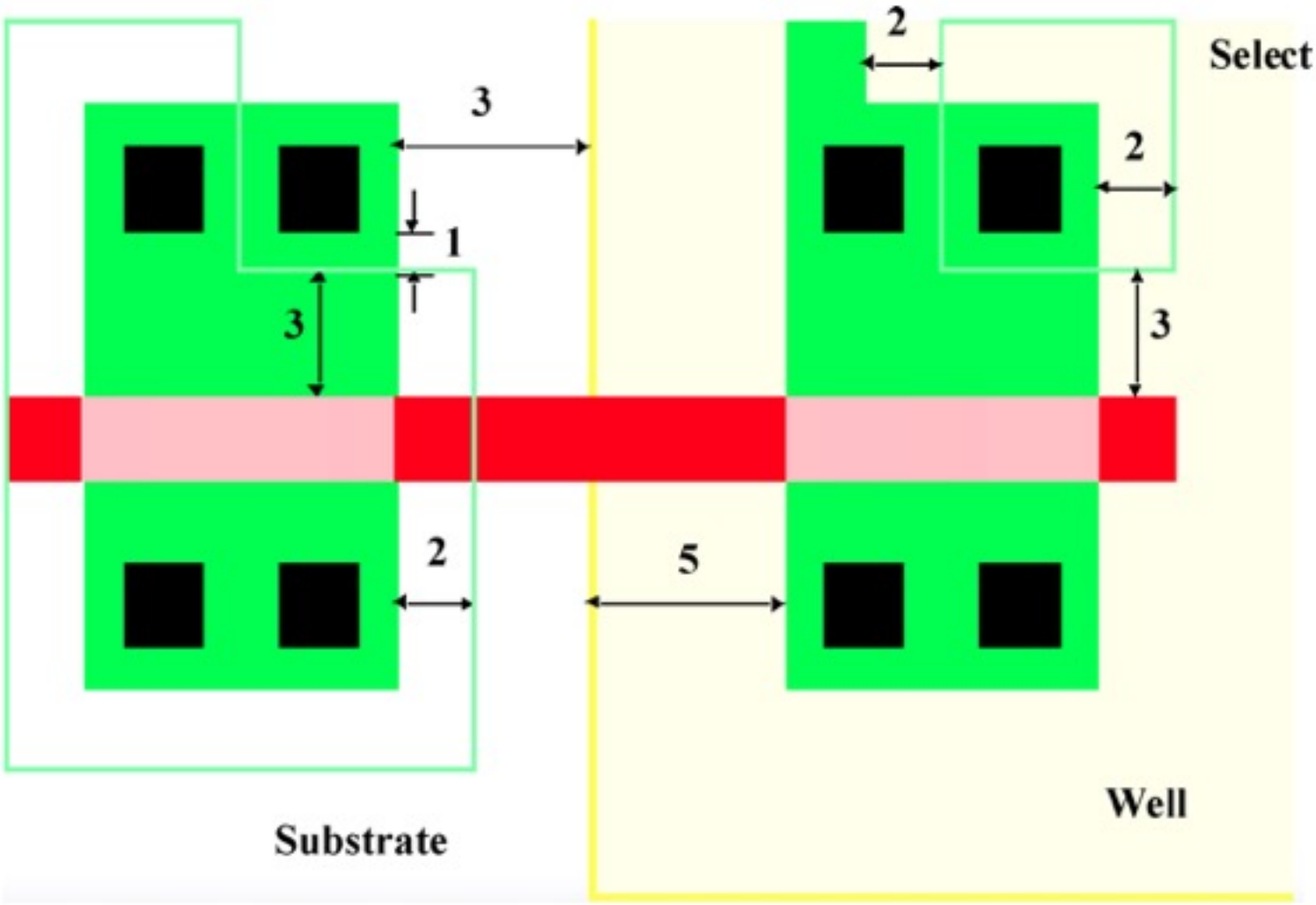
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

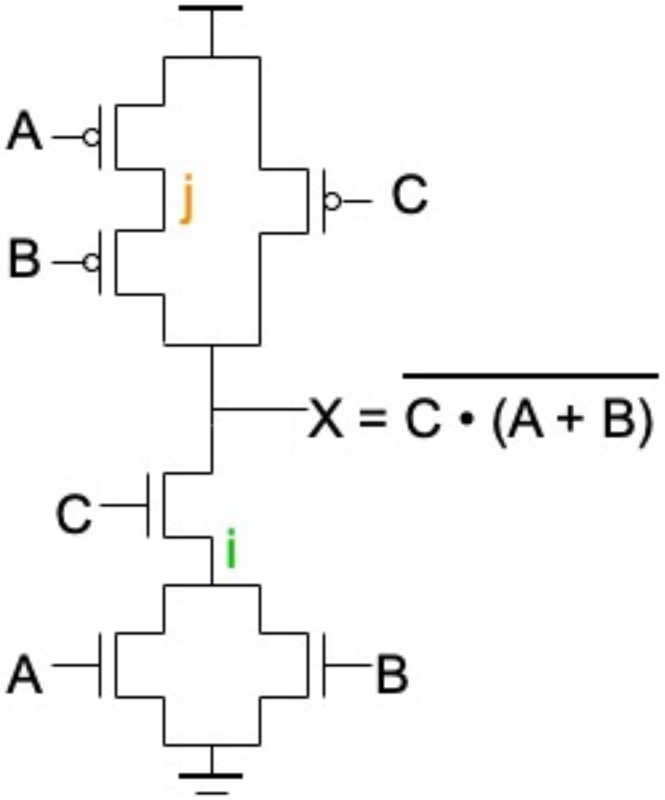
Intra-Layer Design Rules

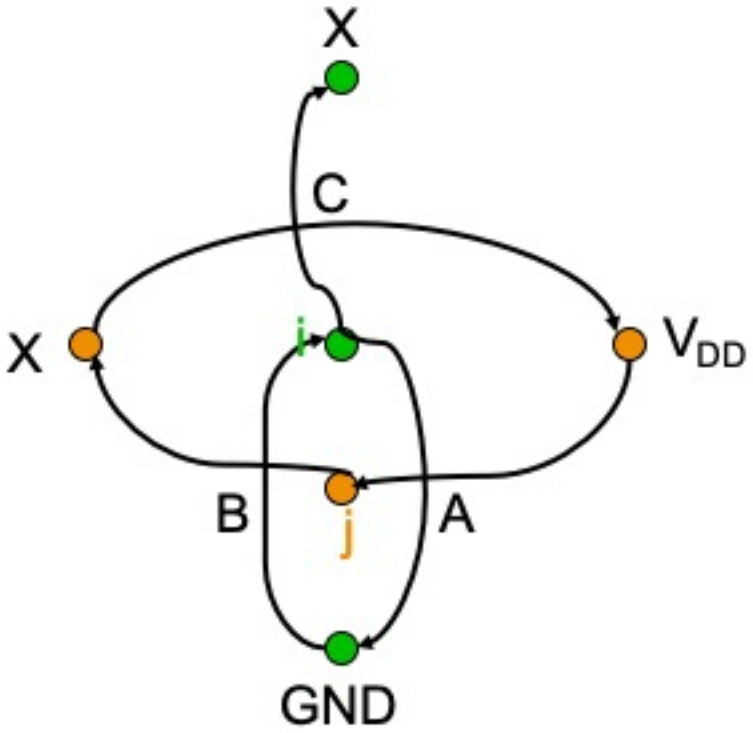


Inter-Layer Design Rules



Common Euler Paths





Common Euler paths:
A-B-C

Layout from Euler Paths