Digital ICs — Lectures

1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
4) **Circuits** [Ch. 5]	*TSEI03/TSTE86*
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7) **Synchronization** [Ch. 10]	*TSTE86*
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10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
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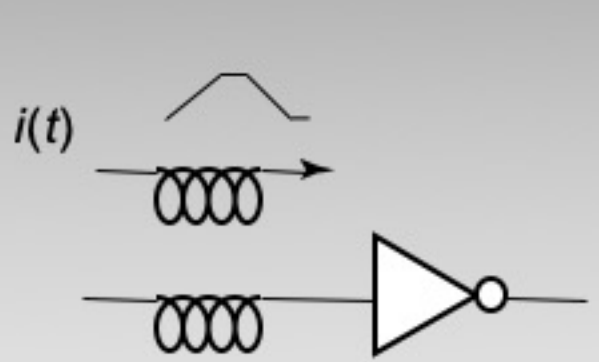
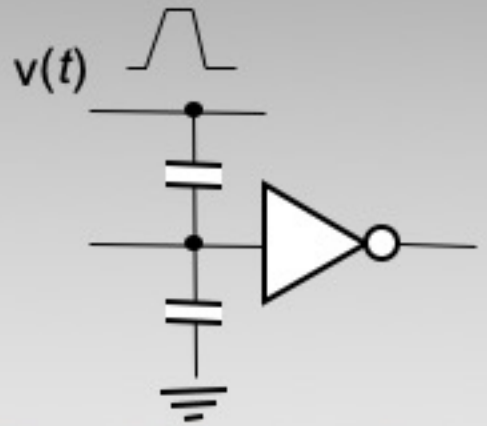
12) **System design** [Ch. 8]	*TSTE86*

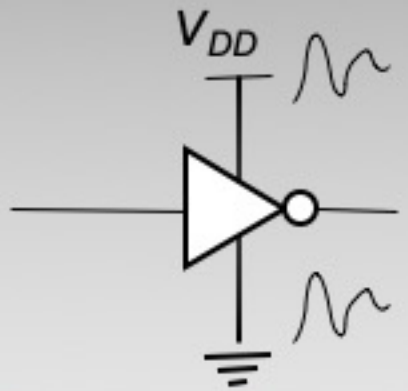
On-Chip Noise



Inductive coupling

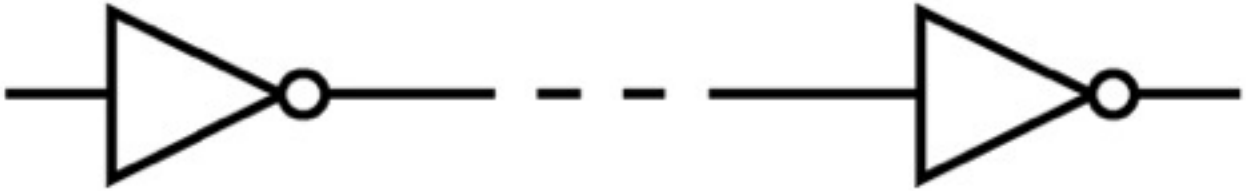


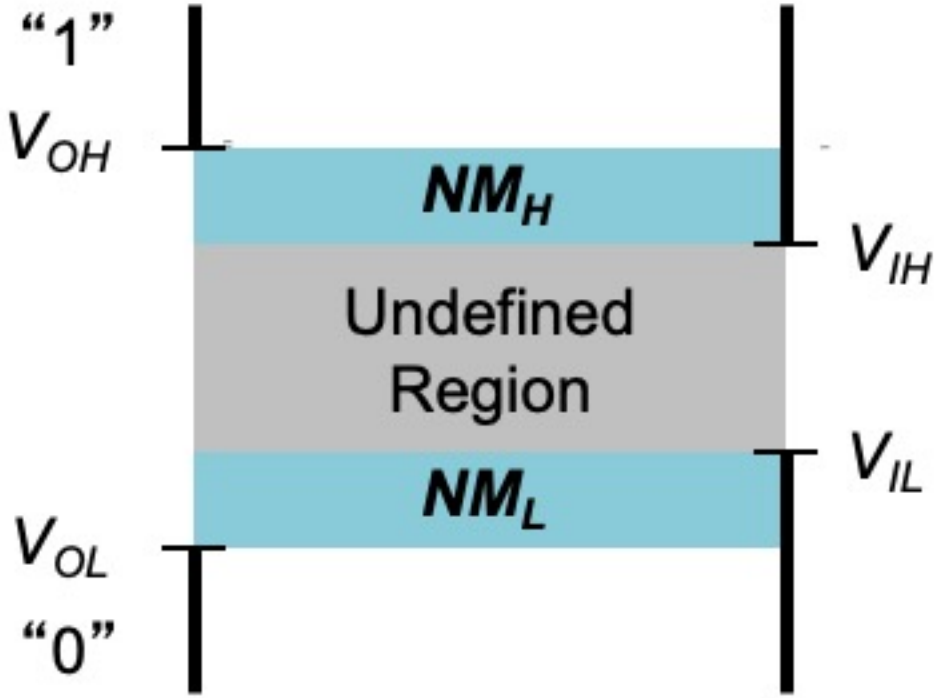
Capacitive coupling



Power and ground noise

Noise Margins

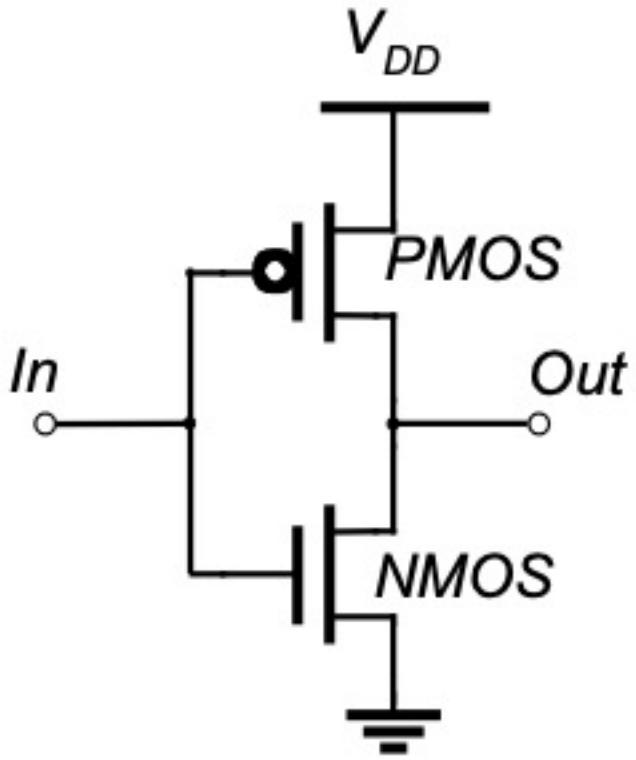


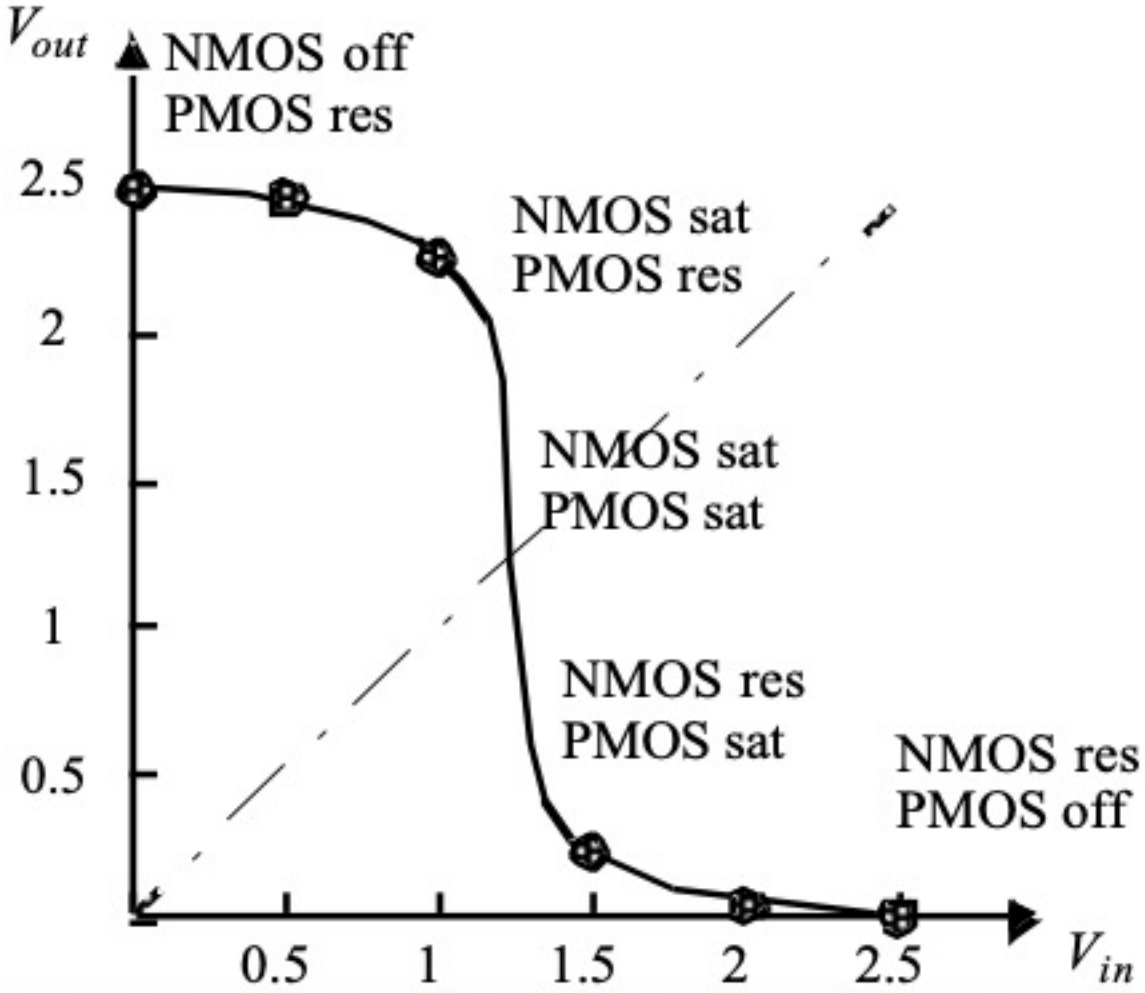


Noise margin high:
$NM_H = V_{OH} - V_{IH}$

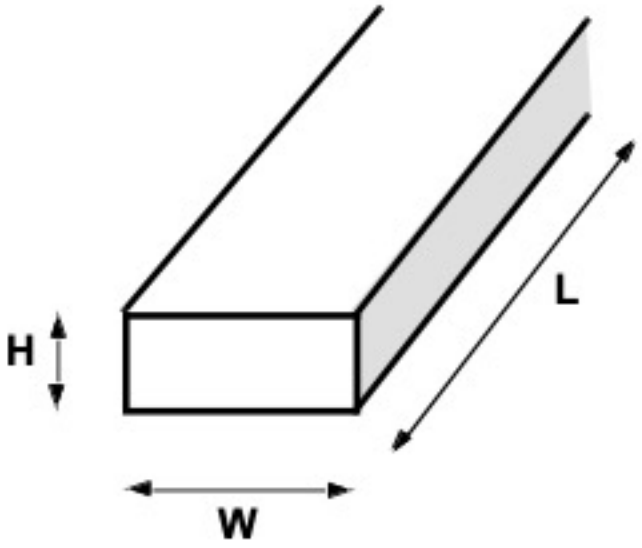
Noise margin low:
$NM_L = V_{IL} - V_{OL}$

CMOS Inverter





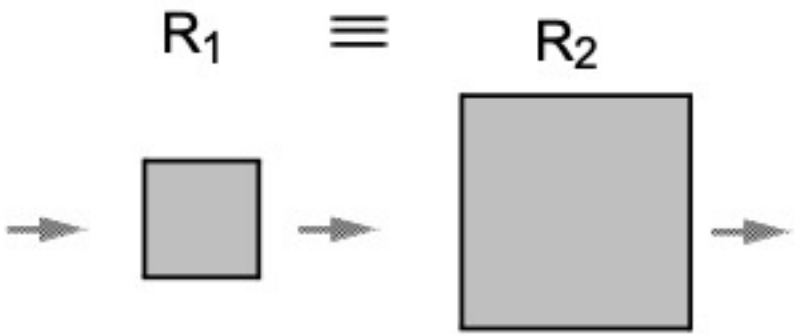
Wire Resistance



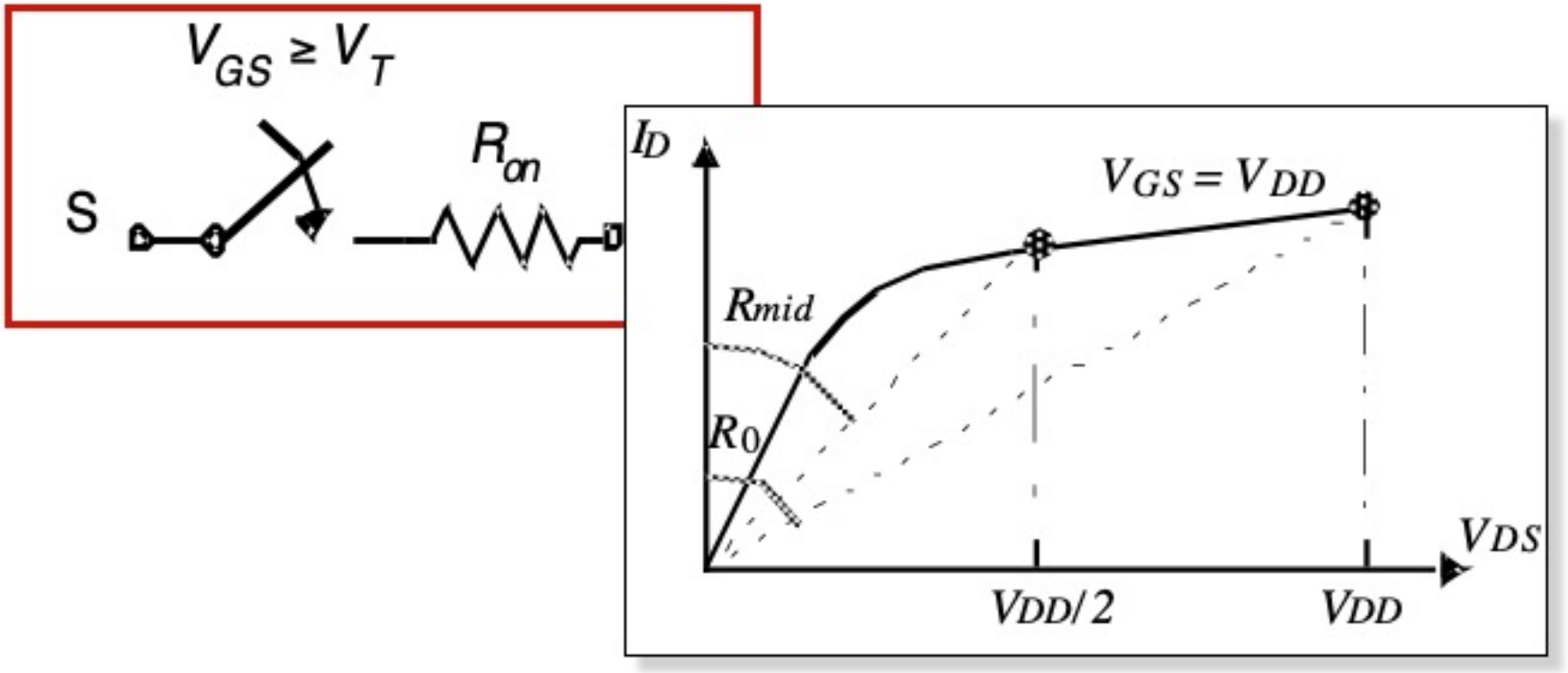
$$R = \rho \frac{L}{HW}$$

Sheet Resistance

R_o

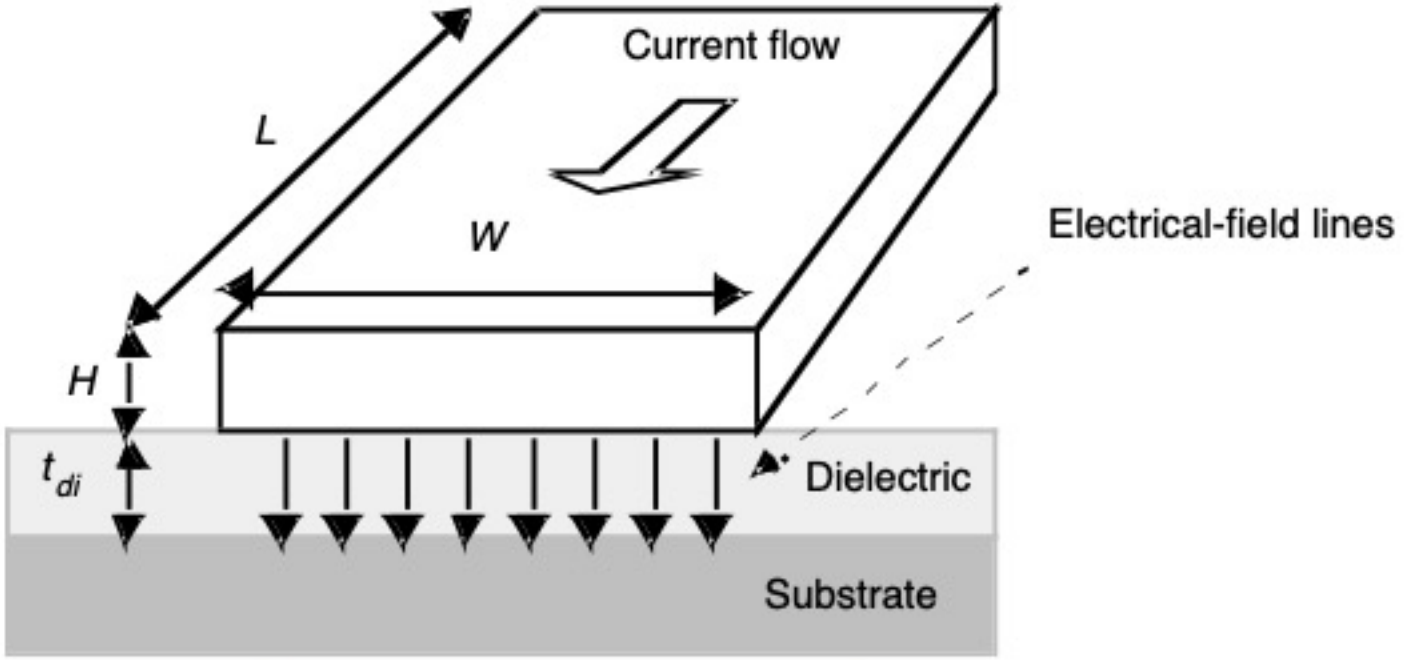


Resistance of the MOSFET Channel



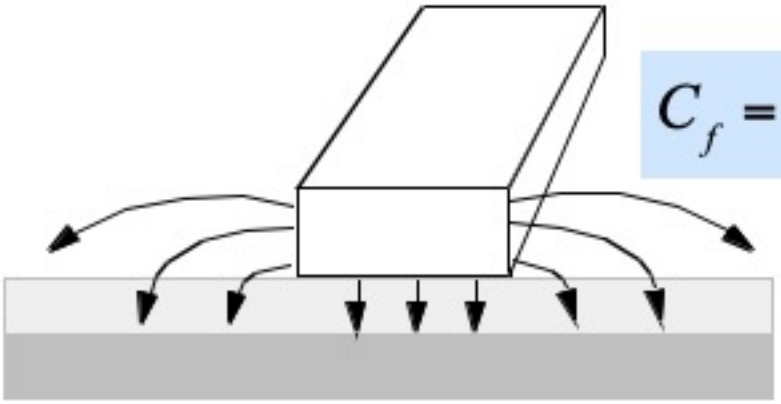
Example : assuming velocity saturation in range $V_{DD} \geq V_{DS} \geq \frac{V_{DD}}{2} \Rightarrow R_{on} \approx \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}} + \frac{V_{DD}/2}{I_{DSAT}}\right) = \frac{3}{4} \cdot \frac{V_{DD}}{I_{DSAT}}$

Parallel Plate Capacitance



$$C_{pp} = \varepsilon_{di} \frac{WL}{t_{di}} = C_{area} WL$$

Fringing Capacitance

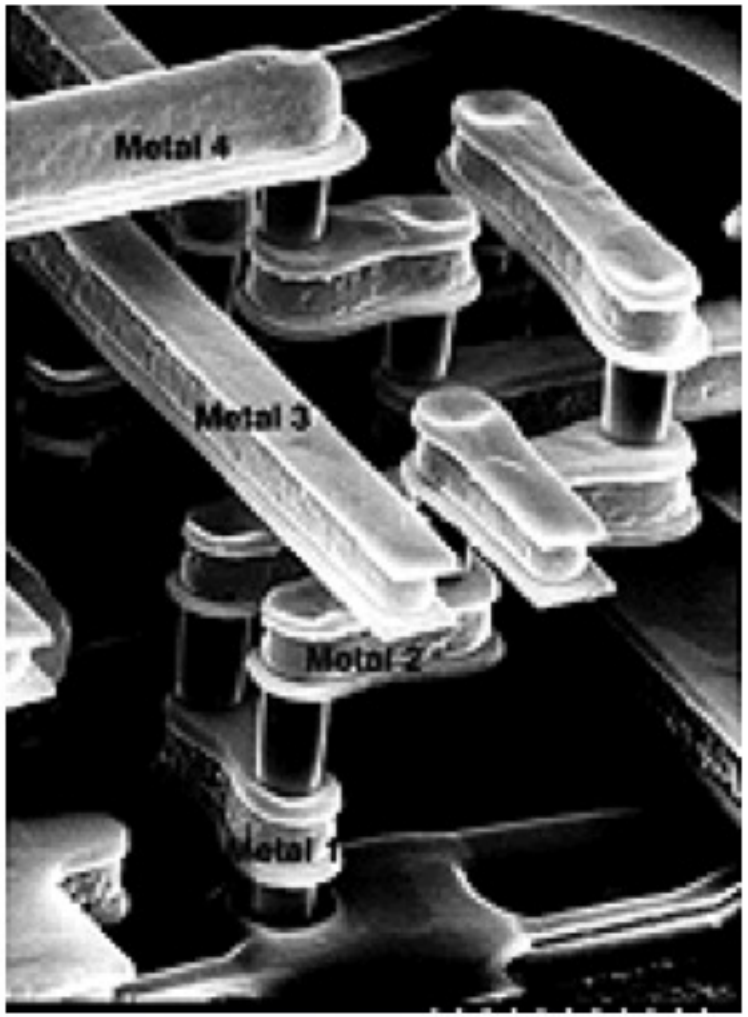


$$C_f = 2C_{edge}L$$

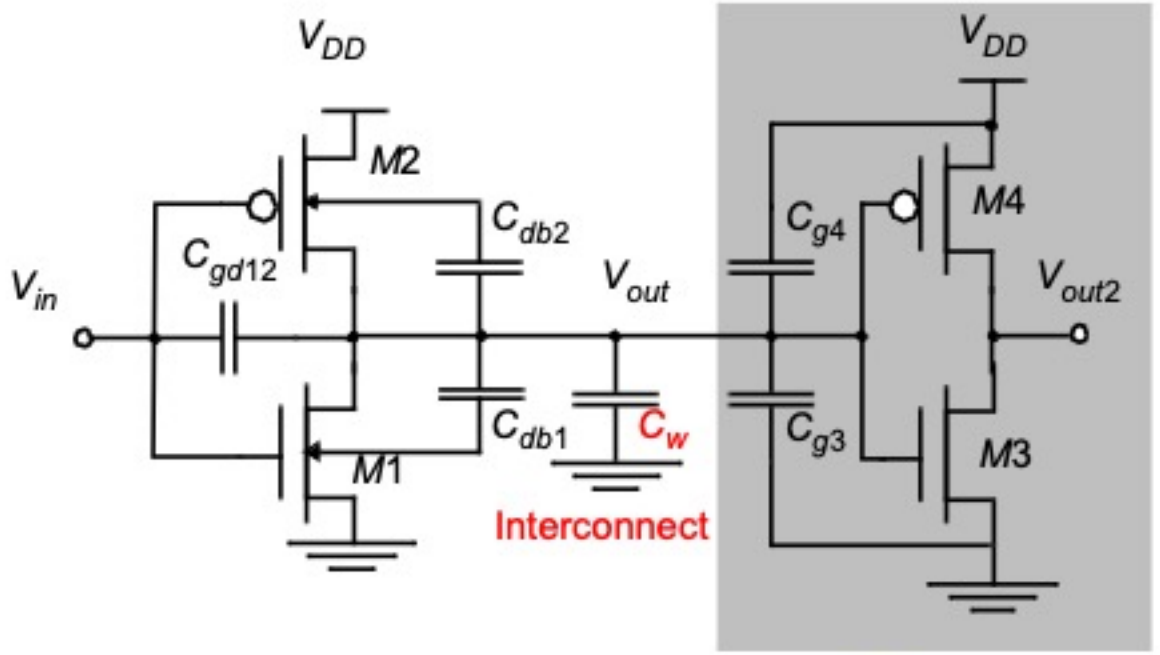
Total wire capacitance:

$$C_{wire} = C_{pp} + C_f = C_{area}WL + 2C_{edge}L$$

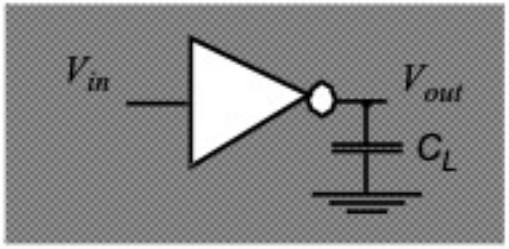
Interconnect



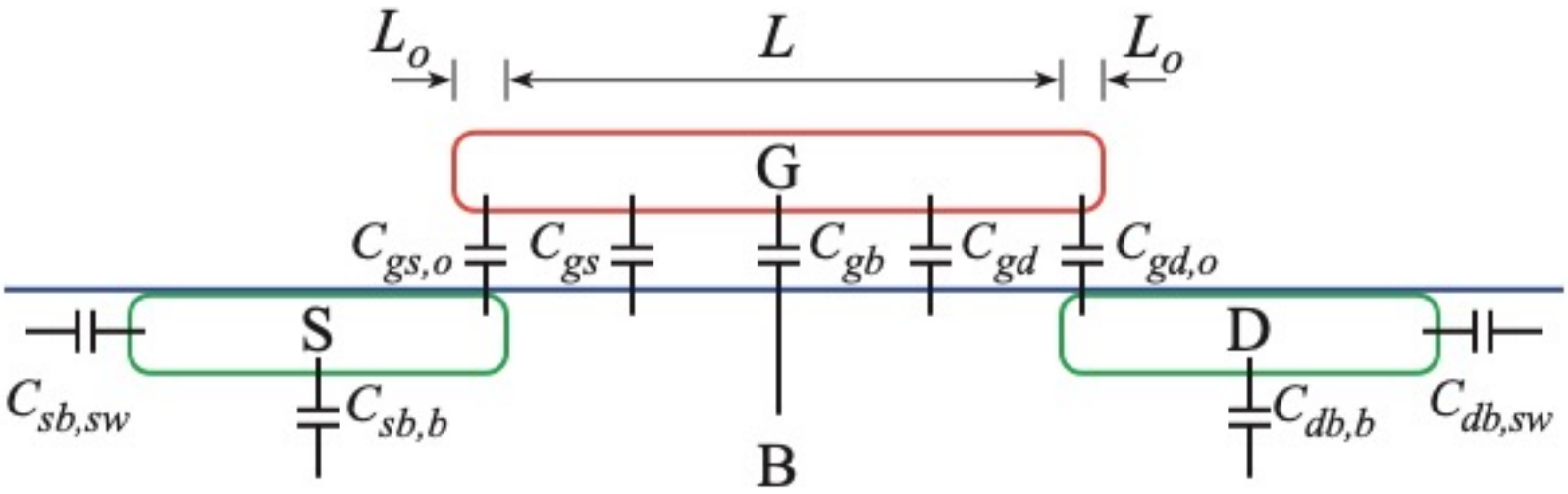
Capacitive Load



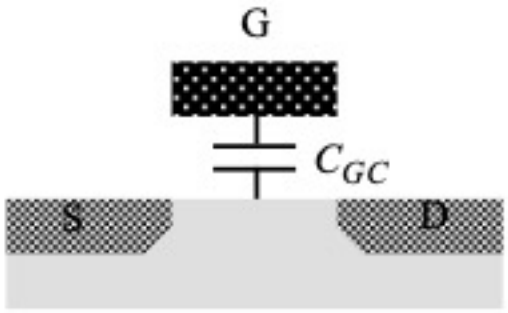
Simplified Model



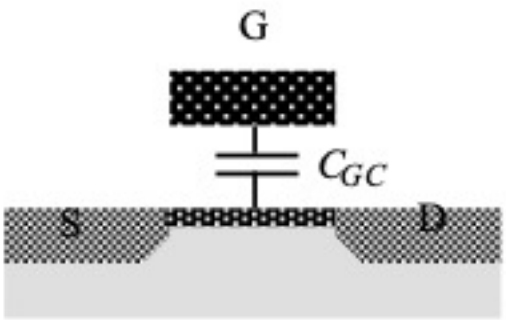
Parasitic MOSFET Capacitances



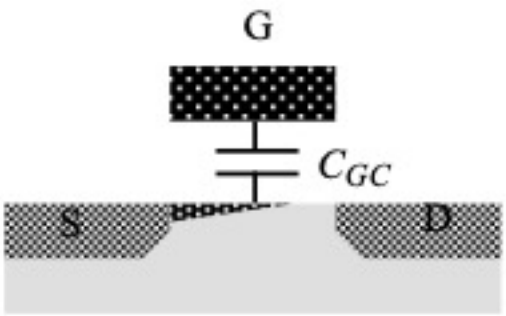
Gate Capacitance



Cut-off



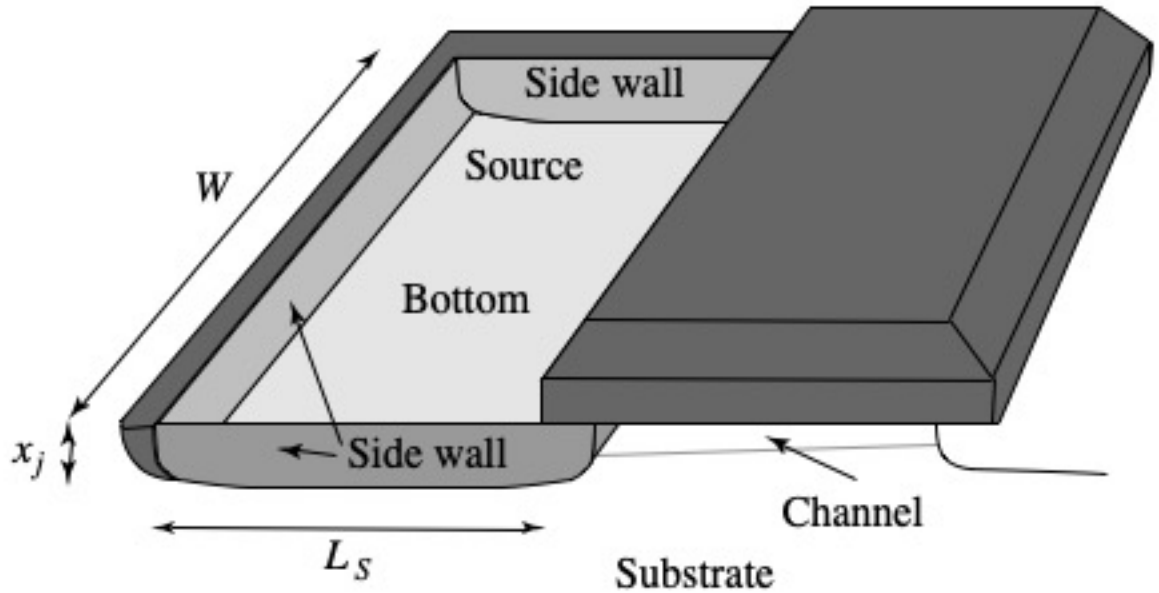
Resistive



Saturation

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

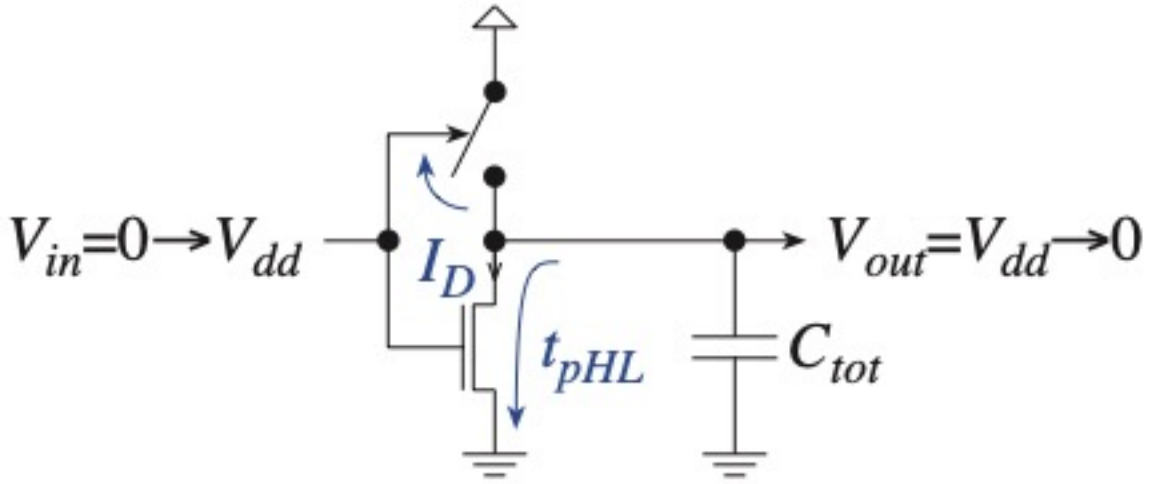
Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Propagation Delay



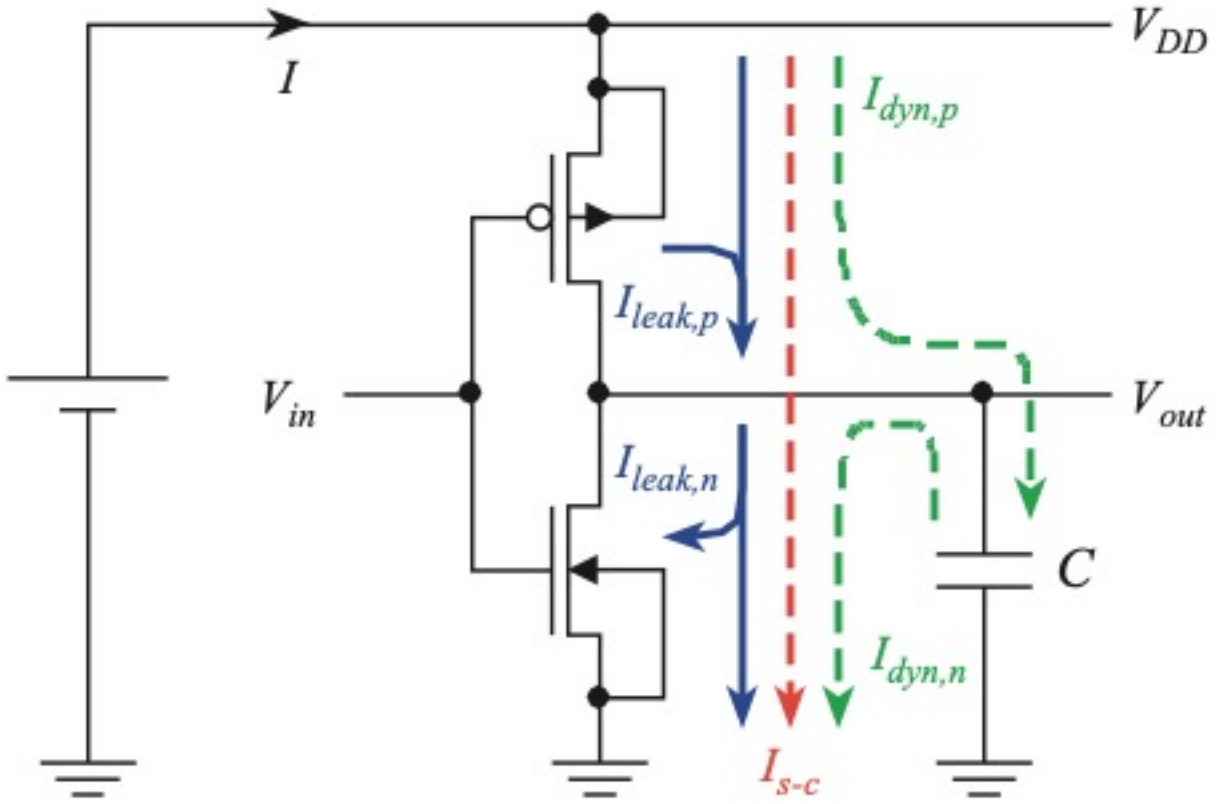
Method 1: estimate average R_{DS}

$$t_{pHL} \approx 0.69 R_{DS} C_{out} \approx 0.69 \frac{R_{DS}(V_{DD}) + R_{DS}(V_{DD}/2)}{2} C_{out}$$

Method 2: estimate average I_D

$$t_{pHL} \approx \Delta Q / I_D \approx \frac{C_{out} V_{DD} - C_{out} V_{DD}/2}{\left[I_D(V_{DD}) + I_D(V_{DD}/2)\right]/2}$$

Power Dissipation



Energy and Energy-Delay

Power-Delay Product (PDP) =

E = energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$