TSTE 86 Digital IC Lecture 3:

Interconnects

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Outline

- Introduction
- Wires
  - Capacitance, Resistance, Inductance
  - Wire Models
- Interconnect Impact
  - Capacitive Parasitics (Crosstalks)
  - Resistive Parasitics (Delay)
  - Inductive Parasitics (Noise)

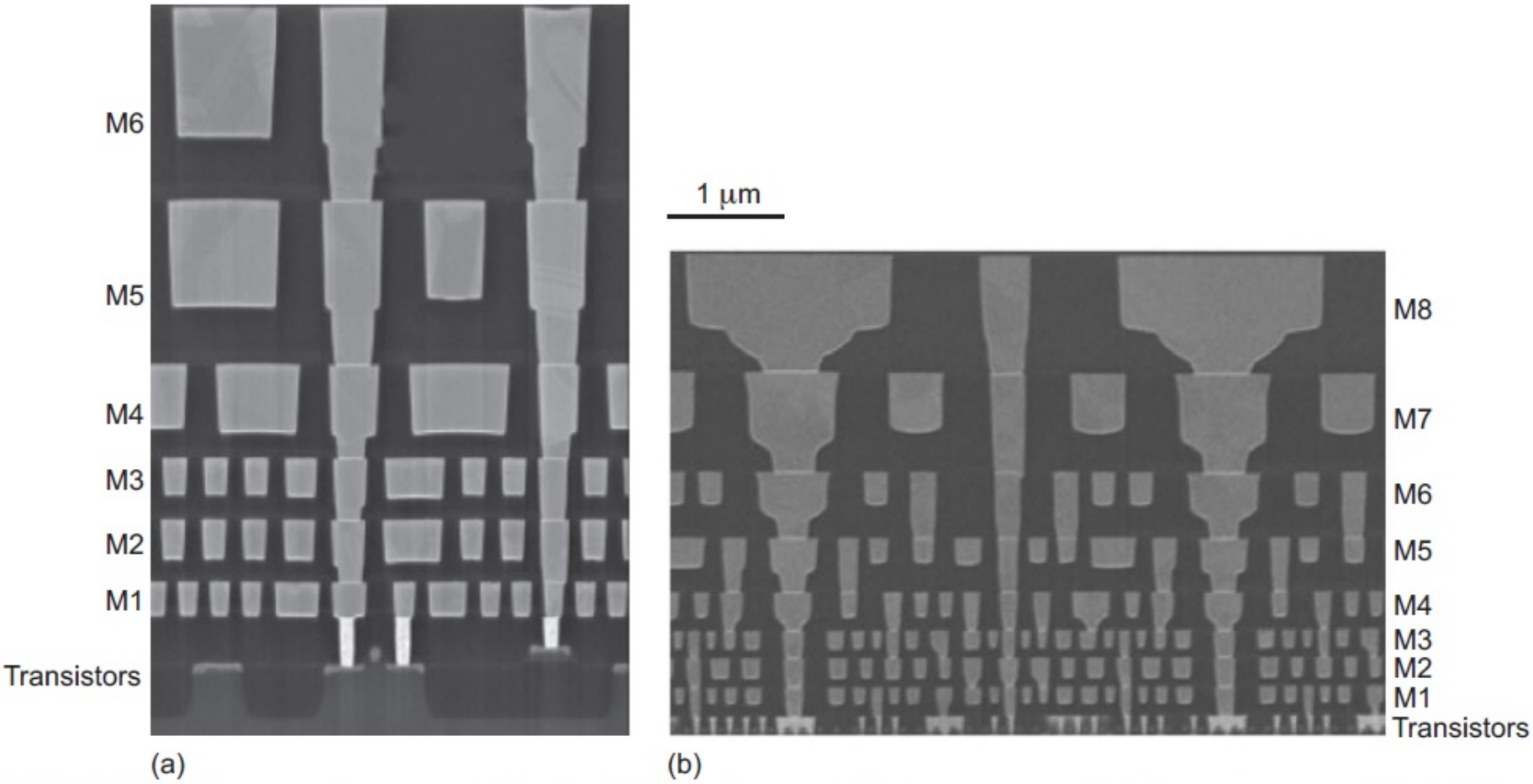
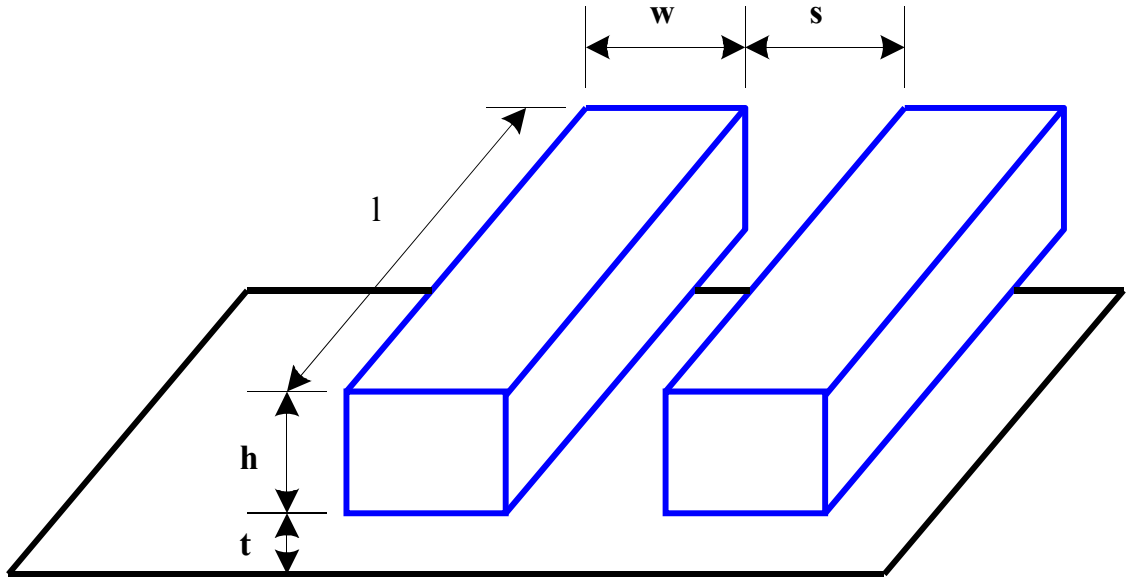


FIGURE 6.2 SEM image of wire cross-sections in Intel's (a) 90 nm and (b) 45 nm processes ((a) From [Thompson02] © 2002 IEEE. (b) From [Moon08] with permission of Intel Corporation.)

Wire Geometry

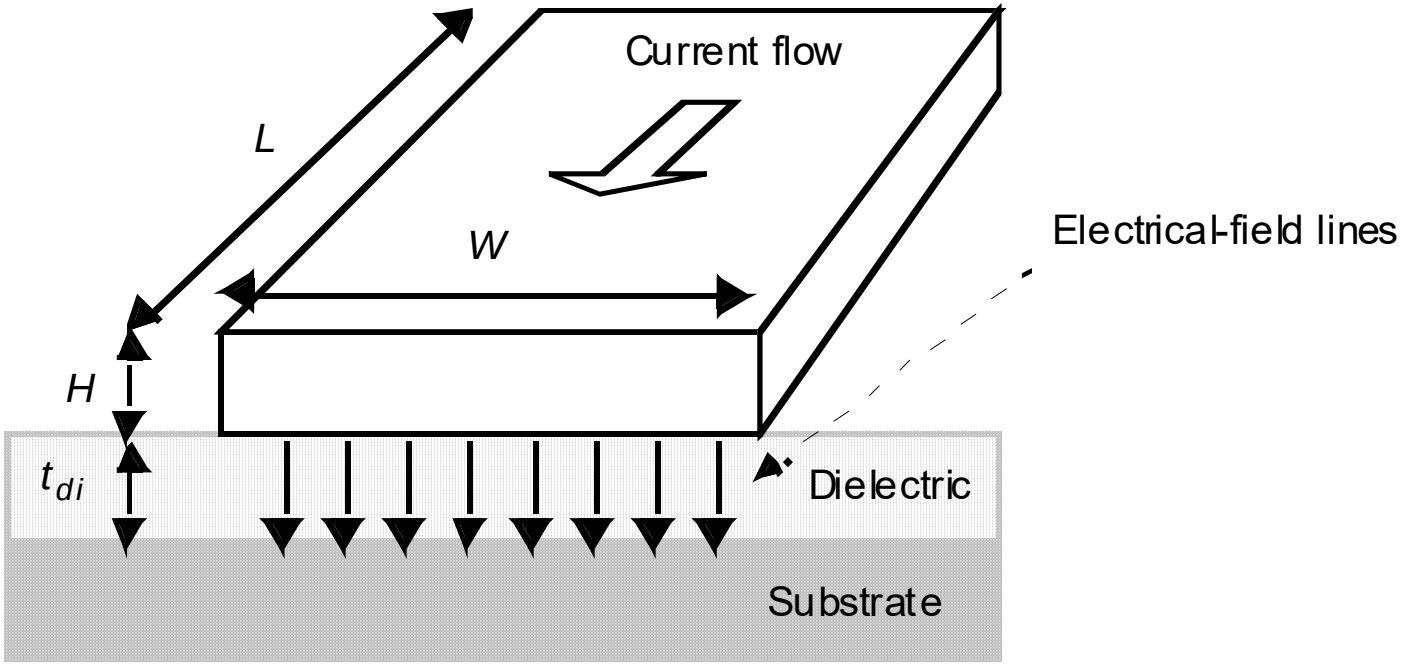


Wire Materials

- *Aluminum* until 180 nm technology
- *Copper* at current technology

Metal	Bulk resistivity (μΩ*cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Molybdenum (Mo)	5.3

Parallel Plate Capacitance

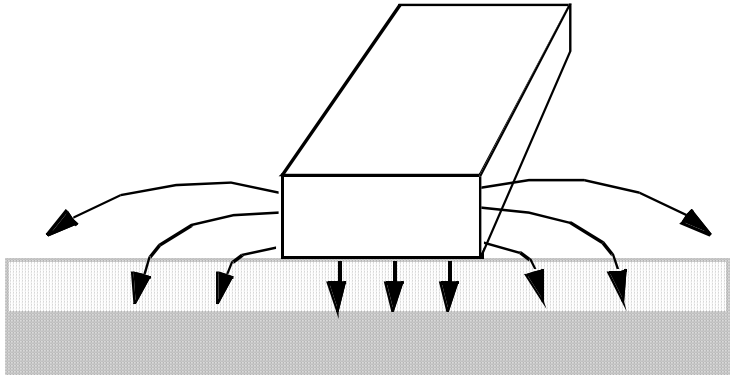


$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

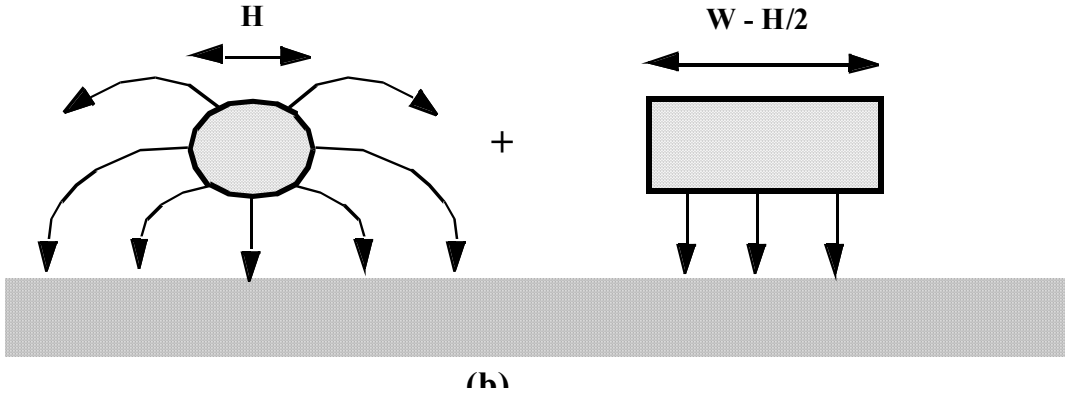
Permittivity

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringe Capacitance



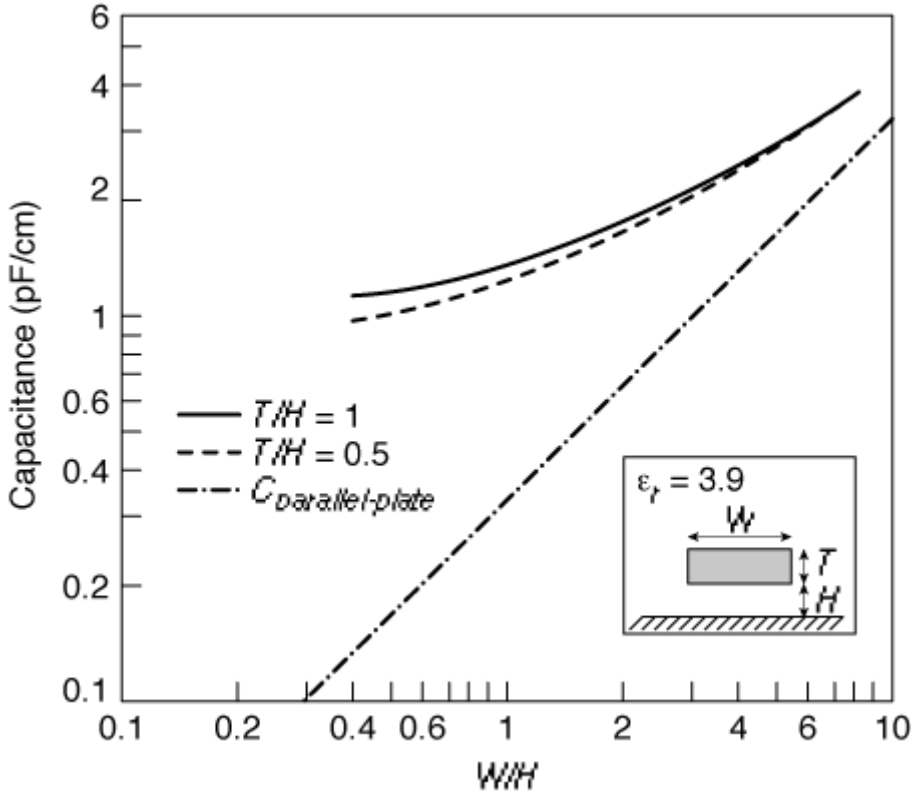
(a)



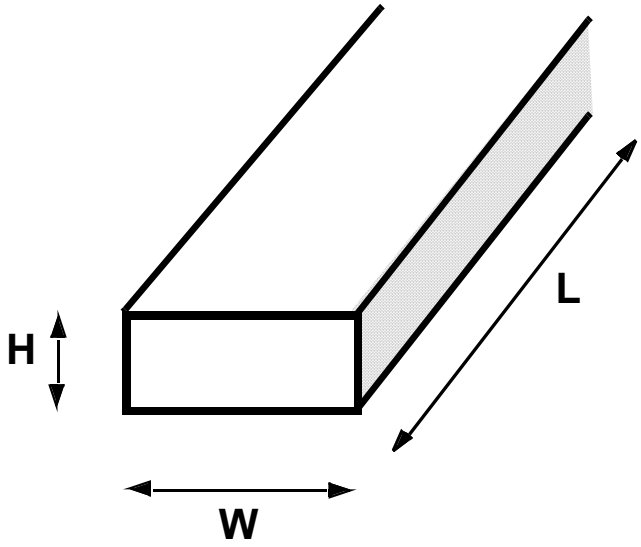
(b)

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

Fringe *vs.* Plate Capacitances



Wire Resistance

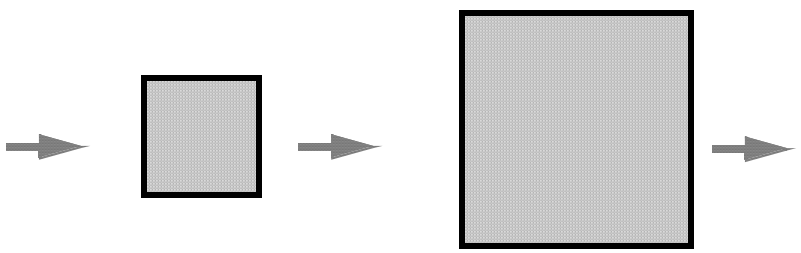


$$R = \rho \frac{L}{H W}$$

Sheet Resistance

R_o

$R_1 \equiv R_2$



0.25um technology, Al: 0.05-0.1 Ω/sq, Poly: 150-200 Ω/sq
n/p well: 1000-1500 Ω/sq, n+/p+: 50-150 Ω/sq

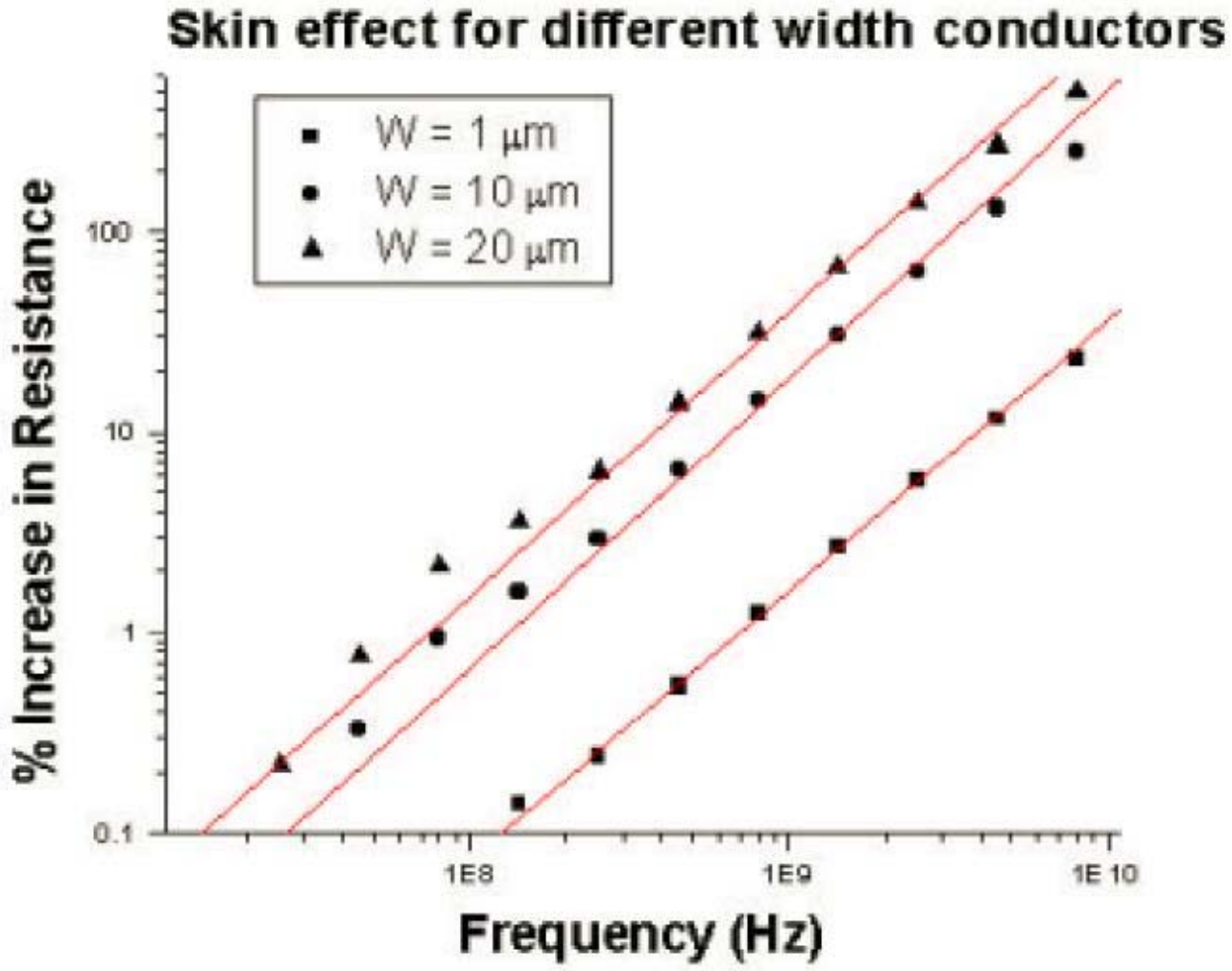
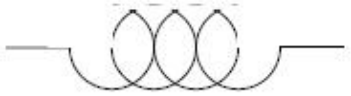


Figure 4.10 Skin-effect induced increase in resistance as a function of frequency and wire width. All simulations were performed for a wire thickness of 0.7 μm [Sylvester97].

Wire Inductance

Any wire has inductance

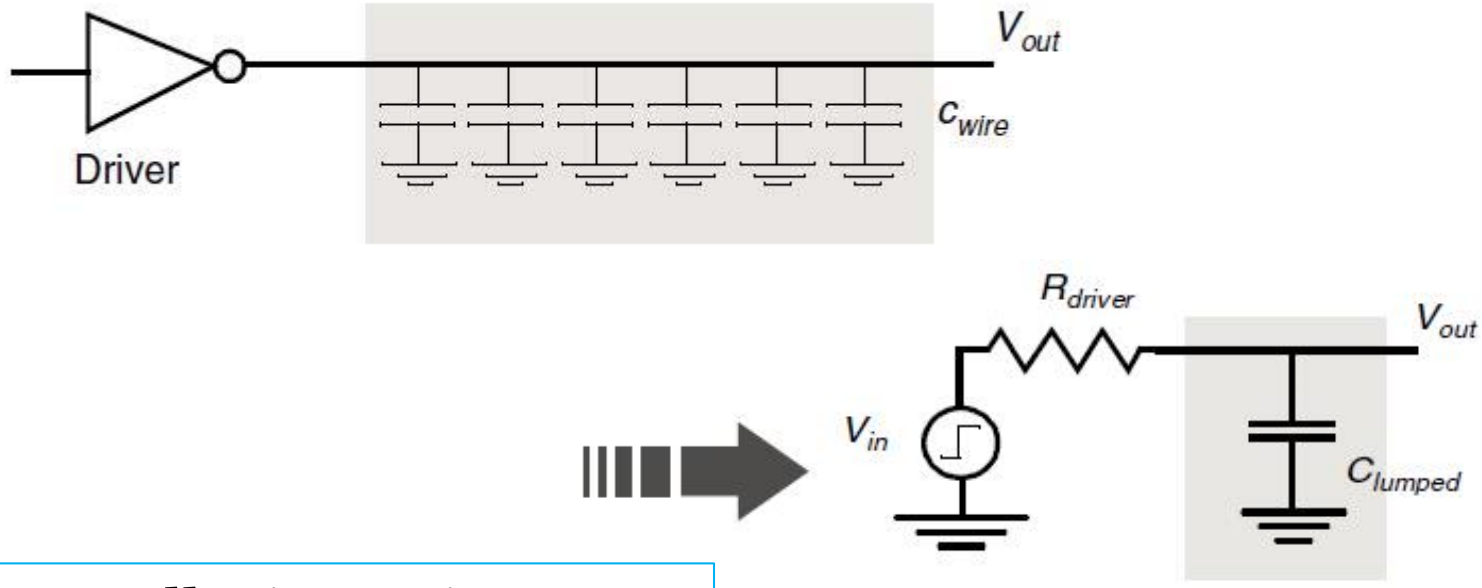


$$v = L\frac{di}{dt}$$

$$cl = \varepsilon\mu$$

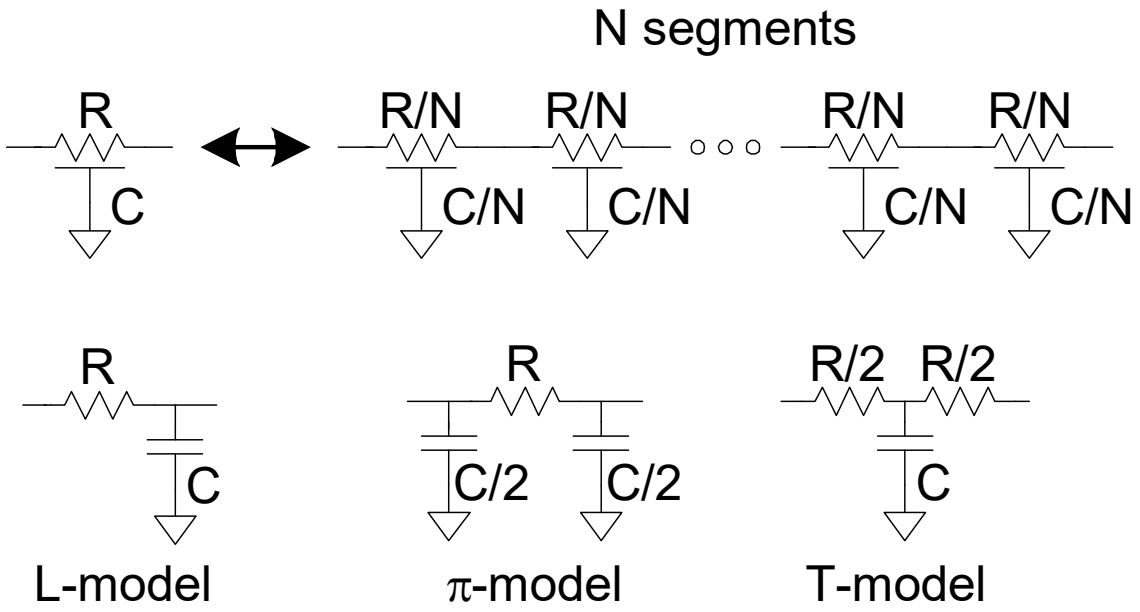
c: capacitance per unit
l: inductance per unit
ε: permittivity
μ: permeability ~1

The Lumped Model



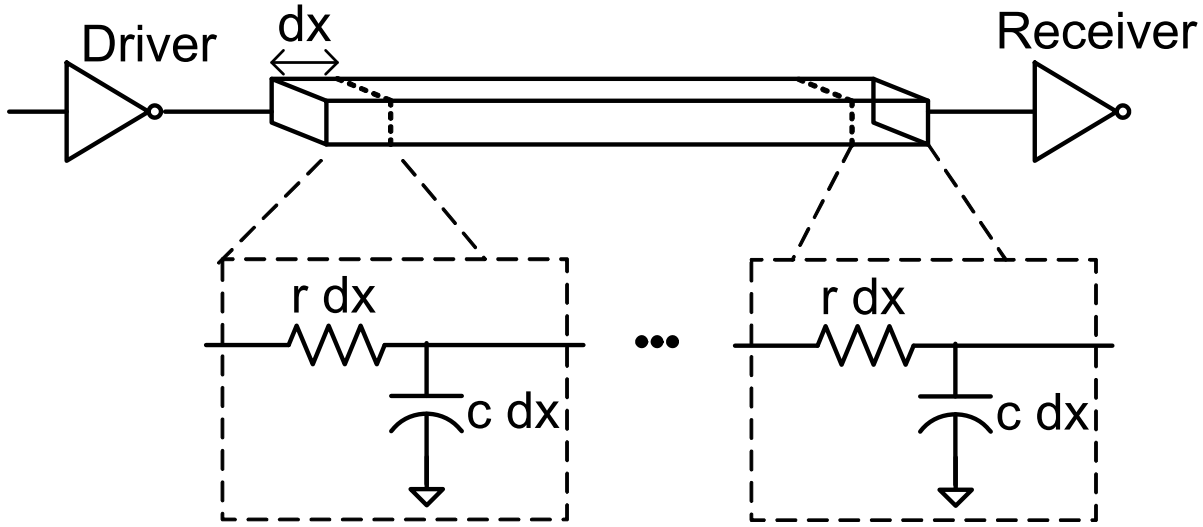
Small wire resistance
Low switching frequency

Comparison of Lumped *RC* Models



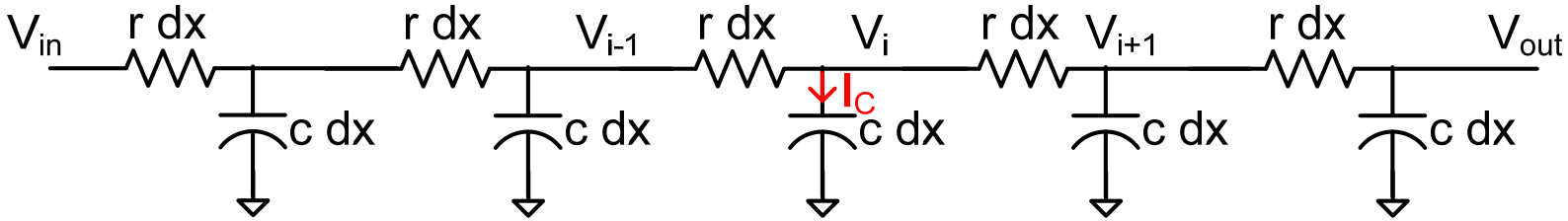
3-segment π-model is as accurate as 100-segment L-model

The Distributed *rc* Line



1. Break the wire into segments
2. Each segments has resistance and capacitance

The Distributed *rc* Line



$$I_C = c\Delta L\frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2}rc}$$

Elmore Delay

- Originally published [Elmore, J. Appl. Phys. 1948]
- Easier to compute analytically in most cases
- Verified by other researchers

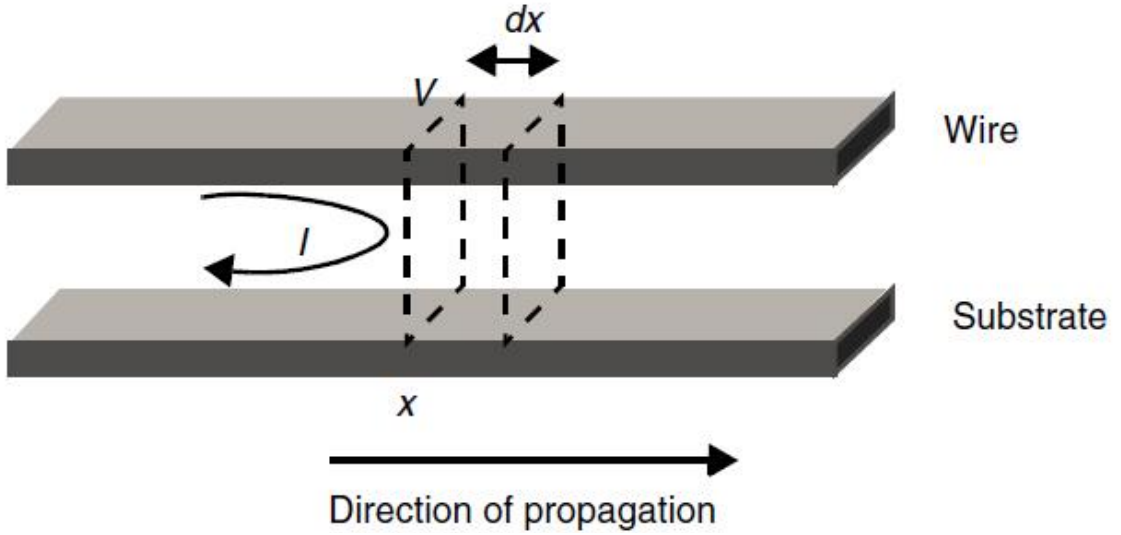
$$\tau_{DN} = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{i=1}^{N} C_i R_{ii}$$

Comparison of *RC* Models

Table 4.7 Step response of lumped and distributed *RC* networks—points of Interest.

Voltage range	Lumped *RC* network	Distributed *RC* network
$0 \rightarrow 50\%$ (t_p)	0.69 *RC*	0.38 *RC*
$0 \rightarrow 63\%$ (τ)	*RC*	0.5 *RC*
$10\% \rightarrow 90\%$ (t_r)	2.2 *RC*	0.9 *RC*
$0\% \rightarrow 90\%$	2.3 *RC*	1.0 *RC*

The Transmission Line



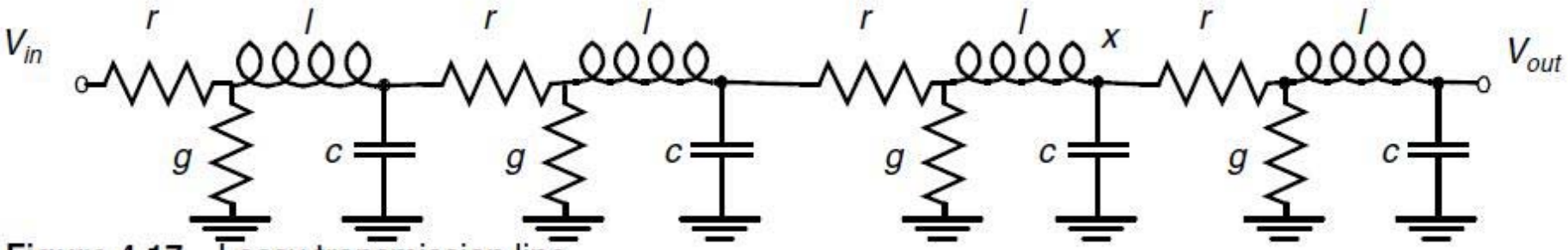


Figure 4.17 Lossy transmission line.

Transmission Line Terminations

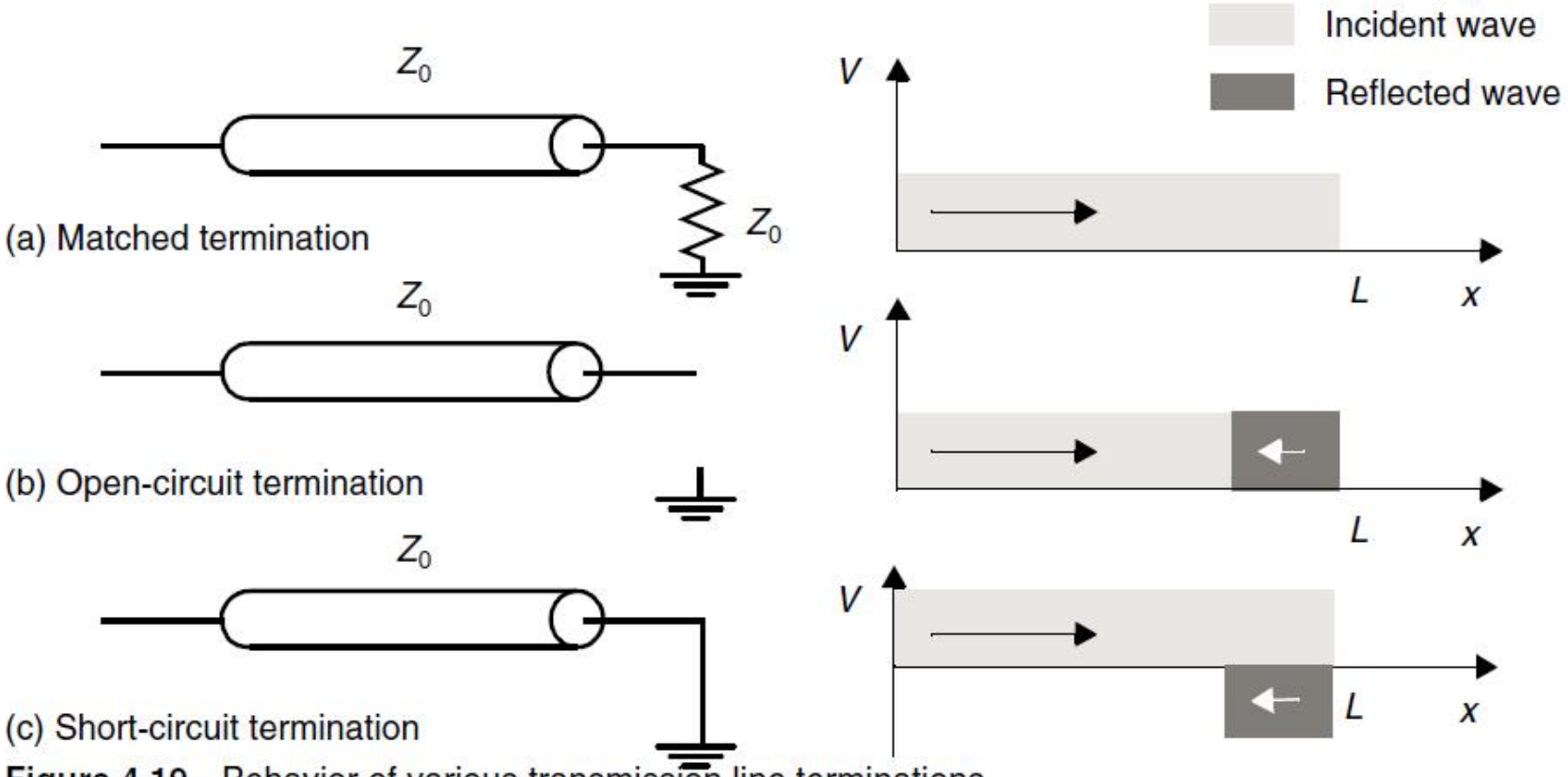


Figure 4.19 Behavior of various transmission line terminations.

When to use Transmission Line Model?

- When $t_{r/f} << 2.5\ t_{flight}$
- When $R_{line} < 5Z_0$
- Consider lossless when $R_{line} < Z_0/2$

$$\frac{t_r}{2.5}\frac{1}{\sqrt{lc}} < L < \frac{5}{r}\sqrt{\frac{l}{c}}$$

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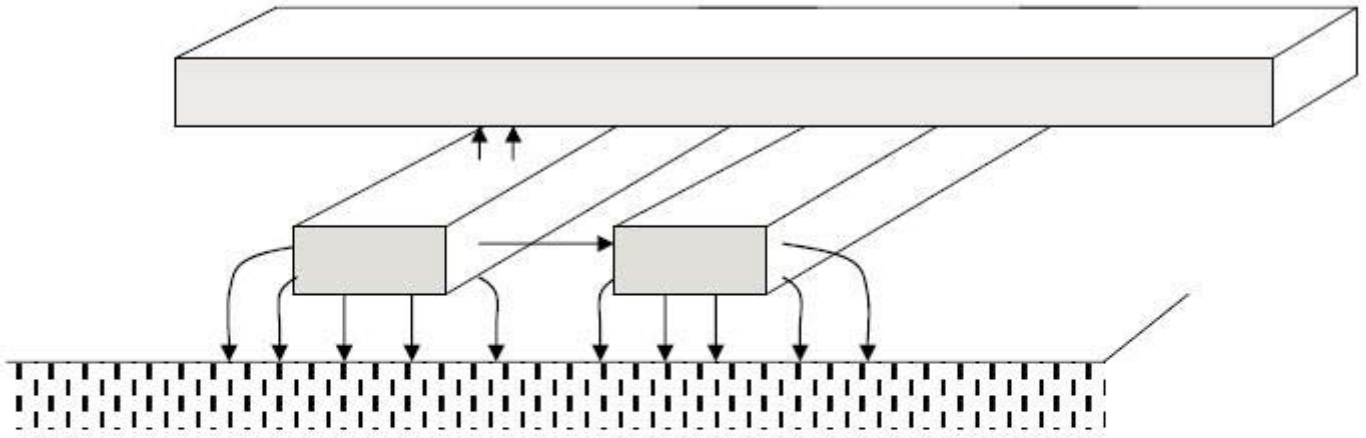
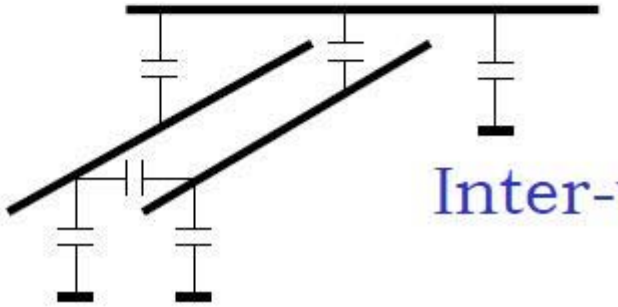
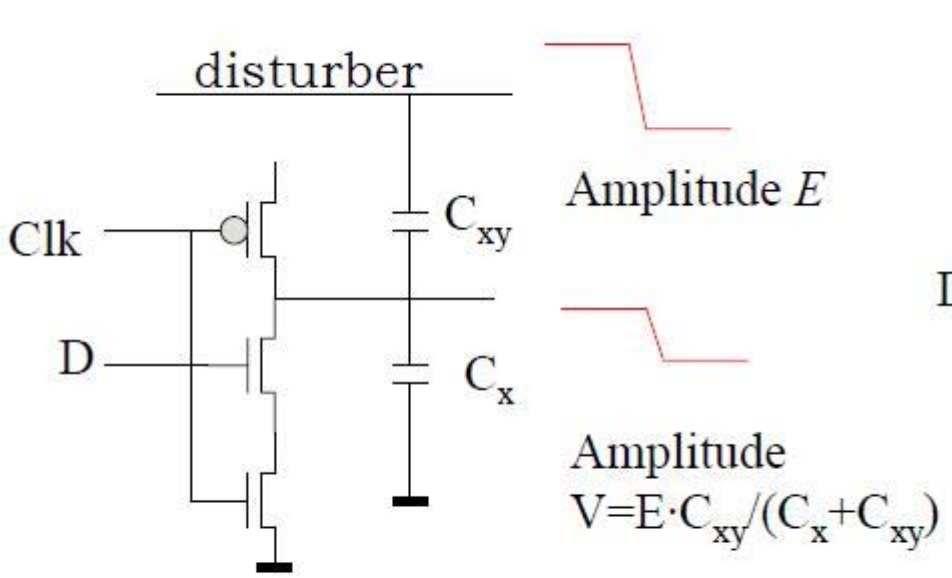
Capacitive Parasitics



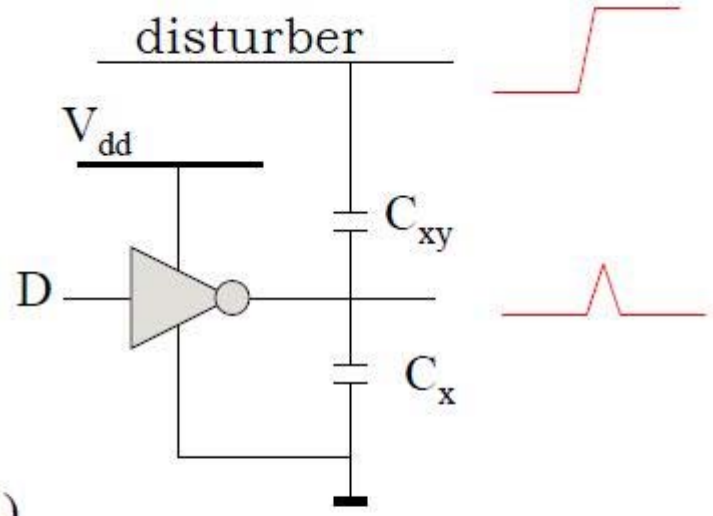


Inter-wire capacitance → *Crosstalk*

Crosstalk



Dynamic, sensitive
(floating output)

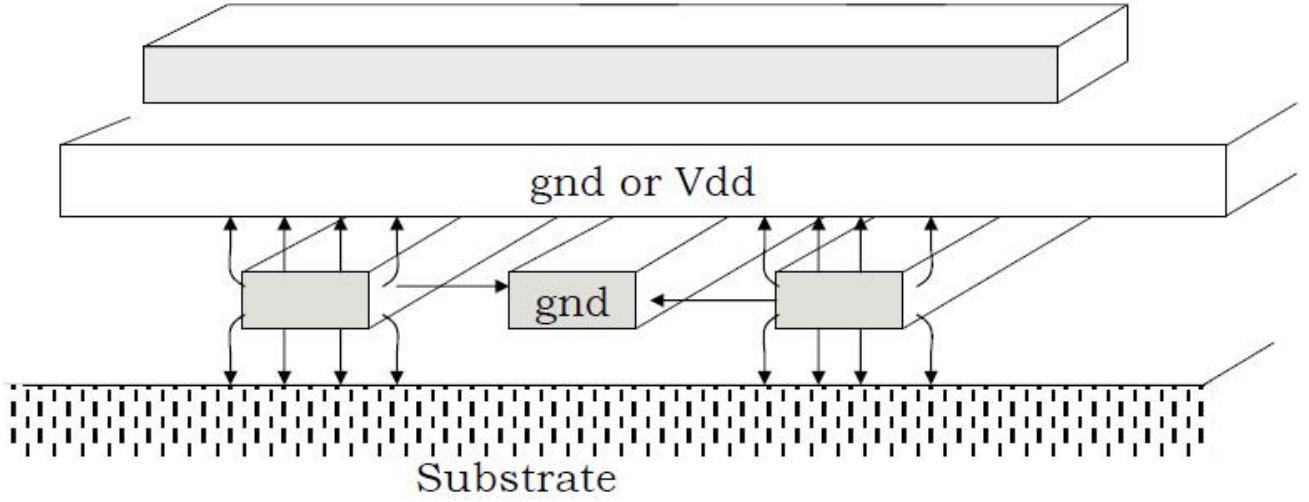


Static, less sensitive
(resistive path to Gnd/Vdd)

Difference between dyanmic and static!

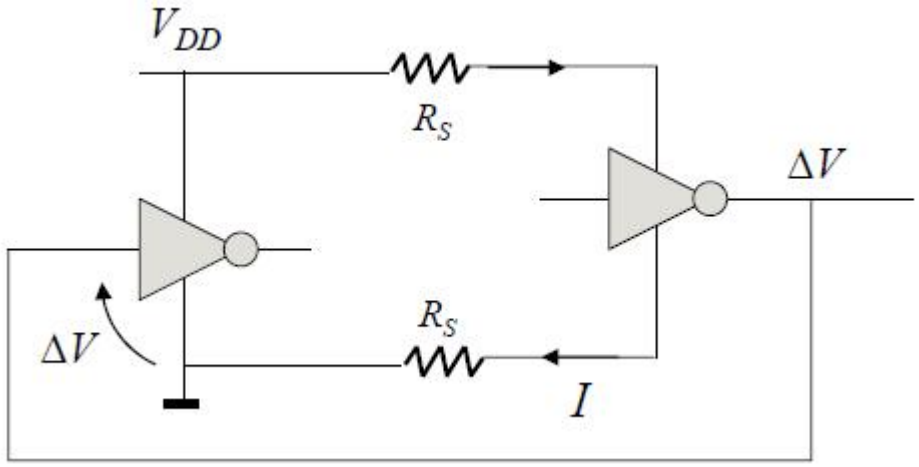
What to do with Crosstalk?

- Avoid floating nodes
- Avoid long parallel interconnects
- Shield wire to GND or V_{DD}



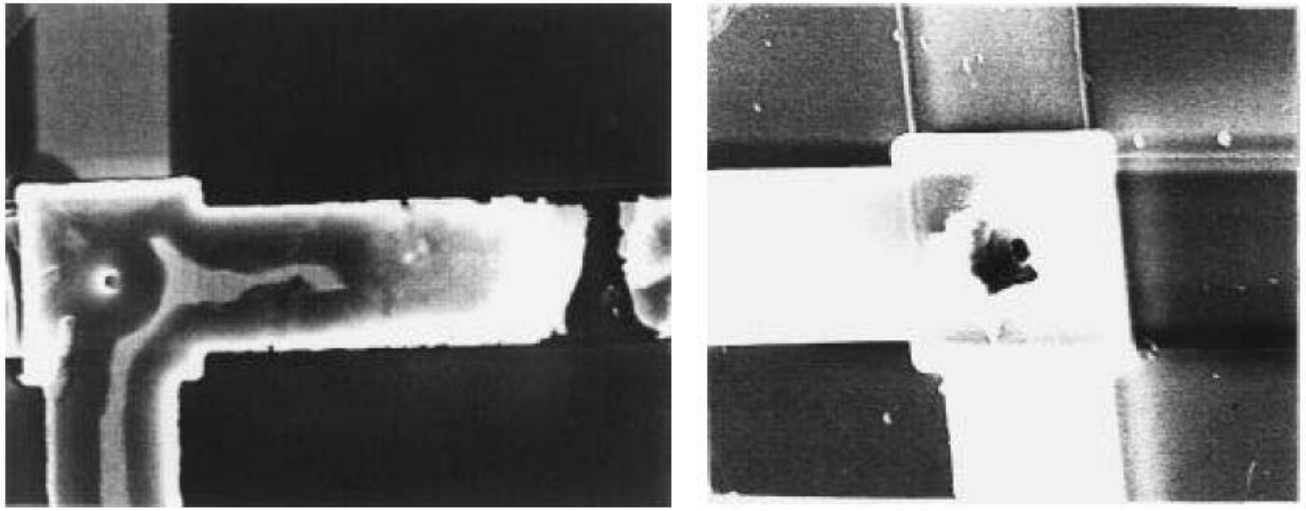
Resistive Parasitics

- Ohmic voltage drop
- Extra delays (RC delays)
- Reduced noise margin



Electromigration

- High current density gives heat and possible ion movement (for DC)
- Current density limited < 1 mA/μm², otherwise wire may become thinned with time leading to defects
- For copper electromigration less critical

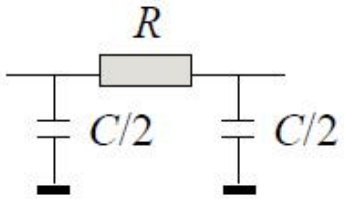


(a) Line-open failure. (b) Open failure in contact plug.

Figure 9.16 Electromigration-related failure modes (*Courtesy of N. Cheung and A. Tao, U.C. Berkeley*).

RC-Delays

1st order approximation:



Time constant: $RC/2$

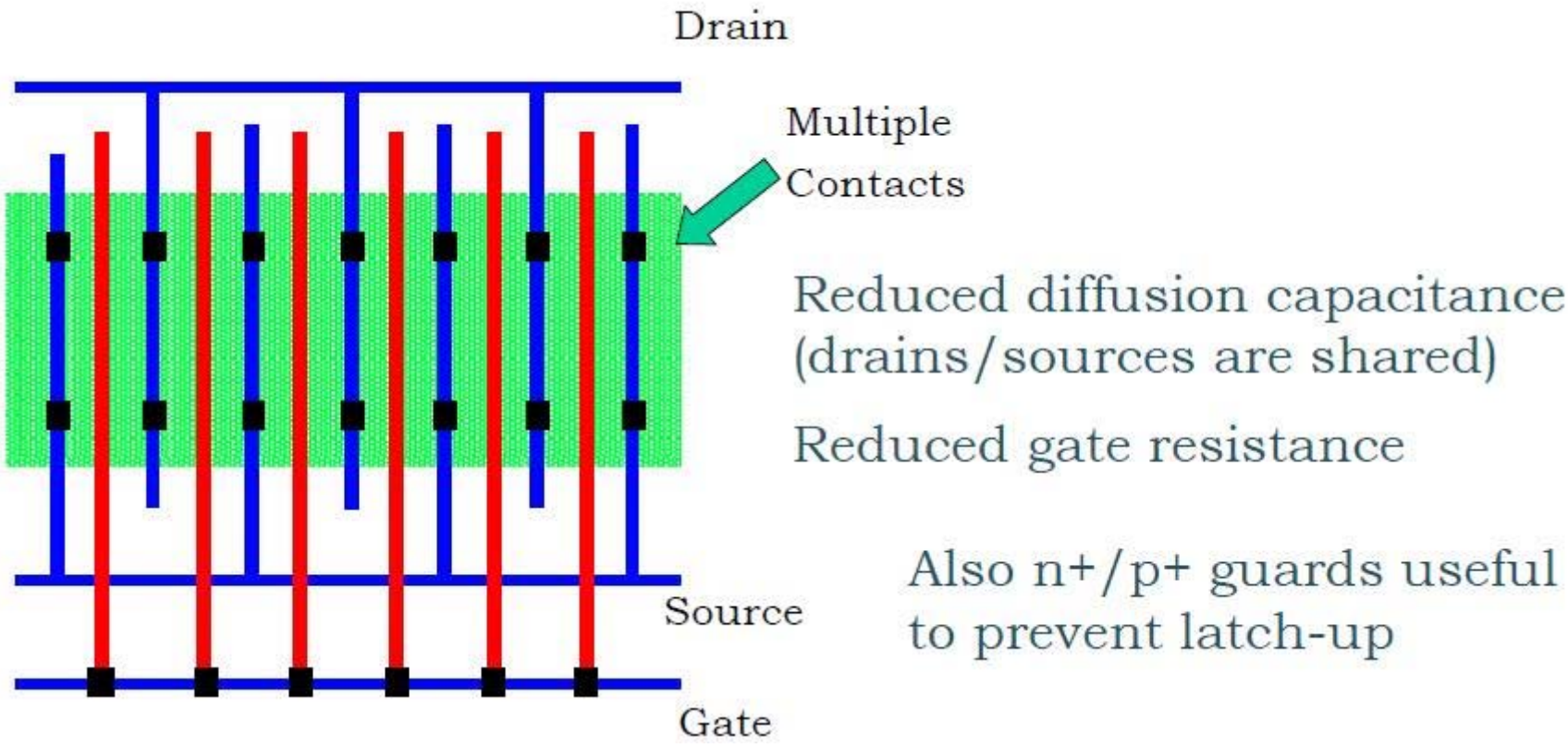
Delay (0-50%): $(RC/2)\ln 2 \approx 0.35RC$

Distributed model: $\text{Delay}_{50\%} = 0.38RC = 0.38R_lC_ll^2$

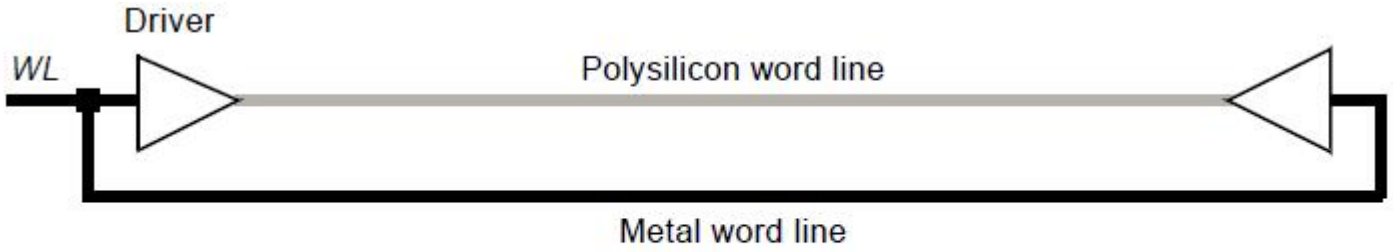
Delay proportional to l^2, quite serious for long wires
or for wires with large ρ (polysilicon)

Effect of geometry scaling: $R_lC_l=(\rho/wh)(\varepsilon w/t)= \rho\varepsilon/ht \sim 1/S^2$
If all geometry is reduced (by S), wire delay *increases* with $1/S^2$.
But usually h does not scale so delay increases with $1/S$.
At the same time a device delay *decreases*

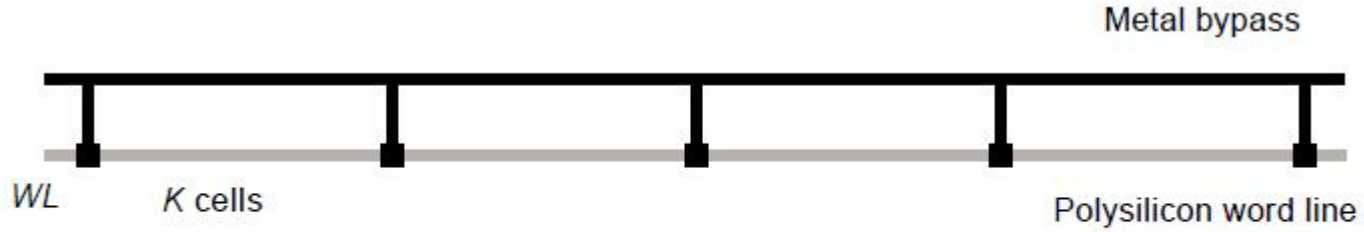
Large Transistors with ‘fingers’ in Parallel



Better Interconnect Materials



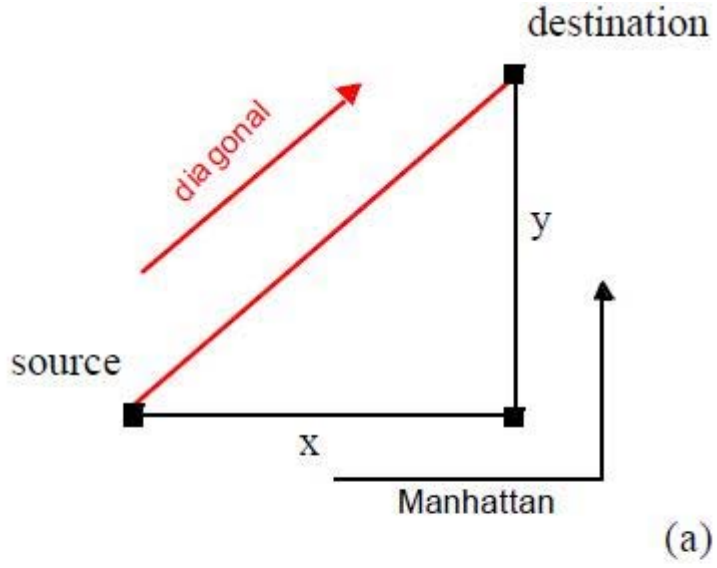
(a) Driving the word line from both sides



(b) Using a metal bypass

Figure 9.17 Approaches to reduce the word-line delay.

Better Interconnect Strategies



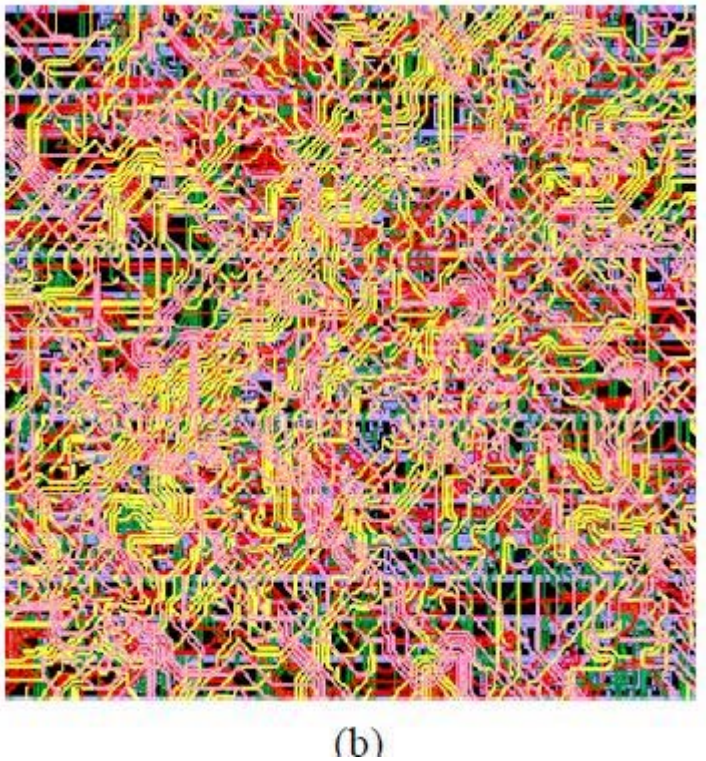
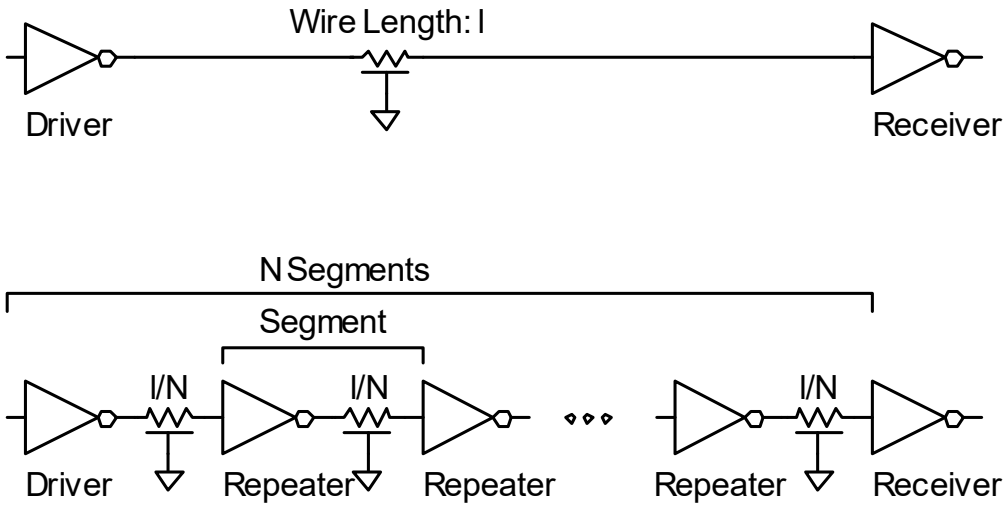


Figure 9.18 Manhattan versus diagonal routing. (a) Manhattan routing uses preferential routing along orthogonal axis, while diagonal routing allows for 45° lines. (b) example of layout using 45° lines.

20% wire length reduction!

Introducing Repeaters

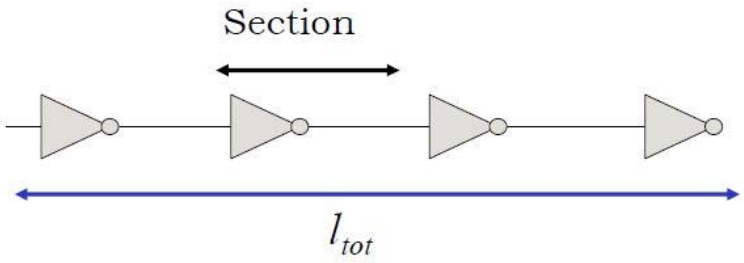
- RC delay proportional to l^2
- Break long wires into segments



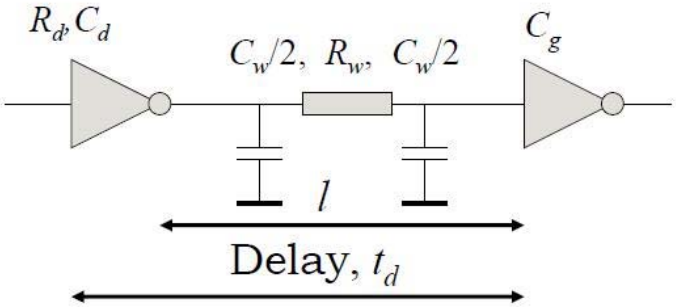
Repeat Design

- How many repeaters needed?
- How large repeaters needed?

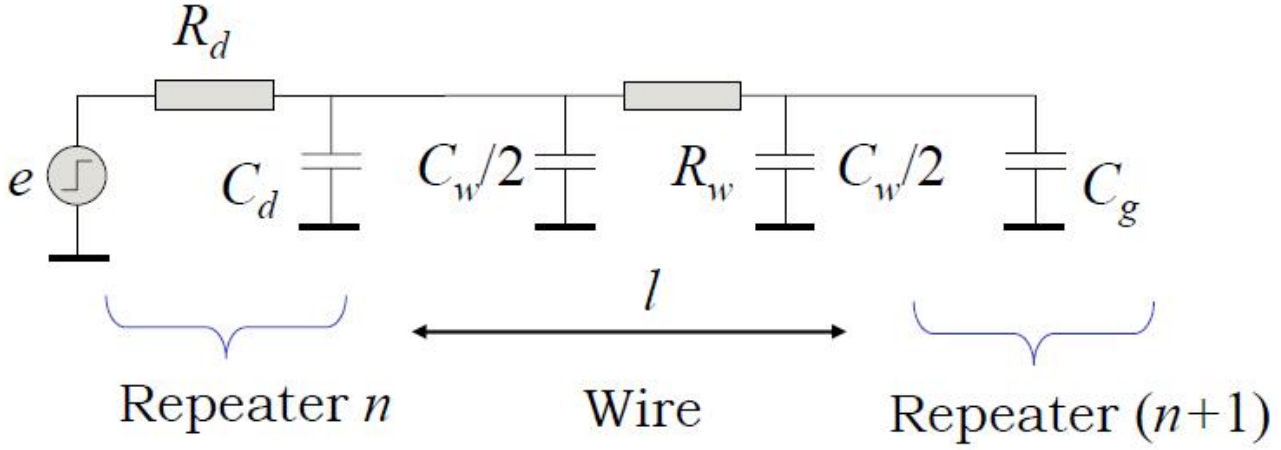
Wire Model:



One section:



Elmore Delay Model



Delay of one section (by Elmore model):

$$t_d = 0.69 \cdot [R_d(C_d + C_w/2) + (R_d + R_w) \cdot (C_w/2 + C_g)]$$
$$= 0.69 \cdot [R_d(C_d + C_g) + R_d C_w + R_w C_g + R_w C_w/2)]$$

$R_w = r_w l \qquad l = l_{tot}/N$ - wire length

$C_w = c_w l$

Optimum Number of Repeaters

$t_{d,tot} = N \cdot t_d$ total delay of the chain

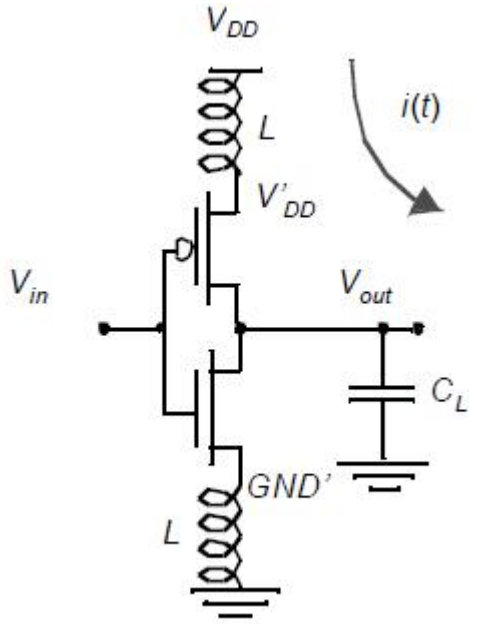
$dt_{d,tot}/dN = 0$ gives $\Rightarrow$ $N_{opt} = l_{tot}\sqrt{\frac{r_w c_w}{2R_d(C_d + C_g)}}$

$l_{opt} = l_{tot}/N_{opt}$ $\Rightarrow$ $l_{opt} = \sqrt{\frac{2R_d(C_d + C_g)}{r_w c_w}}$

Note: $R_d\,(C_d + C_g)$ represents a delay of one repeater, transistor widths can be optimized as well

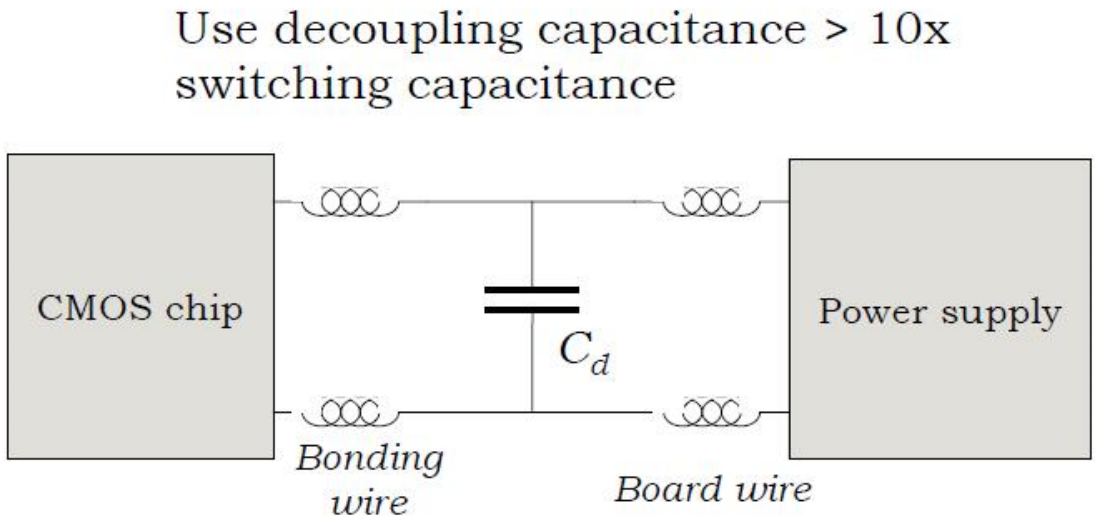
Inductive Parasitics

- Voltage Drop (Bonding Wires)
- Delay (Transmission Line)
- Resonating Noise (LC)



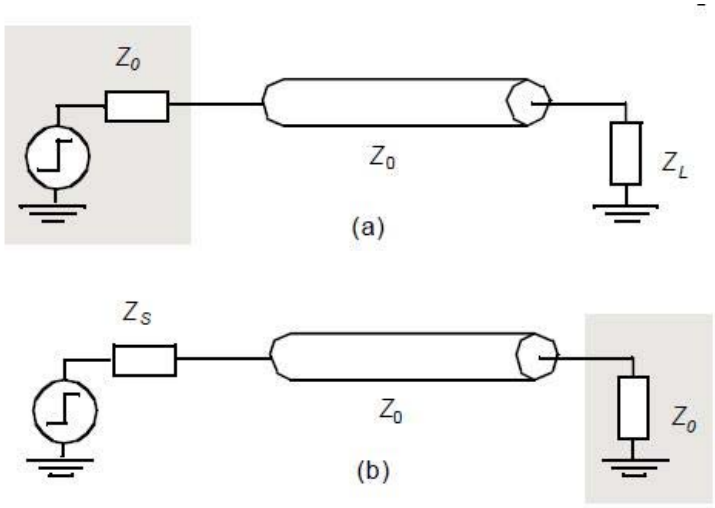
Address the *L(di/dt)* Voltage Drop

- Separate power pins for I/O pads and chip core
- Multiple power and ground pins
- Decoupling capacitance



Address the Transmission Line Effect

- Matched termination



- Shielding

Summary

- Capacitive parasitics cause delays, crosstalk and power consumption
- Resistive parasitics cause voltage loss and extra wire delay
- Inductive parasitics cause voltage loss and transmission line behavior of wires, critical at higher switching speed

Reference

- *Digital Integrated Circuits*, by Jan M. Rabaey, et al.
- *CMOS VLSI Design*, by David Harris, et al.

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