

Digital ICs — TSEI03 / TSTE86

Responsible

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Web

[www.isy.liu.se/edu/kurs/](http://www.isy.liu.se/edu/kurs/TSEI03)
[TSEI03](http://www.isy.liu.se/edu/kurs/TSEI03)
[TSTE86](http://www.isy.liu.se/edu/kurs/TSTE86)

Organization

	<i>TSEI03</i>	<i>TSTE86</i>
Lectures	7x2h	12x2h
Exercises	7x2h	12x2h
Lab work	3x4h	3x4h

Digital ICs — TSEI03 / TSTE86

Material

- Main text book is *Digital Integrated Circuits, 2nd ed.*, by J.M. Rabaey, A. Chandrakasan, and B. Nikolić
- A collection of problems and solutions is sold by *Bokab* located in Kårallen
- Laboratory material is distributed on the web

Grading

	TSEI03	TSTE86
• Written examination	2.5 hp	4.5 hp
• Laboratory work	1.5 hp	1.5 hp

Digital ICs — Staff 2019

Lecturers

Mark Vesterbacka

Deyu Tu



Teaching assistants

Mikael Henriksson (*TSEI03*)

Deyu Tu (*TSTE86*)

Lab assistants

Julia Doñoro Martín

Mohamad Khaddour Basmaji

Samir Sabah

Digital ICs — Lectures

1) Introduction [Ch. 1]	TSEI03/TSTE86
2) Devices [Ch. 3, 4]	TSEI03/TSTE86
3) Interconnect [Ch. 4, 9]	TSTE86
4) Circuits [Ch. 5]	TSEI03/TSTE86
5) Combinational logic [Ch. 6]	TSEI03/TSTE86
6) Sequential circuits [Ch. 7]	TSEI03/TSTE86
7) Synchronization [Ch. 10]	TSTE86
8) Adders [Ch. 11]	TSEI03/TSTE86
9) Multipliers [Ch. 11]	TSTE86
10) Memory [Ch. 12]	TSEI03/TSTE86
11) Manufacturing [Ch. 2]	TSTE86
12) System design [Ch. 8]	TSTE86

Labs

Content

- 1) Measurement
- 2) Layout
- 3) Adder

Collaboration

Students work together in pairs

Sign-up

Sign up for one of each lab on LiU's e-learning platform lisam.liu.se (course registration required)



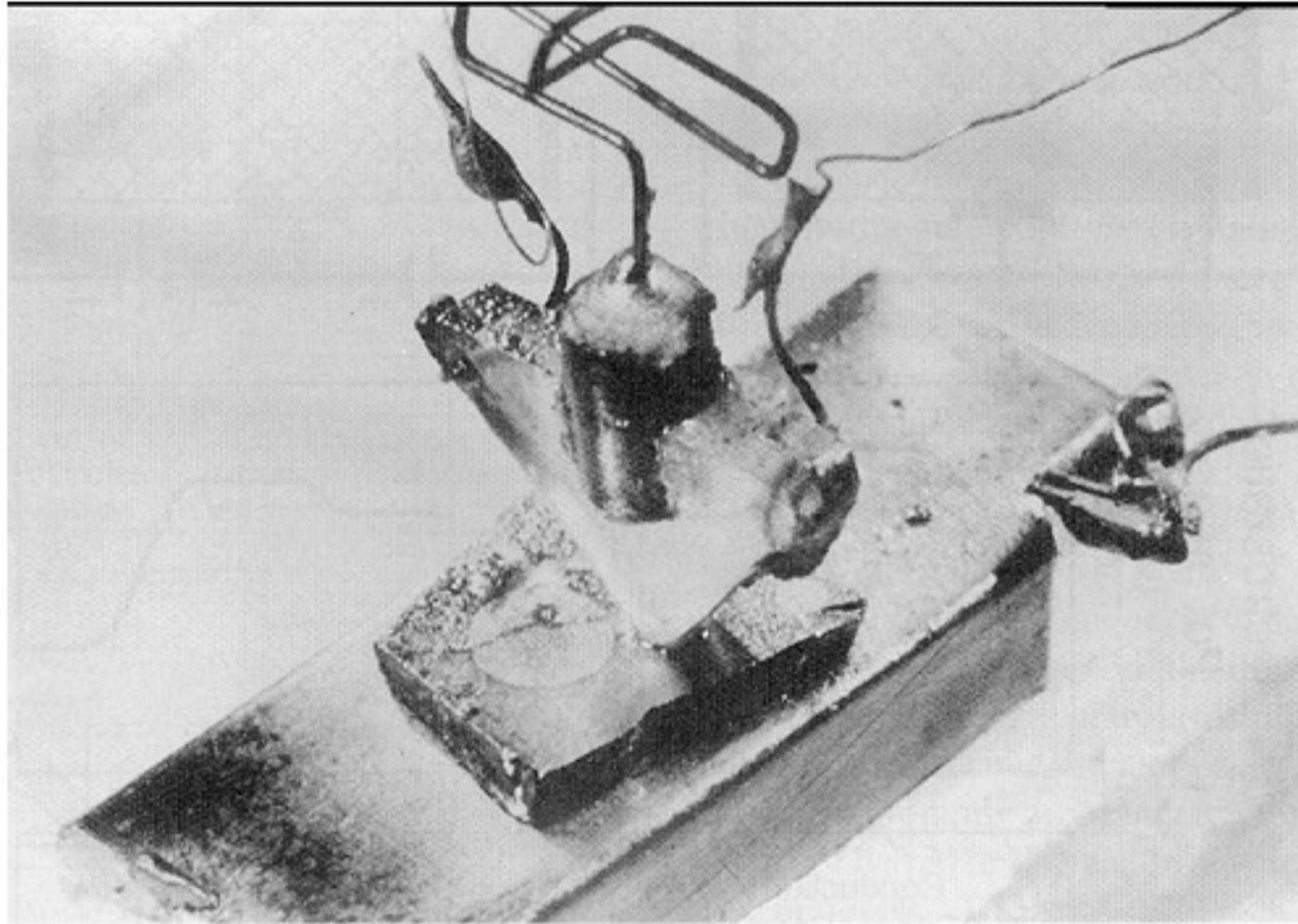
Adapted from

Digital Integrated Circuits A Design Perspective

Jan M. Rabaey
Anantha
Chandrakasan
Borivoje Nikolić

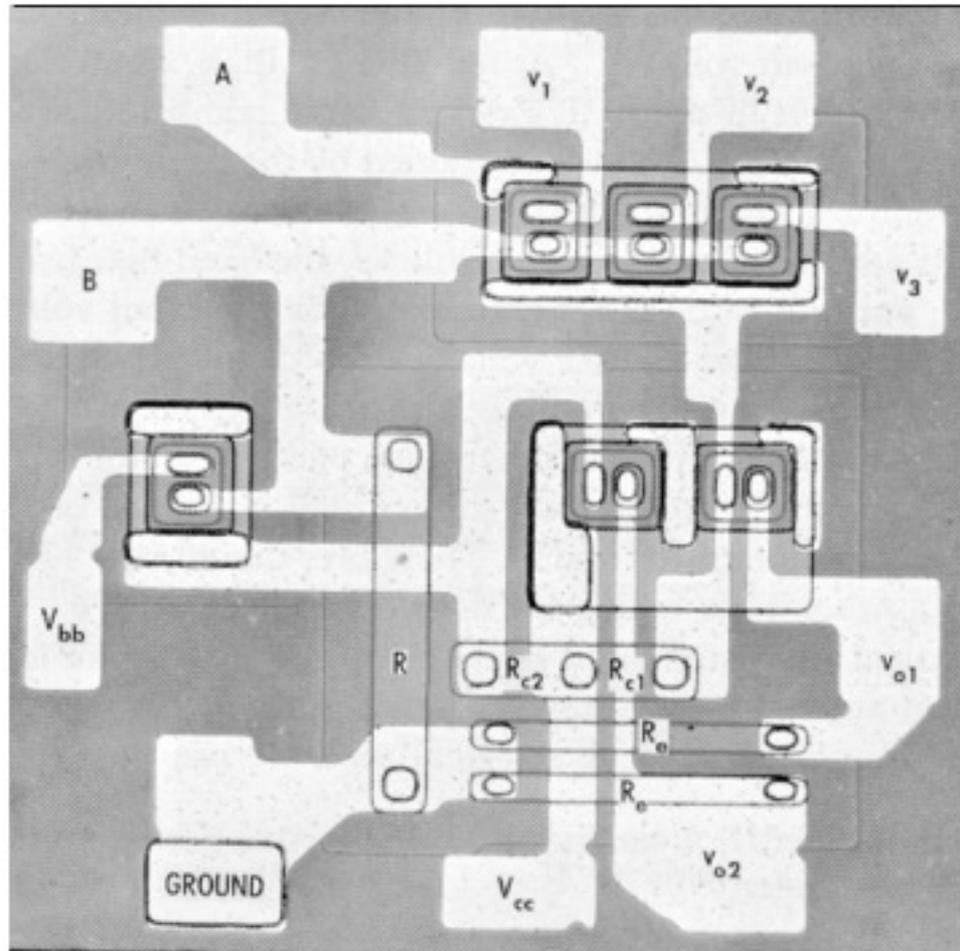
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Transistor Revolution



First transistor
Bell Labs, 1948

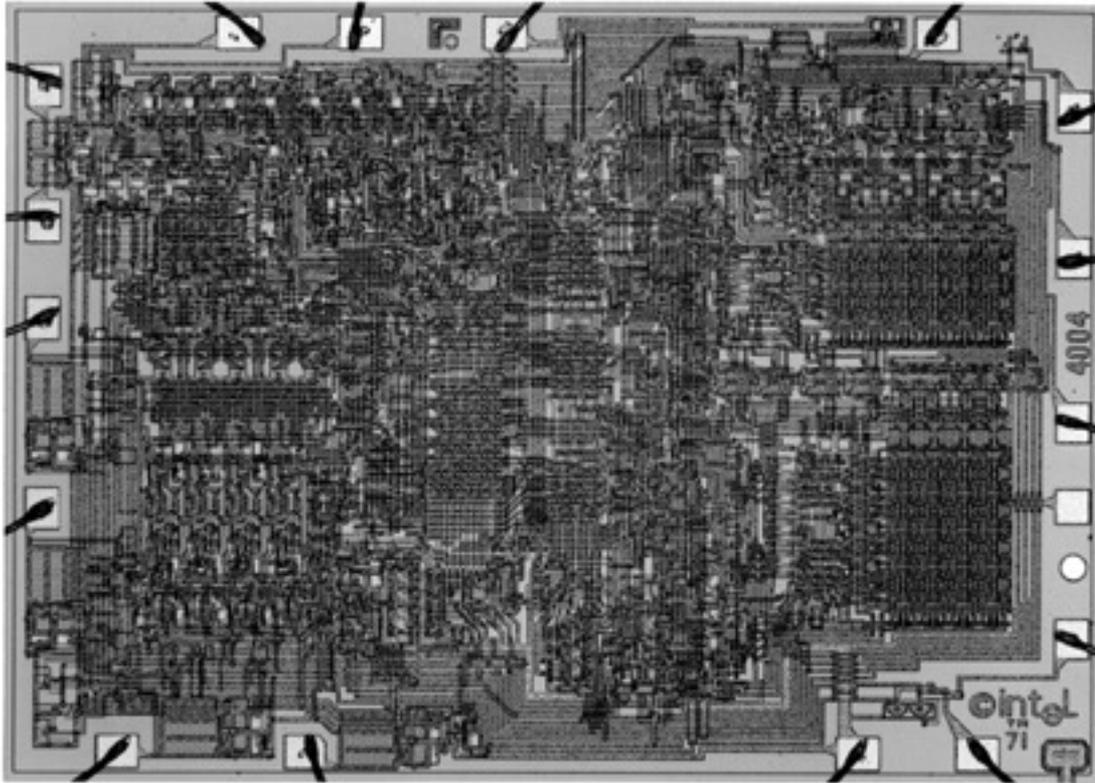
First Integrated Circuits



Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

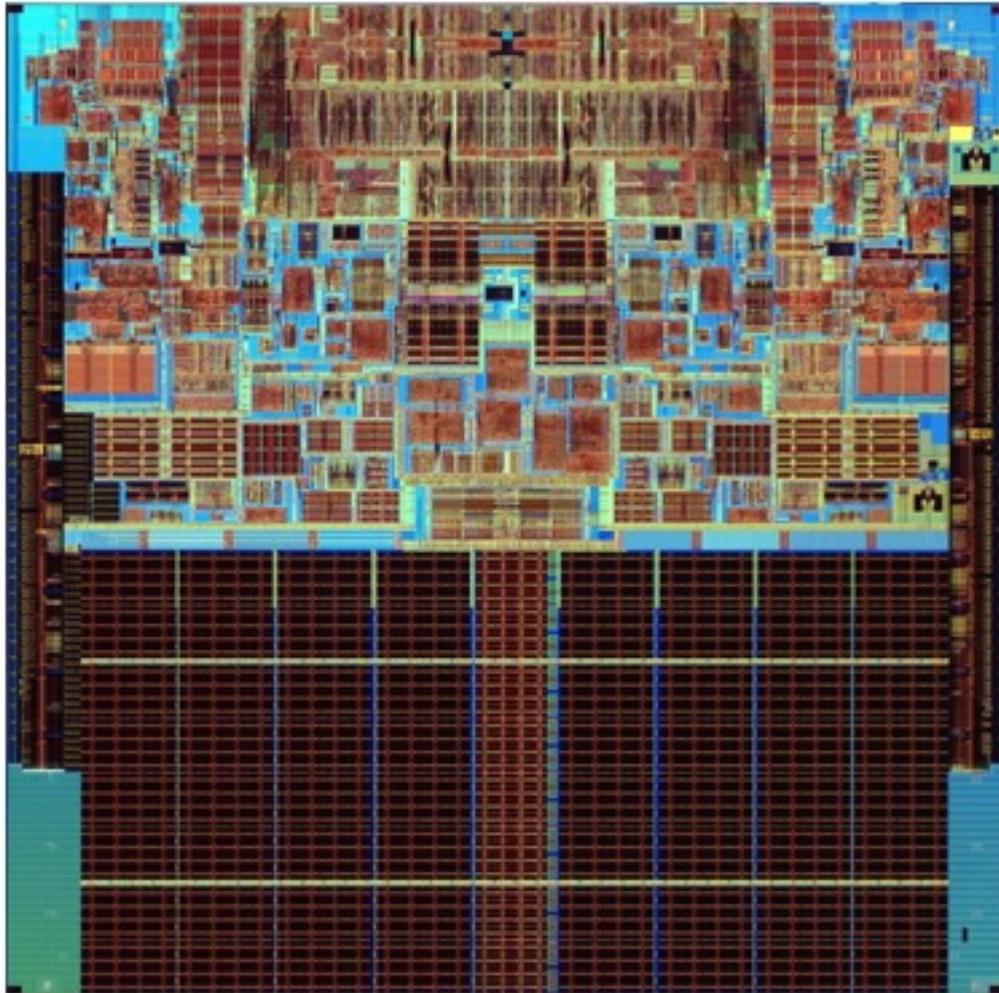
Intel 4004 Microprocessor



1971

- 10 μm feature size
- $\sim 2\text{ k}$ transistors
- $\sim 1\text{ MHz}$ operation

Intel Core 2 Microprocessor



2006

65 nm features

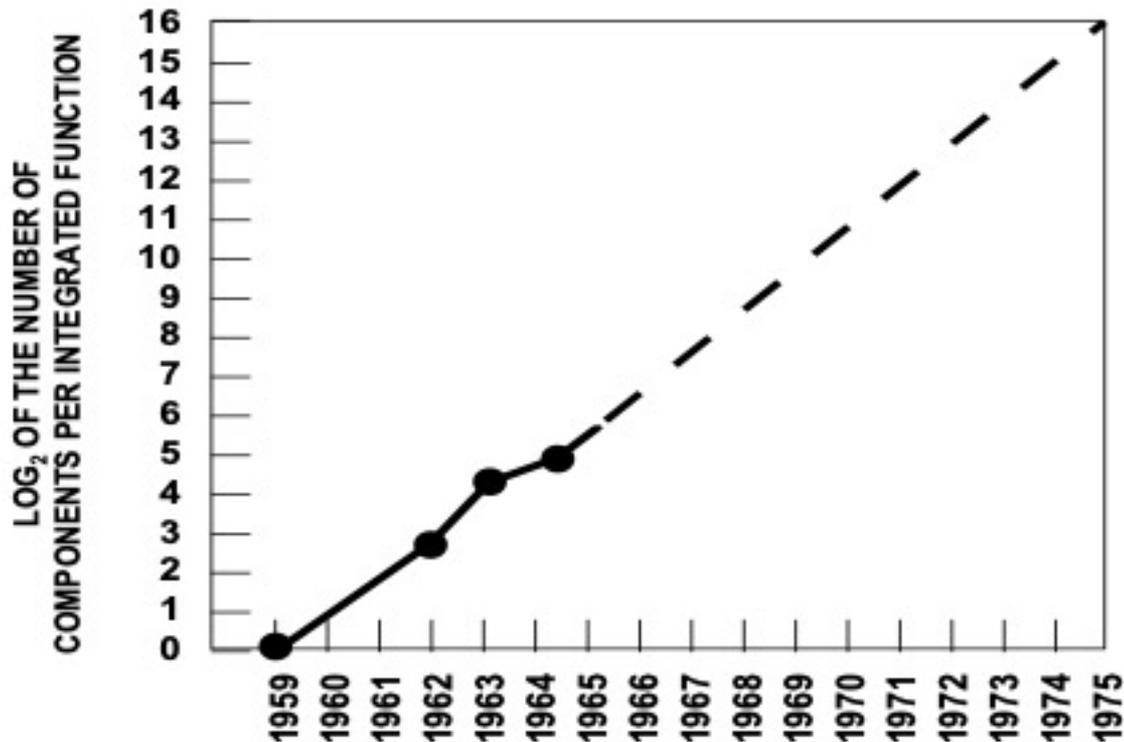
~ 300 000 k transistors

~ 3 000 MHz operation

Moore's Law

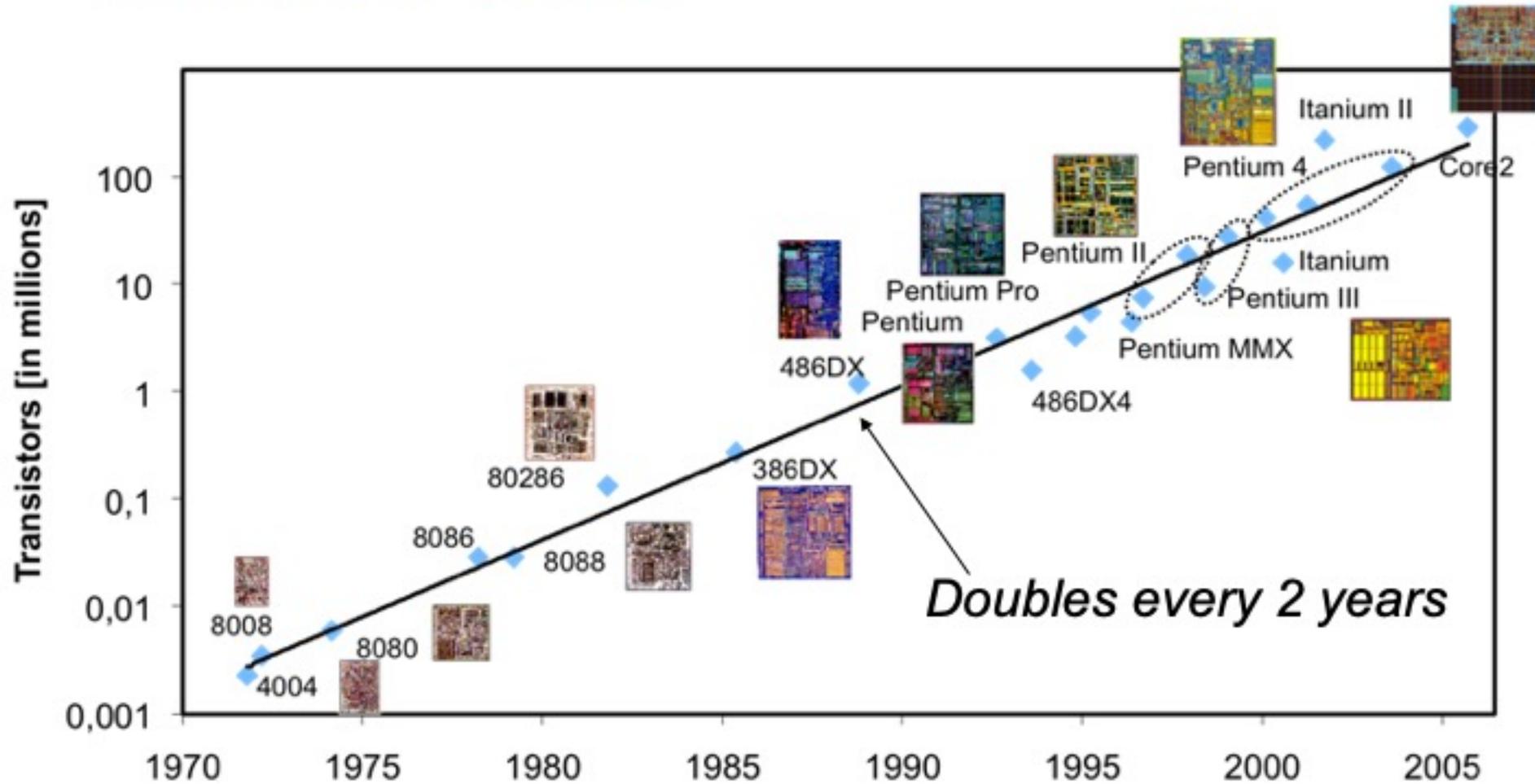
In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months

He made a prediction that semiconductor technology will double its effectiveness every 18 months

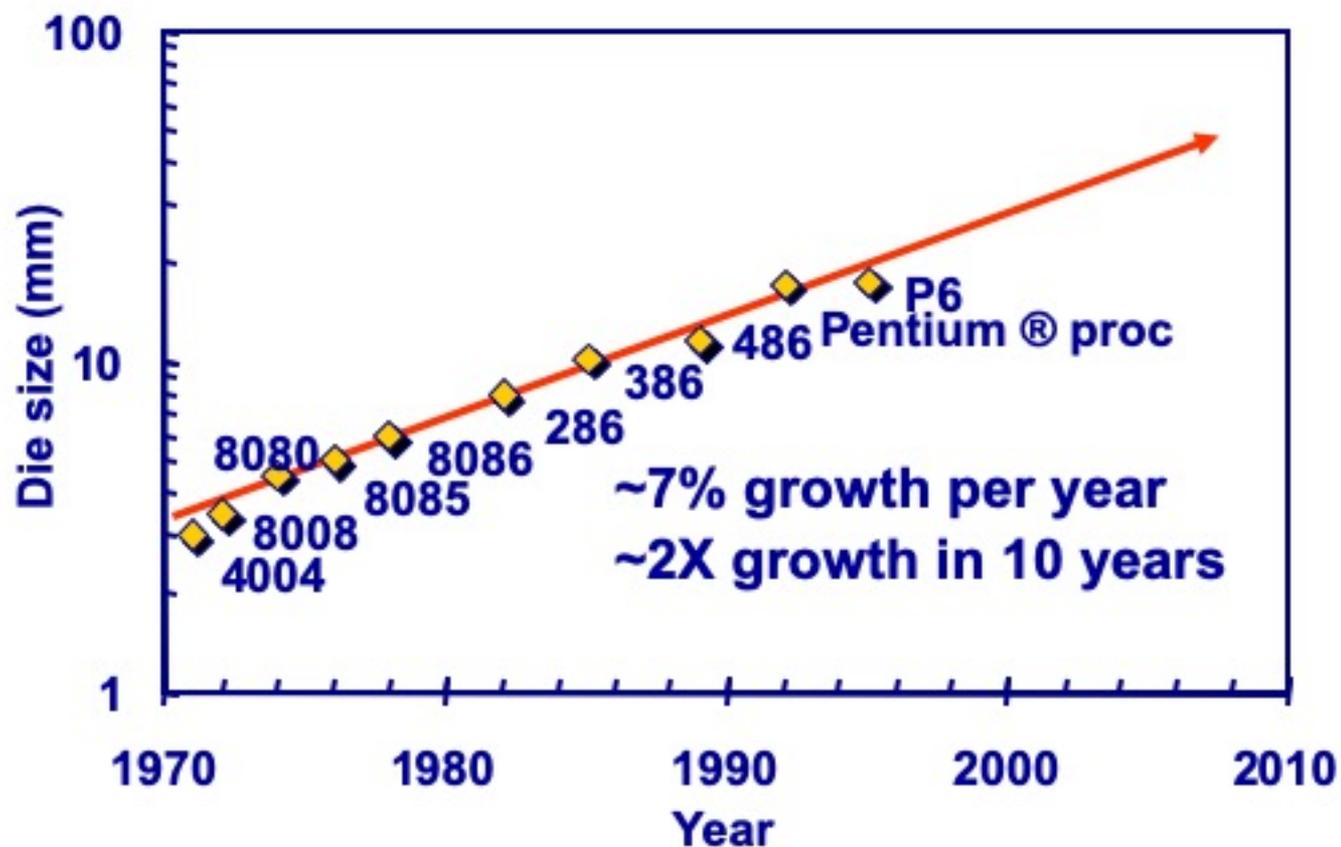


Electronics, April 19, 1965

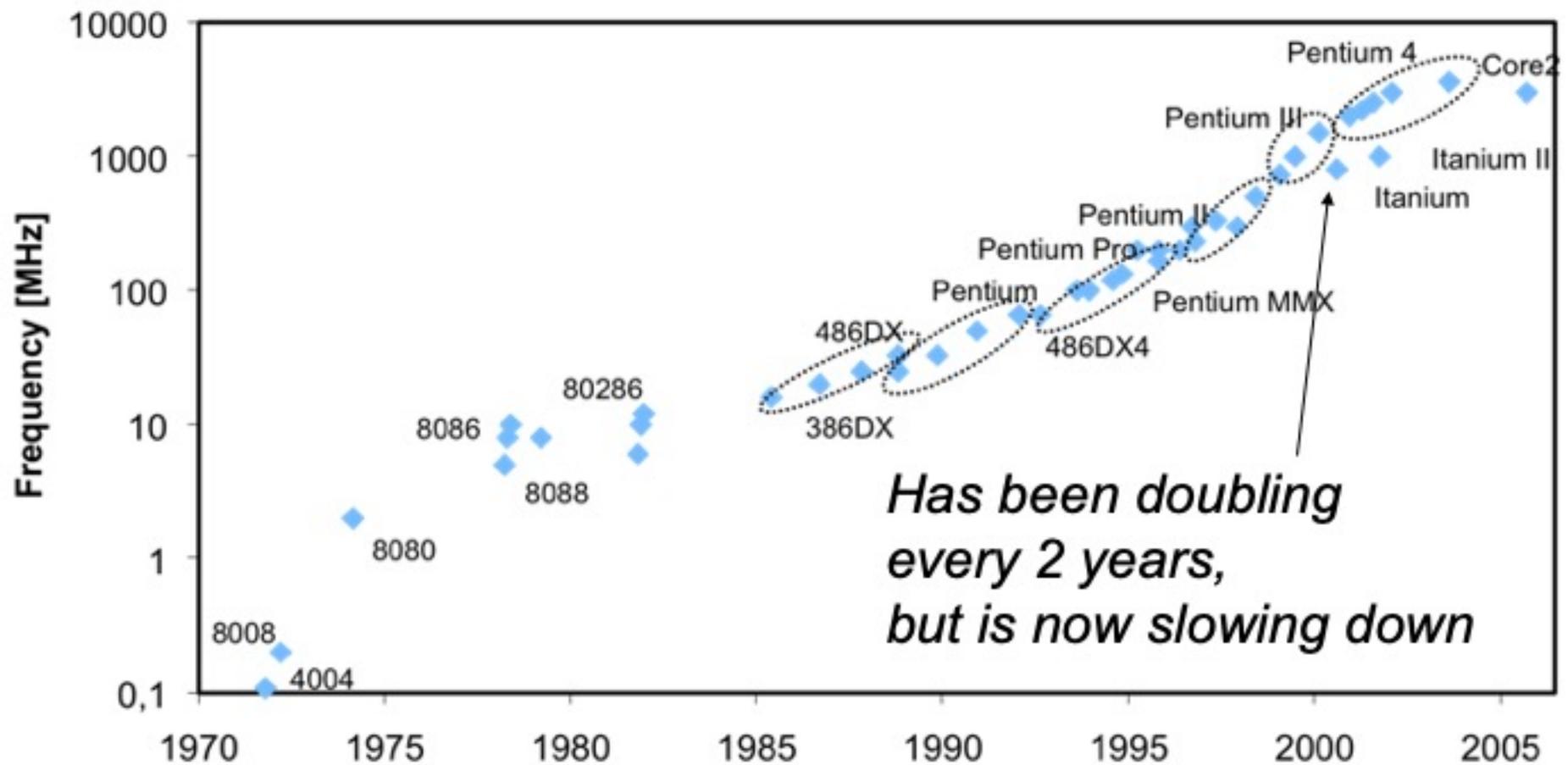
Transistor Count



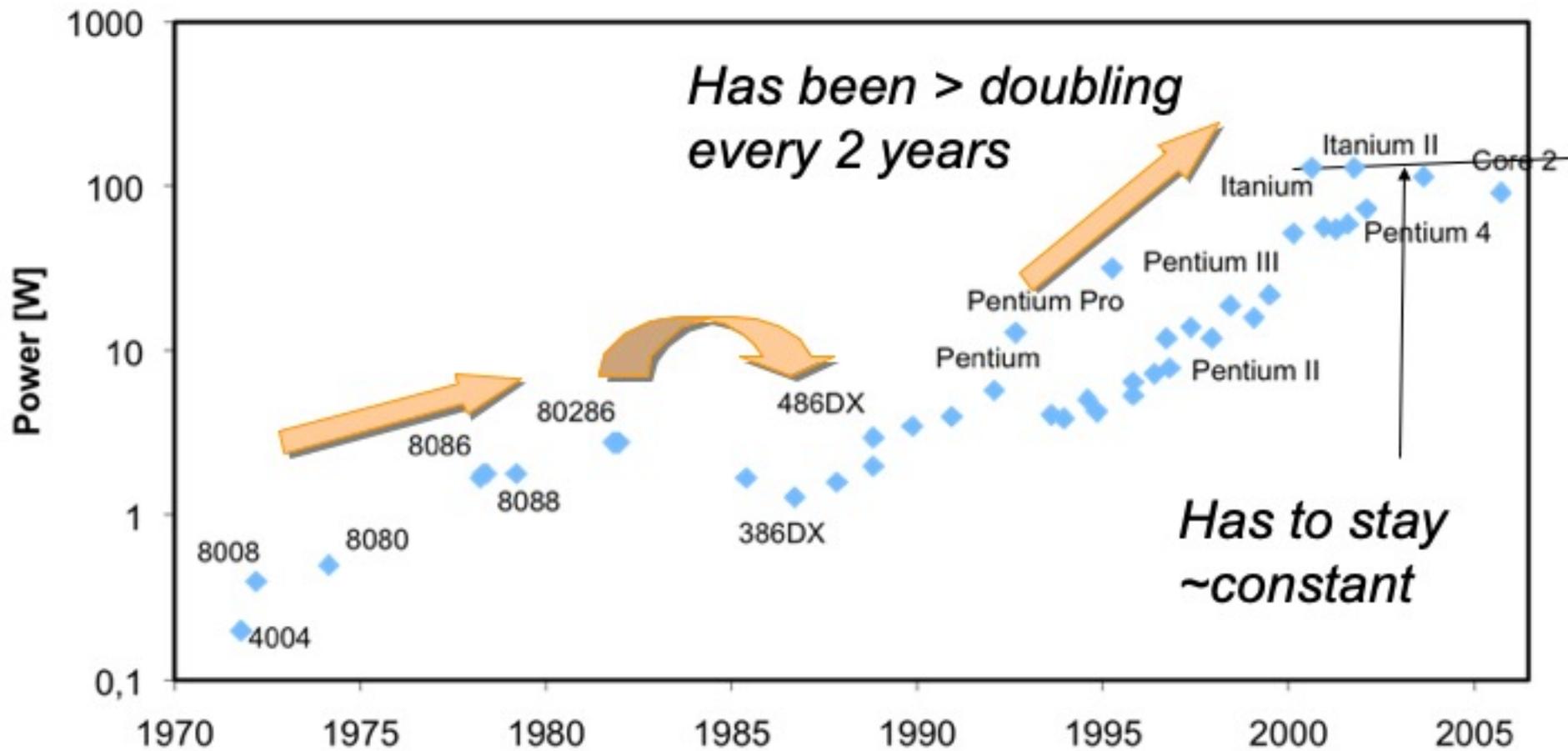
Chip Size



Frequency



Power Consumption



Design example from

***CMOS Digital Integrated Circuits:
Analysis and Design, 2nd (/3rd) ed.***

Sung-Mo Kang
Yusuf Leblebici

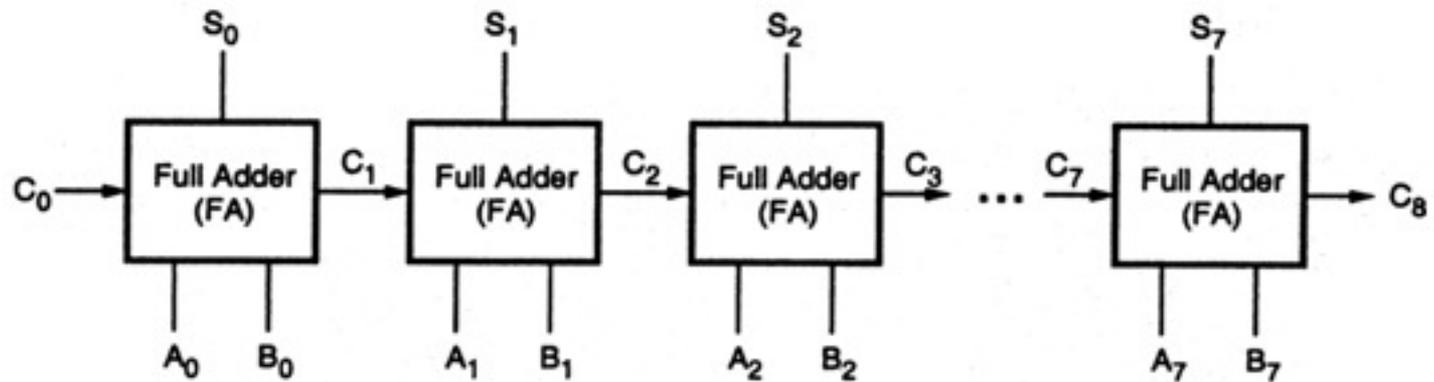


Figure 1.15. Block diagram of a carry ripple adder chain consisting of full adders.

Example 1.1

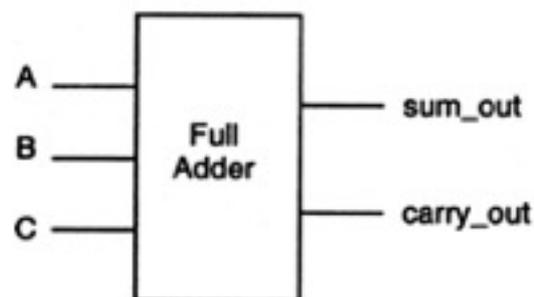
In the following example, we will design a one-bit binary full-adder circuit using 0.8- μm , twin-well CMOS technology. The design specifications are

Propagation delay times of sum and carry_out signals < 1.2 ns (worst case)

Transition delay times of sum and carry_out signals < 1.2 ns (worst case)

Circuit area < 1500 μm^2

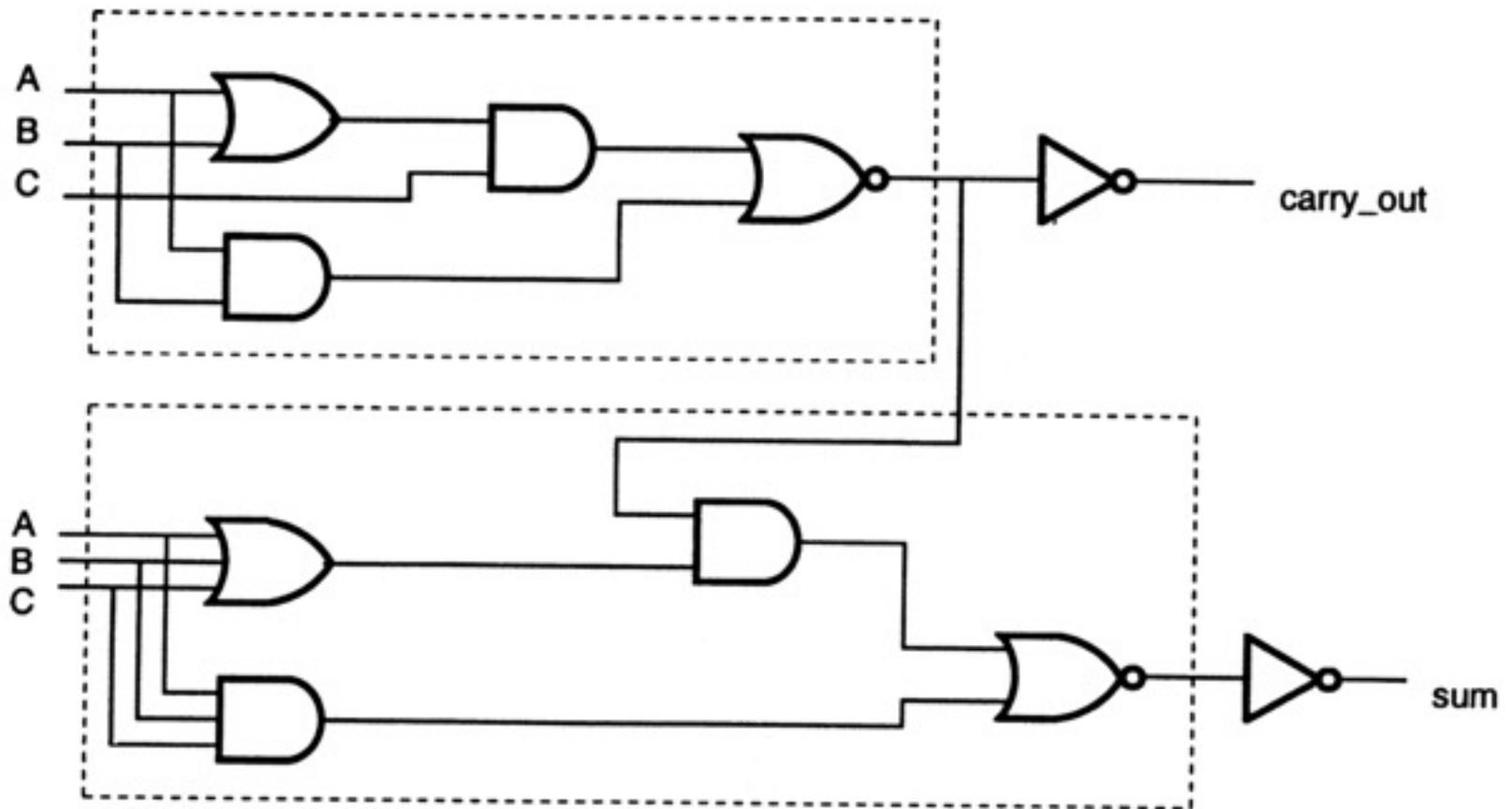
Dynamic power dissipation (@ $V_{DD} = 5\text{ V}$ and $f_{max} = 20\text{ MHz}$) < 1 mW



A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\begin{aligned}\text{sum_out} &= A \oplus B \oplus C \\ &= ABC + A\bar{B}\bar{C} + \\ &\quad \bar{A}\bar{B}C + \bar{A}\bar{C}B\end{aligned}$$

$$\text{carry_out} = AB + AC + BC$$



$$\text{sum_out} = A B C + (A + B + C) \overline{\text{carry_out}}$$

Figure 1.7. Gate-level schematic of the one-bit full-adder circuit.

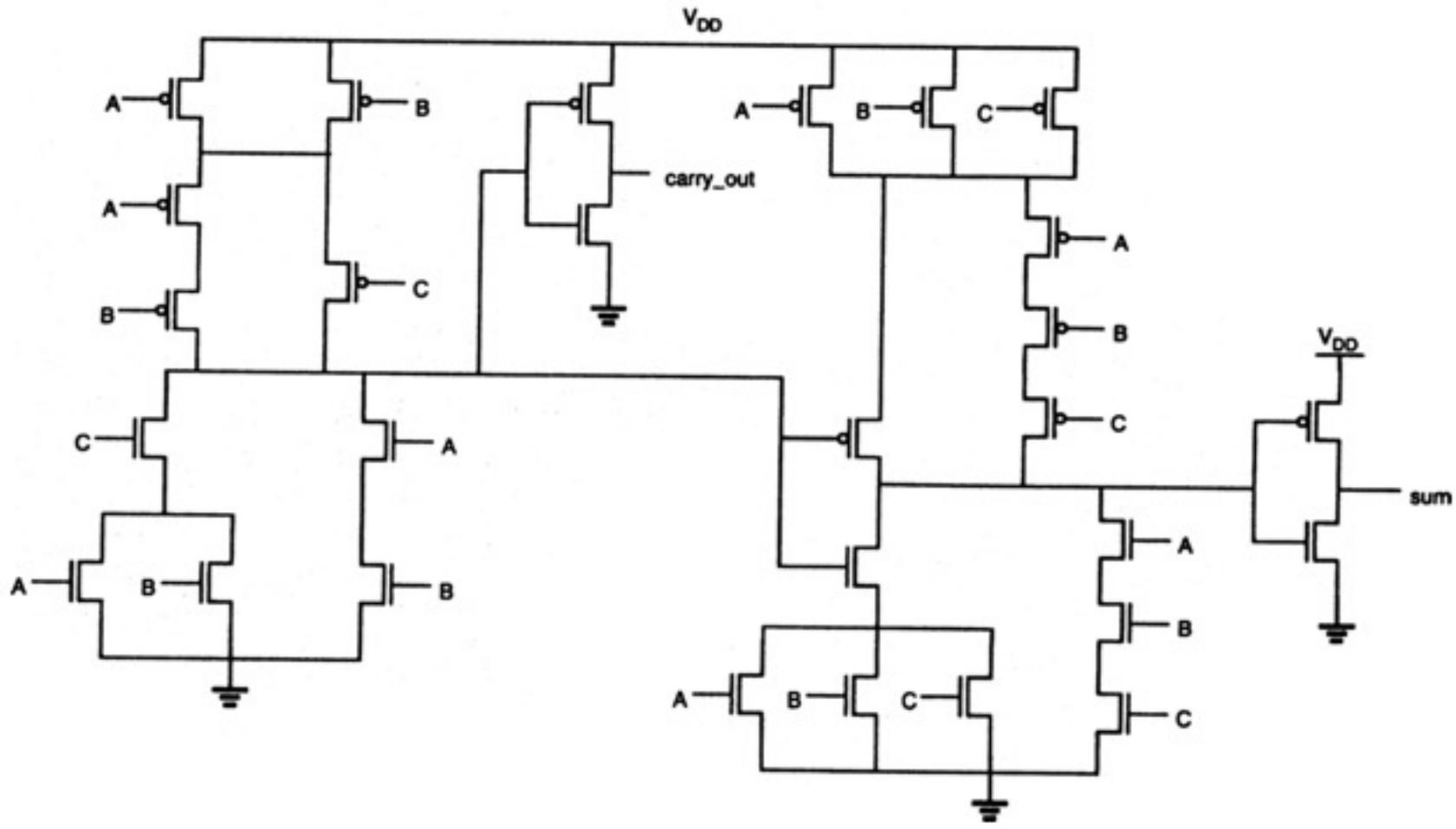


Figure 1.8. Transistor-level schematic of the one-bit full-adder circuit.

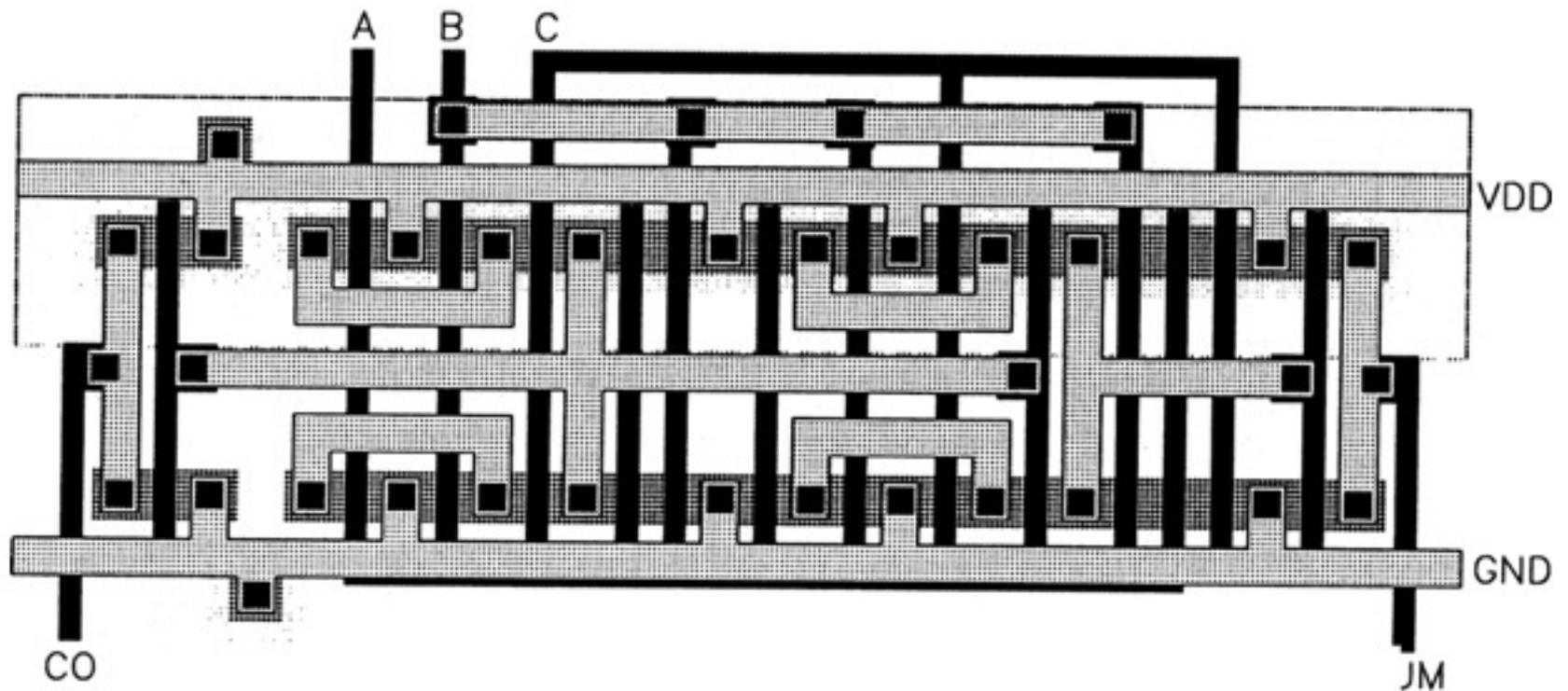


Figure 1.10. Initial layout of the full-adder circuit using minimum-size transistors.

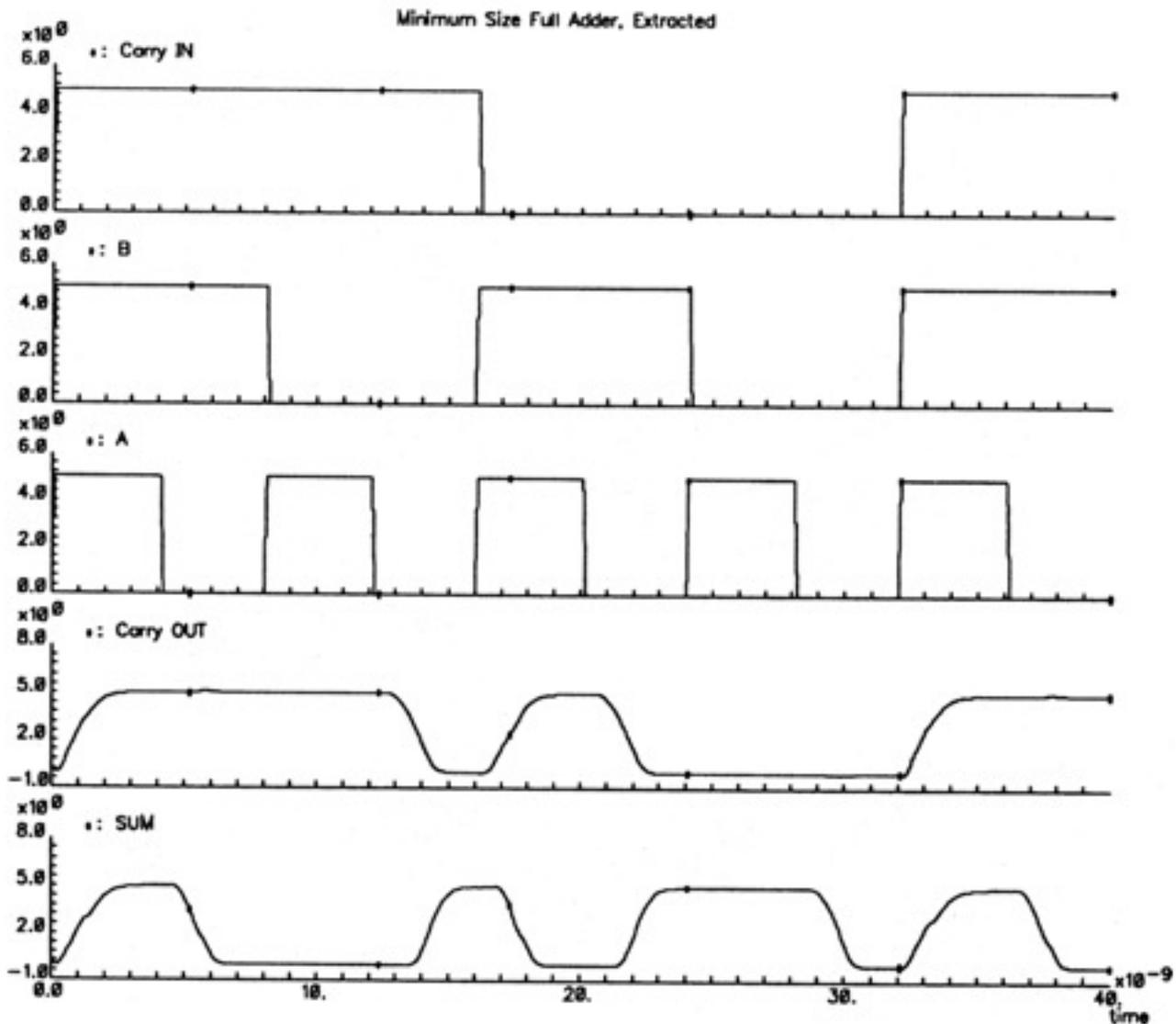


Figure 1.11. Simulated input and output waveforms of the full-adder circuit.

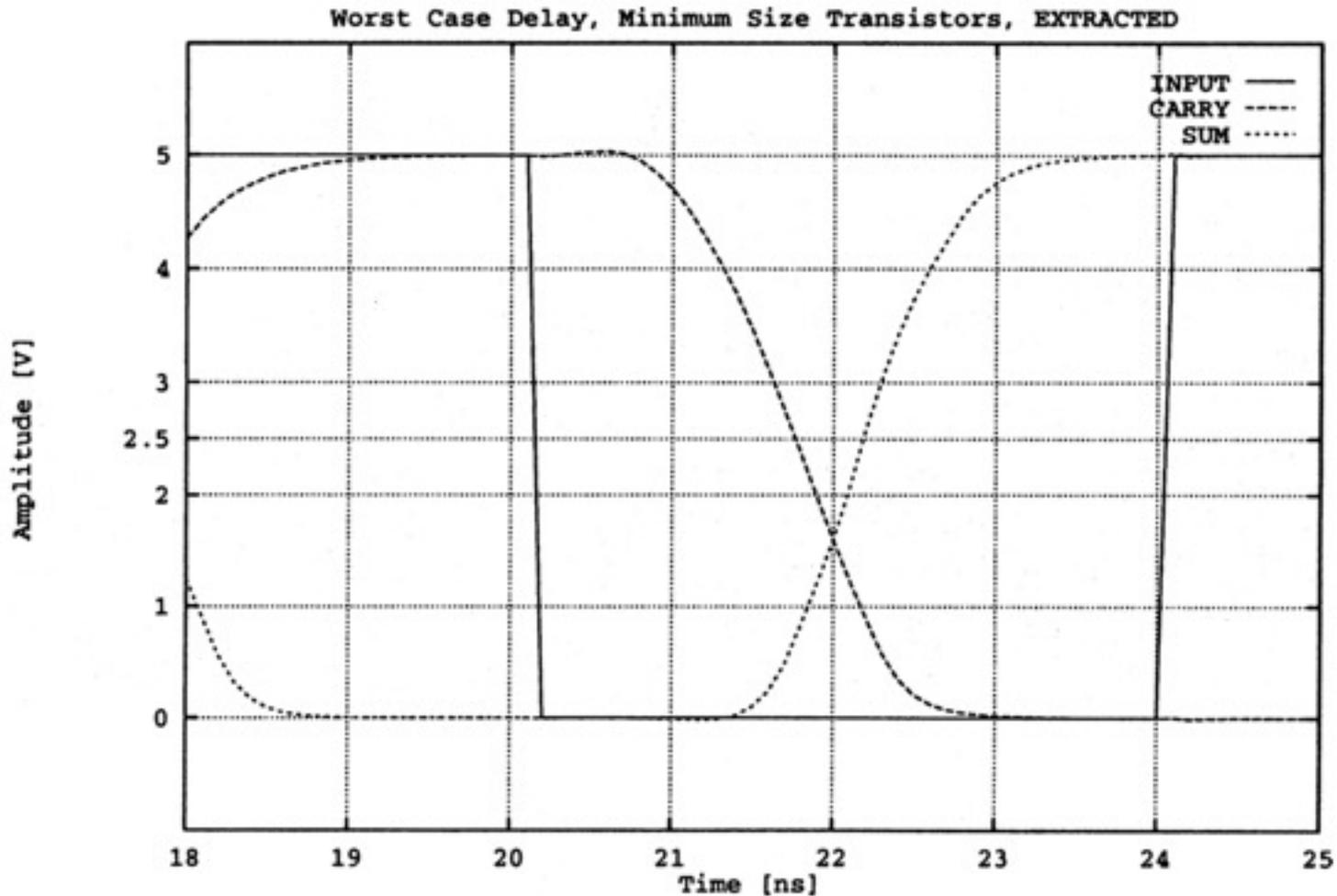


Figure 1.12. Simulated output waveforms of the full adder circuit with minimum transistor dimensions, showing the signal propagation delay during one of the worst-case transitions.

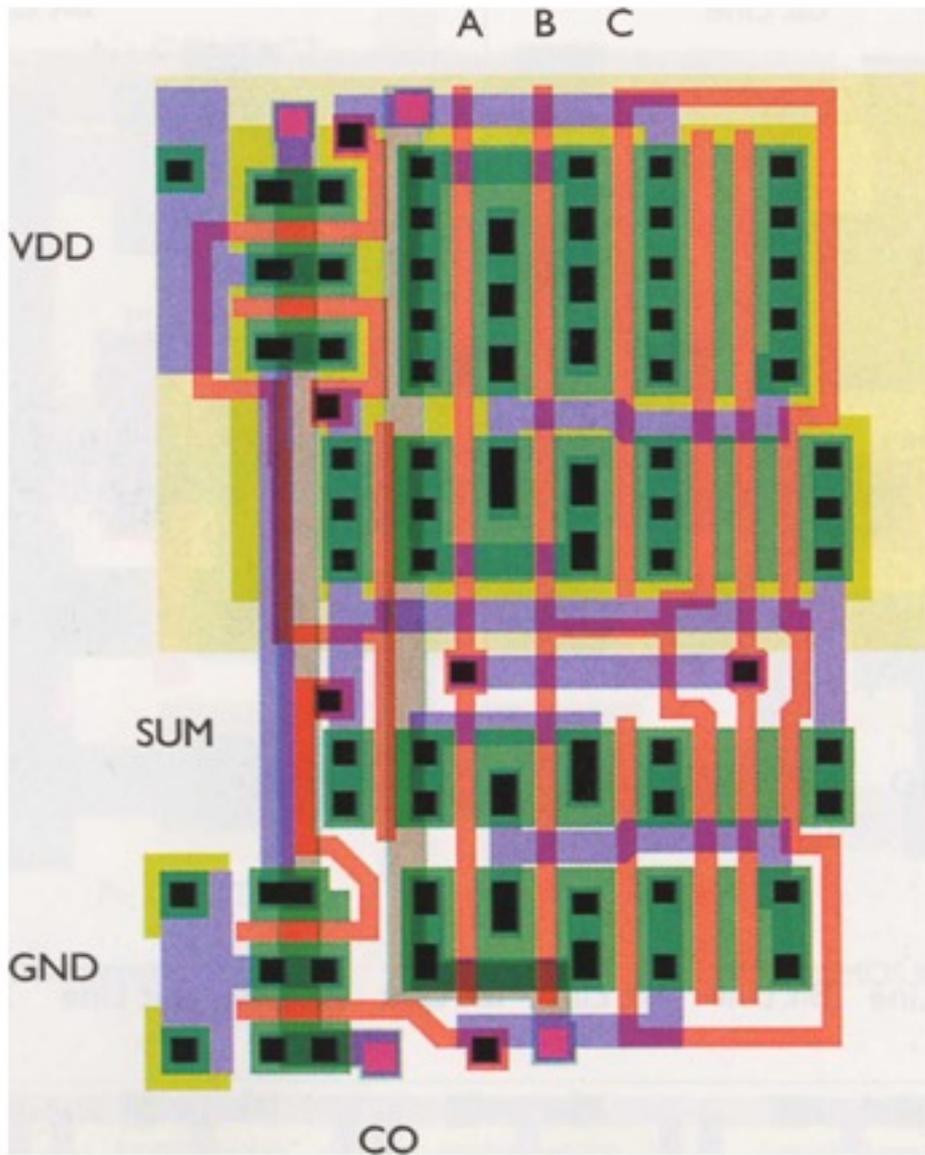


Figure 1.13. Modified layout of the full-adder circuit, with optimized transistor dimensions.

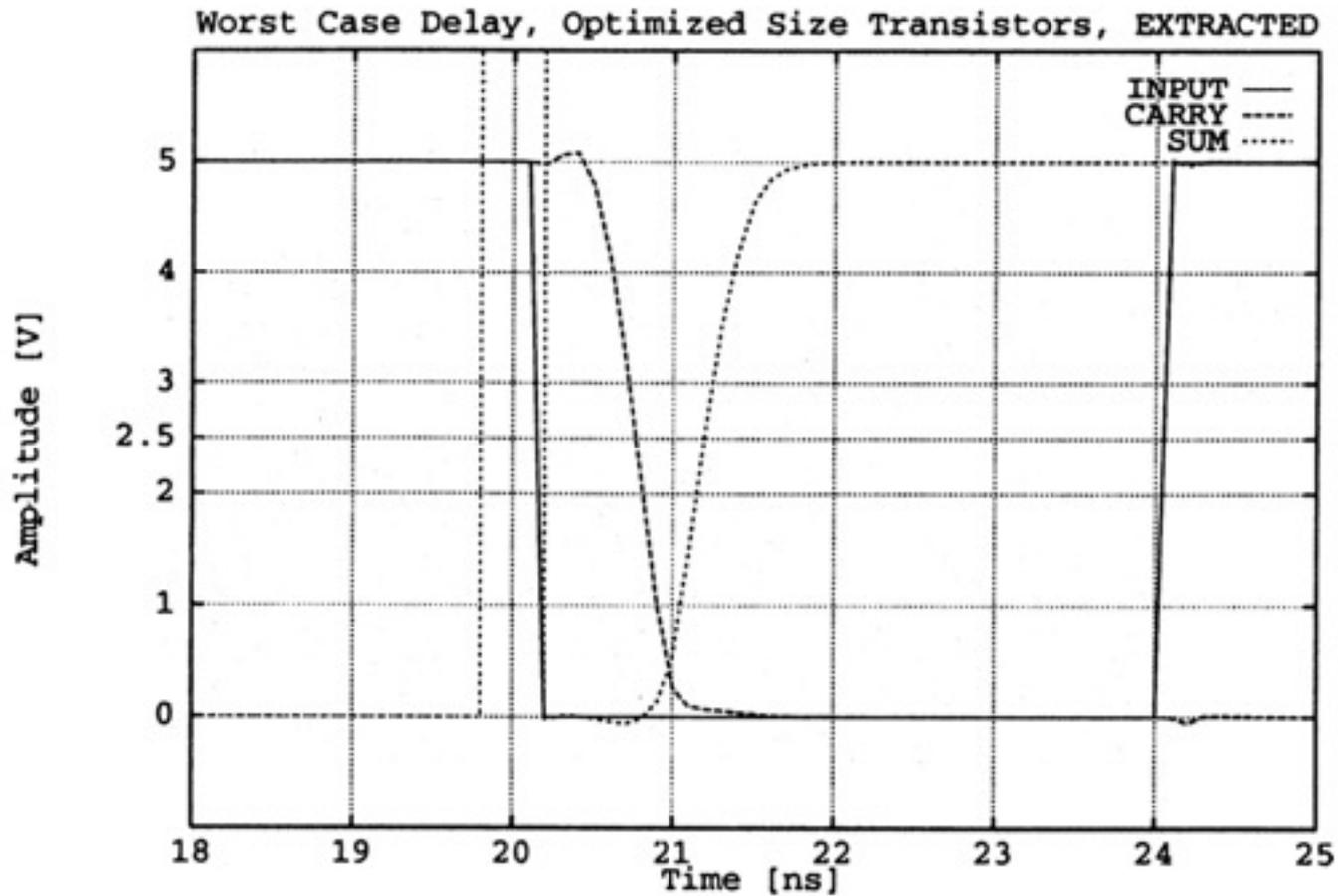


Figure 1.14. Simulated output waveforms of the full-adder circuit with optimized transistor dimensions, showing the signal propagation delay during the same worst-case transition.

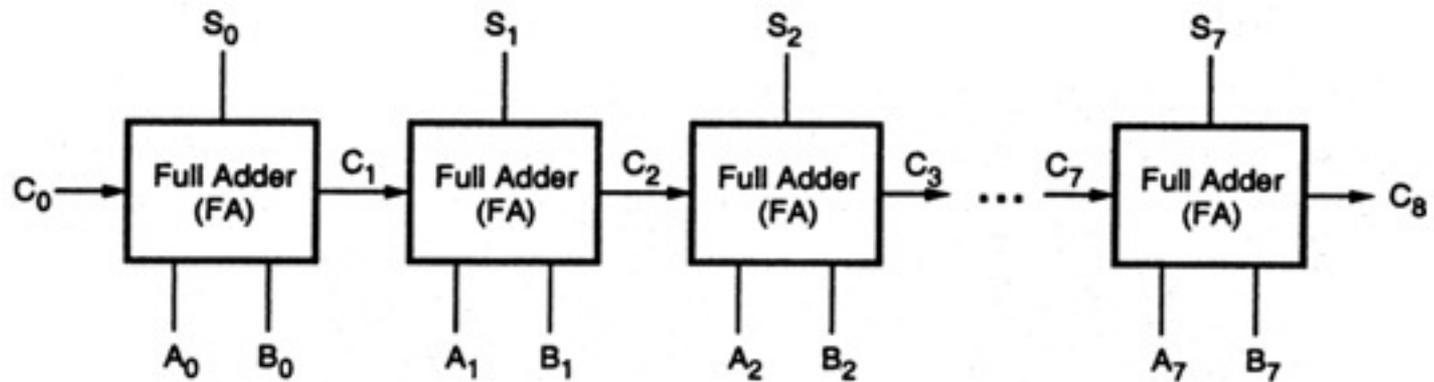


Figure 1.15. Block diagram of a carry ripple adder chain consisting of full adders.

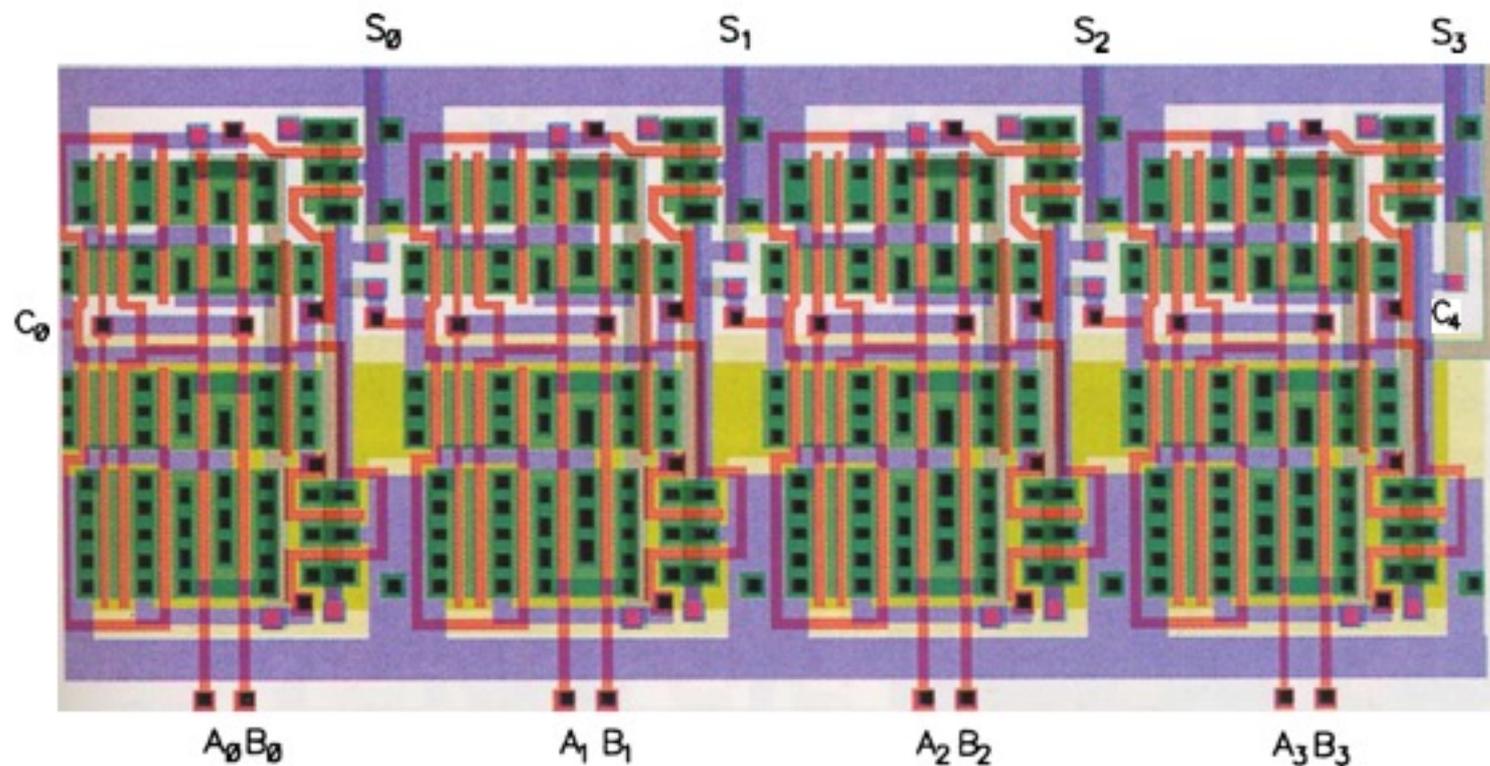


Figure 1.16. Mask layout of the carry ripple adder array.

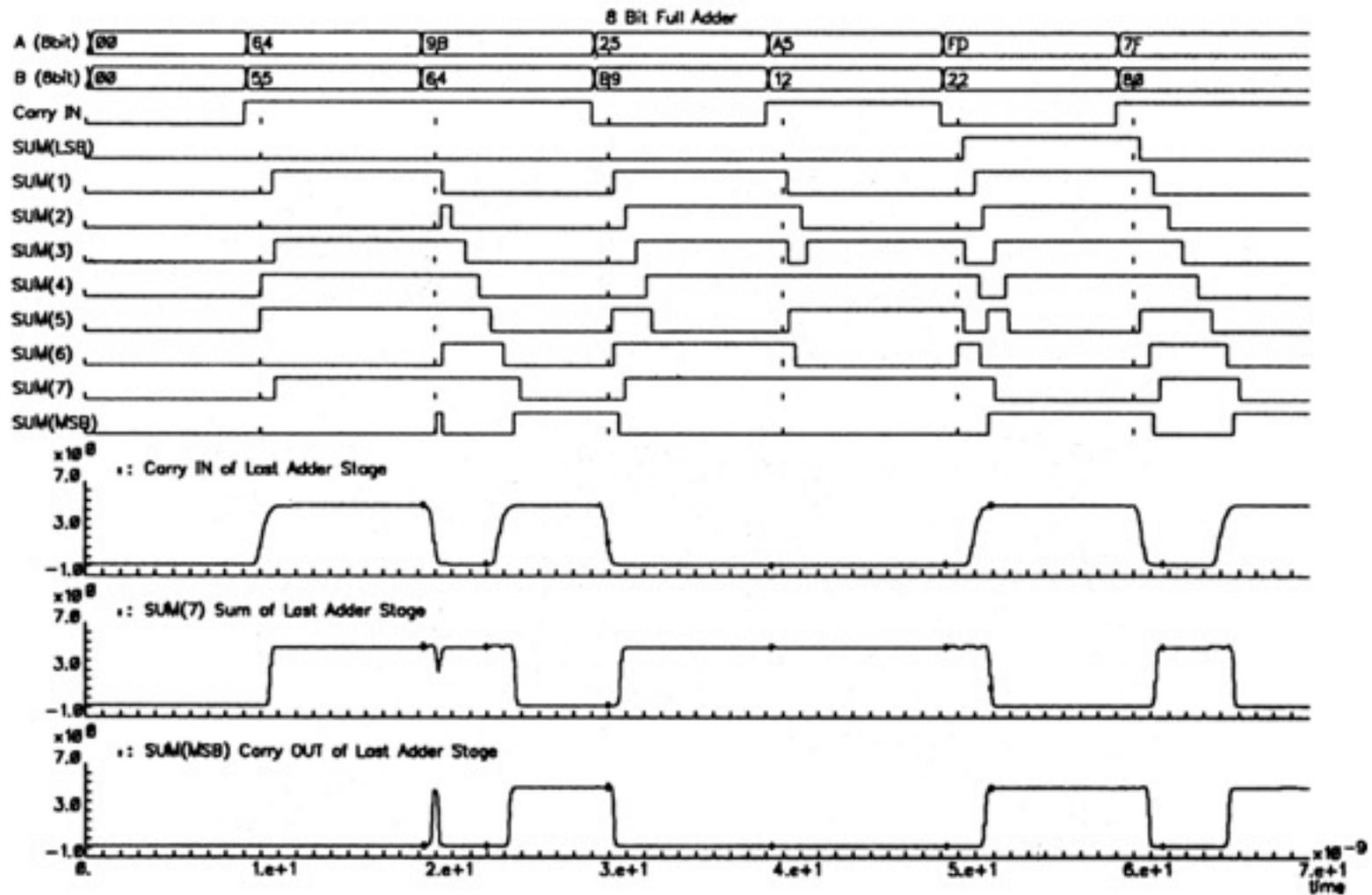


Figure 1.17. Simulated input and output waveforms of the 8-bit carry ripple adder circuit, showing a maximum signal propagation delay of about 7 ns.