Solutions to exam 2020-01-13 in TSTE85 Low Power Electronics

1. For instance, when the output of a static CMOS gate is high, at least one NMOS transistor has a gate voltage of zero. This means that the transistor operates in the subthreshold region where the current normally is small, but it is still large enough to affect the power consumption. One way to reduce the static leakage currents is to increase the bulk voltage of the PMOS transistors and decrease the bulk voltage of the NMOS transistors, which result in higher threshold voltages and therefore lower leakage currents. Another way is to use so called sleep transistors (with a higher threshold voltage) that are turned off when the circuit does no computation. A third way is to use high threshold transistors in non-critical data paths and low threshold transistor in the critical data paths.

2. The probability that the output of the NAND gate is low is $P_0 = P_aP_bP_c$, yielding the probability that the output is high as $P_1 = 1–P_0$. The transition activity is $\alpha_{01} = P_0P_1 = P_0(1–P_0)$. Find maximum transition activity:

$$\frac{d\alpha_{01}}{dP_0} = 1 - 2P_0 = 0 \Rightarrow P_0 = \frac{1}{2}, \frac{d^2\alpha_{01}}{dP_0^2} = -2 < 0 \Rightarrow \text{this is a max value}$$

Hence input probabilities given by $P_aP_bP_c$=1/2 yield highest α_{01} = 1/4. They are $P_a = P_b = P_c = 2^{-1/3} \approx 0.79$.

3.

a) Energy density and rank of the battery technologies

Battery	Voltage	Capacity	*E* density	Rank
$LiCoO_2$	3.7 V	140 mAh/g	518 Wh/kg	2
$LiMn_2O_4$	4.0 V	100 mAh/g	400 Wh/kg	4
$LiNiO_2$	3.5 V	180 mAh/g	630 Wh/kg	1
$LiFePO_4$	3.3 V	150 mAh/g	495 Wh/kg	3

b) Cells for V_{av} > 16 V and weight per battery to obtain energy 15 W for 4 h = 6 Wh

Battery	Voltage	Cells	*E* density	Weight
$LiCoO_2$	3.7 V	5	518 Wh/kg	0.12 kg
$LiMn_2O_4$	4.0 V	4	400 Wh/kg	0.15 kg
$LiNiO_2$	3.5 V	5	630 Wh/kg	0.10 kg
$LiFePO_4$	3.3 V	5	495 Wh/kg	0.12 kg

4. $$R = \frac{V_{DD,new}}{V_{DD,new} - V_T} \cdot \frac{V_{DD,old} - V_T}{V_{DD,old}} \Rightarrow V_{DD,new} = \frac{RV_TV_{DD,old}}{V_T + RV_{DD,old} - V_{DD,old}}$$

a) $V_T = 0.40 \text{ V} \Rightarrow V_{DD,new} \approx 0.78 \text{ V}$

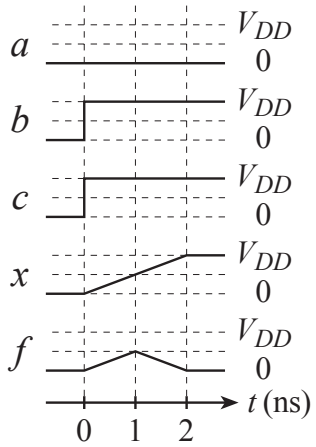
Power reduction is approximately $1 - \frac{0.78^2}{1.5^2} \approx 73\%$

b) $V_T = 0.30 \text{ V} \Rightarrow V_{DD,new} \approx 0.64 \text{ V}$

Power reduction is approximately $1 - \frac{0.64^2}{1.5^2} \approx 82\%$

5.

a) Timing with inputs applied at $t = 0$

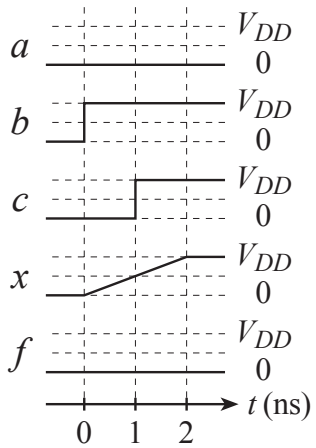


b) Calculate dissipated energy E_D as the difference between the energy E_{Bi} taken from the battery and the energy E_{Ci} stored in the capacitance of node i.

$$E_D = E_{Bx} - E_{Cx} + E_{Bf} - E_{Cf} = \int_0^{V_{DD}} C_L V_{DD}\, dV - \int_0^{V_{DD}} C_L V\, dV + \int_0^{V_{DD}/2} C_L V_{DD}\, dV - 0 =$$

$$= C_L V_{DD}\left[V\right]_0^{V_{DD}} - C_L\left[\frac{V^2}{2}\right]_0^{V_{DD}} + C_L V_{DD}\left[V\right]_0^{V_{DD}/2} = C_L V_{DD}^2 - \frac{C_L V_{DD}^2}{2} + \frac{C_L V_{DD}^2}{2} = C_L V_{DD}^2$$

c) Timing and dissipated energy with input c delayed 1 ns



$$E_D = E_{Bx} - E_{Cx} = \int_0^{V_{DD}} C_L V_{DD}\, dV - \int_0^{V_{DD}} C_L V\, dV = \frac{C_L V_{DD}^2}{2}$$

6.

a) Assume first step of charging starts at time t_0 and finishes at time t_1. Denoting the charge current i_C, capacitance of the load C, and the voltage over the load V_C, the energy taken from the V_{DD1} supply is

$$E_{VDD1} = \int_{t_0}^{t_1} V_{DD1} i_C\, dt = \int_{t_0}^{t_1} V_{DD1} C\left(\frac{dV_C}{dt}\right) dt = \left\langle t_1 \gg t_0 \right\rangle = V_{DD1} C \int_0^{V_{DD1}} dV_C = C V_{DD1}^2$$

Assume second step of charging finishes at time t_2. The energy taken from the V_{DD2} supply during this phase is

$$E_{VDD2} = \int_{t_1}^{t_2} V_{DD2} i_C \, dt = \int_{t_1}^{t_2} V_{DD2} C \left(\frac{dV_C}{dt} \right) dt = \left\langle t_2 \gg t_1 \right\rangle = V_{DD2} C \int_{V_{DD1}}^{V_{DD2}} dV_C = C V_{DD2} \left(V_{DD2} - V_{DD1} \right)$$

Total energy taken from both supplies is

$$E_{tot} = E_{VDD1} + E_{VDD2} = C \left(V_{DD1}^2 + V_{DD2}^2 - V_{DD1} V_{DD2} \right)$$

Energy stored in the capacitor is

$$E_C = C V_{DD2}^2 / 2$$

Dissipated energy is

$$E_{diss} = E_{tot} - E_C = \left\langle t_2 \gg t_1 \gg t_0 \right\rangle = C \left(V_{DD1}^2 + V_{DD2}^2 / 2 - V_{DD1} V_{DD2} \right)$$

b) Assume ratio $r = V_{DD1}/V_{DD2} \Rightarrow$

$$E_{diss} = C \left(r^2 V_{DD2}^2 + V_{DD2}^2 / 2 - r V_{DD2}^2 \right) = \left(r^2 - r + 1/2 \right) C V_{DD2}^2$$

Find minimal energy dissipation with respect to r

$$\frac{dE_{diss}}{dr} = \left(2r - 1 \right) C V_{DD2}^2 = 0 \Rightarrow r = \frac{1}{2}, \quad \frac{d^2 E_{diss}}{dr^2} = C V_{DD2}^2 > 0 \Rightarrow r = \frac{1}{2} \text{ is a local minima}$$

Minimal energy dissipation

$$E_{min} = C \left(V_{DD2}^2 / 4 + V_{DD2}^2 / 2 - V_{DD2}^2 / 2 \right) = C V_{DD2}^2 / 4 \text{ for } V_{DD1} = V_{DD2} / 2$$

7.

a) Critical path through c-d $\Rightarrow t_{old} = 4 + 3$ ns $= 7$ ns @ $V_{dd} = V_{old} = 1.5$ V

Relation between old and new times and supply voltages

$$\frac{t_{new}}{t_{old}} = \frac{V_{new}}{\left(V_{new} - V_T \right)^2} \cdot \frac{\left(V_{old} - V_T \right)^2}{V_{old}}$$

where

$t_{new} = (125 \text{ MHz})^{-1} = 8$ ns, $V_T = 0.4$ V and V_{new} is sought

Solve e.g. by inserting numerical values

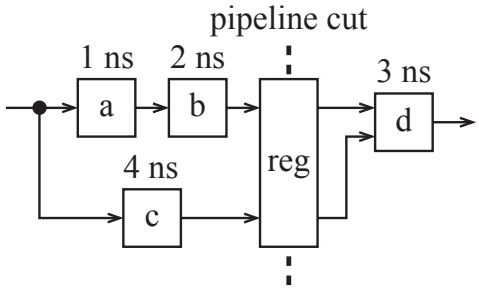
$$\frac{8^2}{7^2} = \frac{V_{new}}{\left(V_{new} - 0.33 \right)^2} \cdot \frac{\left(1.5 - 0.33 \right)^2}{1.5} \Leftrightarrow \frac{8^2 \cdot 1.5}{7^2 \cdot \left(1.5 - 0.33 \right)^2} \left(V_{new} - 0.33 \right)^2 - V_{new} = 0 \Rightarrow$$

$V_{new} \approx 1.38$ V (other solution is less than V_T)

Power saving

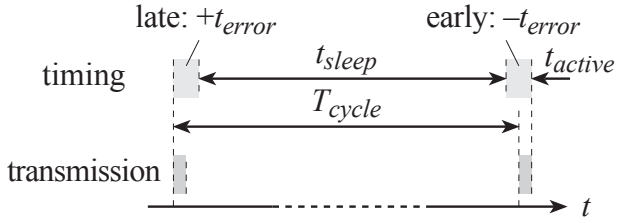
$$S = 1 - \frac{P_{new}}{P_{old}} = 1 - \frac{f C V_{new}^2}{f C V_{old}^2} \approx 1 - \frac{1.38^2}{1.5^2} \approx 15\%$$

b) Pipelining according to e.g. cut in figure below



New critical path is through c-reg. Repeating calculations with $t_{old} = t_{pipe} = 4$ ns yields $V_{pipe} \approx 1.01$ V and $S_{pipe} \approx 54\%$.

8. Consider the diagram below that illustrates required timing to let the system be active during transmissions. We need to add one maximum error to the active intervals due to late wake ups and another maximum error due to early wakeups to not miss the transmission intervals.



a) Timing when missed transmissions are allowed
$t_{error} = 0 \Rightarrow t_{active} = 0.001$ s, $t_{sleep} = 0.999$ s and $T_{cycle} = t_{active} + t_{sleep} = 1.000$ s

Power dissipation
$P_{active} = 2 \cdot 10^{-3}$ W, $P_{sleep} = 200 \cdot 10^{-9}$ W, $P_{timer} = 100 \cdot 10^{-9}$ W

$$P_a = \frac{P_{active} t_{active}}{T_{cycle}} + \frac{P_{sleep} t_{sleep}}{T_{cycle}} + P_{timer} \approx 2.2\ \mu\text{W}$$

b) Timing when missed transmissions are not allowed
$t_{error} = 0.999 \cdot 500 \cdot 10^{-6}$ s ≈ 0.0005 s $\Rightarrow$
$t'_{active} = t_{active} + 2t_{error} \approx 0.002$ s and $t'_{sleep} = t_{sleep} - 2t_{error} \approx 0.998$ s

Power dissipation

$$P_b = \frac{P_{active} t'_{active}}{T_{cycle}} + \frac{P_{sleep} t'_{sleep}}{T_{cycle}} + P_{timer} \approx 4.2\ \mu\text{W}$$

c) Timing after redesign with more accurate sleep timer
$t''_{error} = 0.999 \cdot 200 \cdot 10^{-6}$ s ≈ 0.0002 s $\Rightarrow$
$t''_{active} = t_{active} + 2t''_{error} \approx 0.0014$ s and $t''_{sleep} = t_{sleep} - 2t''_{error} \approx 0.9986$ s

Power dissipation
$P''_{timer} = 40 \cdot 10^{-9}$ W

$$P_c = \frac{P_{active} t''_{active}}{T_{cycle}} + \frac{P_{sleep} t''_{sleep}}{T_{cycle}} + P''_{timer} \approx 3.0\ \mu\text{W}$$