Solutions to exam 2019-01-11 in TSTE85 Low Power Electronics

1.

a) Some historical applications: wrist watches, pocket calculators, cellular phones, pagers, hearing aids, pacemakers.

b) *Transition strategies* aim at solving the problem when a component should be switched between different modes.

Load-change strategies aim at modifying the functionality of a component so it can be in low-power modes more often.

Adaptation strategies aim at modifying the software to novel, power-saving uses of components.

c) Average power determines battery life time and cooling requirements. Peak power determines the width of power supply wires, number of bonding wires, and amount of bypass capacitors, and affects the design effort required for proper signal integrity.

d) There is no power wasted in driving the extra stray capacitance of the pad, package, and board.

e) Based on the precomputation of a subset of the input signals, decision can be made whether the rest of the input signals must be taken to into account. If the rest of the input signals can be ignored power is saved that clock cycle.

2. For example, when the output of a static CMOS gate is high, at least one NMOS transistor has a gate voltage of zero. This means that the transistor operates in the subthreshold region where the current normally is small, but it is still large enough to affect the power consumption. One way to reduce the static leakage currents is to increase the bulk voltage of the PMOS transistors and decrease the bulk voltage of the NMOS transistors which result in higher threshold voltages and therefore lower leakage currents. Another way is to use so called sleep transistors (with a higher threshold voltage) that are turned off when the circuit does no computation. A third way is to use high threshold transistors in non-critical data paths and low threshold transistor in the critical data paths.

3. The propagation delay is

$$t_p = \frac{\Delta Q}{I_D} = \frac{C\frac{V_{DD}}{2}}{k'\frac{W}{L}(V_{DD}-|V_T|)^r} = t_p(C, V_{DD}, W)$$

where $r = 2$ for long-channel case and $r = 1.5$ for short-channel case

a) *Long-channel case*

Assume original delay is $t_{p0}(C_{out} + C_w + C_{in}, V_0, W_0)$

$C_{out}, C_{in} \propto W \Longrightarrow$ delay of scaled circuit is $t_{p1}(2C_{out} + C_w + 2C_{in}, V_1, 2W_0)$

Equalize propagation delays

$$t_{p0} = t_{p1} \Leftrightarrow \frac{(C_{out}+C_w+C_{in})V_0/2}{k'(W_0/L)(V_0-|V_T|)^2} = \frac{(2C_{out}+C_w+2C_{in})V_1/2}{k'(2W_0/L)(V_1-|V_T|)^2} \Leftrightarrow \frac{(C_0+4C_0+C_0)V_0}{(V_0-|V_T|)^2} = \frac{(2C_0+4C_0+2C_0)V_1}{2(V_1-|V_T|)^2}$$

$$\Leftrightarrow \frac{6V_0}{(V_0-|V_T|)^2} = \frac{8V_1}{2(V_1-|V_T|)^2}$$

Insert voltages and solve for V_1

$$\frac{6\cdot 1.2}{(1.2-0.4)^2} = \frac{8V_1}{2(V_1-0.4)^2} \Longrightarrow V_1^2 - \frac{26}{45}V_1 + \frac{4}{25} = 0 \Longrightarrow V_1 = \frac{26}{45} \pm \sqrt{\left(\frac{26}{45}\right)^2 - \frac{4}{25}} \approx \begin{cases} 0.995\ \text{V} \\ (0.161\ \text{V}) \end{cases}$$

Relative dynamic power consumption

$$P_{\text{rel}} = \frac{f(2C_{out}+C_w+2C_{in})V_1^2}{f(C_{out}+C_w+C_{in})V_0^2} = \frac{(2C_0+4C_0+2C_0)V_1^2}{(C_0+4C_0+C_0)V_0^2} = \frac{4V_1^2}{3V_0^2} \approx 0.916$$

The dynamic power consumption decreases with 8.4% using the wider transistors in the long-channel case

b) *Short-channel case*

Equalize propagation delays

$$t_{p0} = t_{p1} \Leftrightarrow \frac{(C_{out}+C_w+C_{in})V_0/2}{k'(W_0/L)(V_0-|V_T|)^{1.5}} = \frac{(2C_{out}+C_w+2C_{in})V_1/2}{k'(2W_0/L)(V_1-|V_T|)^{1.5}} \Leftrightarrow \frac{6V_0}{(V_0-|V_T|)^{1.5}} = \frac{8V_1}{2(V_1-|V_T|)^{1.5}} \Longrightarrow$$

$$f(V_1) = 7.2(V_1-0.4)^{1.5} - 4\cdot 0.8^{1.5}V_1 = 0 \Longrightarrow V_1 \approx 0.906\ \text{V}$$

Relative dynamic power consumption

$$P_{\text{rel}} = \frac{f(2C_{out}+C_w+2C_{in})V_1^2}{f(C_{out}+C_w+C_{in})V_0^2} = \frac{4V_1^2}{3V_0^2} \approx 0.761$$

The dynamic power consumption decreases with 24% using the wider transistors in the short-channel case

4.

a) Stored energy at t_1 is $E_{C1} = \frac{C}{2}\left(\frac{V_{DD}}{X}\right)^2$

b) Stored energy at t_2 is $E_{C2} = \frac{CV_{DD}^2}{2}$

c) Energy drawn from the power supply from t_0 to t_1 is $E_{B01} = C\left(\frac{V_{DD}}{X}\right)^2$

Energy drawn from the power supply from t_1 to t_2 is $E_{B02} = CV_{DD}\left(V_{DD} - \frac{V_{DD}}{X}\right)$

Total drawn energy is $E_B = CV_{DD}^2\left(\frac{1}{X}\right)^2 + CV_{DD}^2\left(1-\frac{1}{X}\right) = CV_{DD}^2\left(1-\frac{1}{X}+\frac{1}{X^2}\right)$

d) To minimize the energy we can minimize function $f(X) = 1-X^{-1}+X^{-2}$ derived in c)

Derivate $f(X)$ and solve for $f'(X) = 0$: $f'(X) = \frac{1}{X^2} - \frac{2}{X^3} = 0 \Rightarrow X = 2$

Check if $X = 2$ is a minima or a maxima: $f''(X) = -\frac{2}{X^3} + \frac{6}{X^4} \Rightarrow f''(2) = \frac{1}{8}$

$f''(2)$ is positive, hence we have found a minima.

To minimize the power drawn from the power supply, choose $X = 2$

5.

a) One's probabilities and transition activities of the nodes

$P_a = 0.1 \Rightarrow \alpha_{a01} = (1 - P_a)P_a = 0.09$
$P_b = 0.2 \Rightarrow \alpha_{b01} = (1 - P_b)P_b = 0.16$
$P_c = 0.3 \Rightarrow \alpha_{c01} = (1 - P_c)P_c = 0.21$
$P_x = 1 - (1 - P_a)(1 - P_b) = P_a + P_b - P_aP_b = 0.28 \Rightarrow \alpha_{x01} = (1-P_x)P_x = 0.2016$
$P_f = P_xP_c = 0.084 \Rightarrow \alpha_{f01} = (1-P_f)P_f = 0.076944$

Dynamic power consumption assuming a zero-delay model
$P_0 = (\alpha_{a01} + \alpha_{b01} + \alpha_{c01} + \alpha_{x01} + 3\alpha_{f01})C_0fV_{DD}^2 \approx 6.4\ \mu W$

b) *x* will be delayed compared with *c*, resulting in glitches in node *f*. Glitches occur in some cases when there are transitions in *x* and *c*. Since there is only one delayed extra state, a glitch can only occur when the output *f* is not supposed to make a transition.

There is no case with glitches when node *f* is held steady high, since there is only one state yielding this output. Let us investigate the input transitions that should yield a steady low output:

$x\ c\ f$	$\rightarrow$	$x\ c'\ f'$	$\rightarrow$	$x'c'\ f''$
0 0 0		0 1 0		0 1 0
0 0 0		0 0 0		1 0 0
0 1 0		0 0 0		0 0 0
0 1 0		0 0 0		1 0 0
1 0 0		1 0 0		0 0 0
1 0 0		1 1 1		0 1 0

The last transition $<x\ c> = 1\ 0 \rightarrow 1\ 1 \rightarrow 0\ 1$ yields a glitch

The transition activity for this case is $\alpha_g = P_x(1 - P_c)(1 - P_x)P_c = 0.042336$

Dynamic power consumption assuming a unit-delay model

$P_1 = P_0 + 3\alpha_g C_0 f V_{DD}^2 \approx 7.3\ \mu W$

6.

a) Power dissipation: $P = I_{av}V_{DD} = (Q/T)V_{DD} = CV_{pp}fV_{DD} = fCV_{pp}V_{DD}$

b) Assume $V_{pp} = cV_{DD}$, where $0 < c < 1$ is a constant.

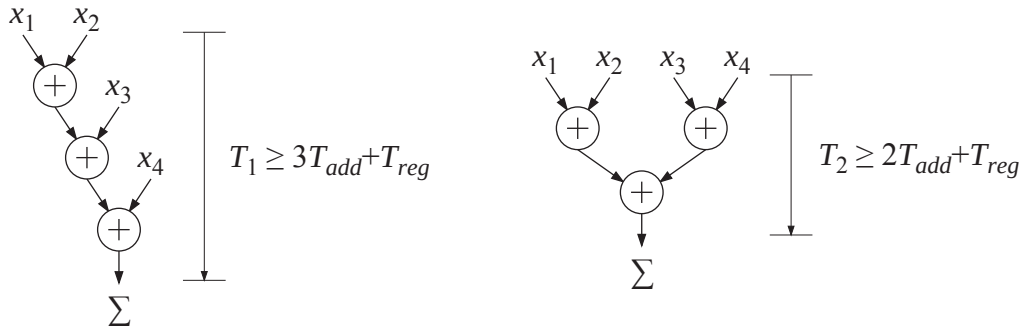
Signal-to-noise ratio: $\text{SNR} = 10\log\left[Cc^2V_{DD}^2/(8kT)\right] \Rightarrow cCV_{DD}^2 = \dfrac{8kT}{c}10^{0.1SNR}$

Power dissipation: $P = cCfV_{DD}^2 = \dfrac{8kT}{c}f10^{0.1SNR}$

We see that the power is determined from SNR, *f*, and *T* since *c* and *k* are constants. These variables should be selected as low as possible for minimum power dissipation, restricted by the respective requirements. Hence, these requirements determine the minimum power dissipation.

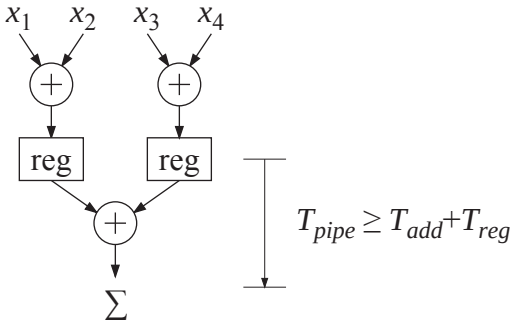
7.

a) There are two major circuit structures, one based on a cascading of operations, shown to the left below, while the second to the right is based on a tree structure:



Comparing those it can be seen that the sequential structure has more cascaded operations and, hence, a longer critical path than the tree structure. More cascaded operations generally infer more paths with different delay which is a major cause of glitches. Further, the operations towards the end of the cascade will have inputs with more glitches than in the tree, making the case even worse. From a dynamic power point of view it is also good if the critical path can be made short. If we are able to decrease the minimal clock period, we can use supply voltage scaling to save power assuming a fixed throughput. This is because the dominant dynamic power dissipation is proportional to V_{DD}^2, while the throughput is approximately proportional to V_{DD}. Hence, by decreasing V_{DD} until the requirement on throughput is met, there will be large savings in power due to the square relation. The large savings possible allow us to afford certain overhead in terms of hardware, e.g., pipelining registers, with a net gain in power dissipation as long as the increase in throughput is enough. In both cases above, the tree structure performs generally performs better and thus should be preferred.

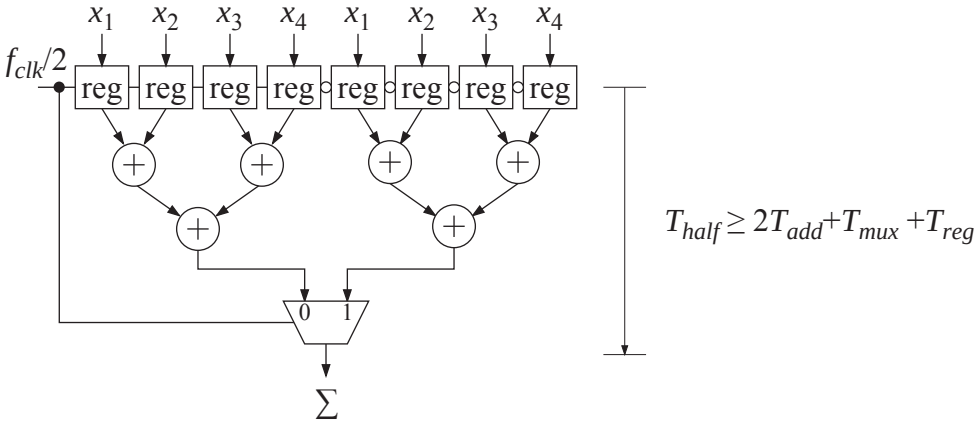
b) Pipelined tree structure with two additional registers:



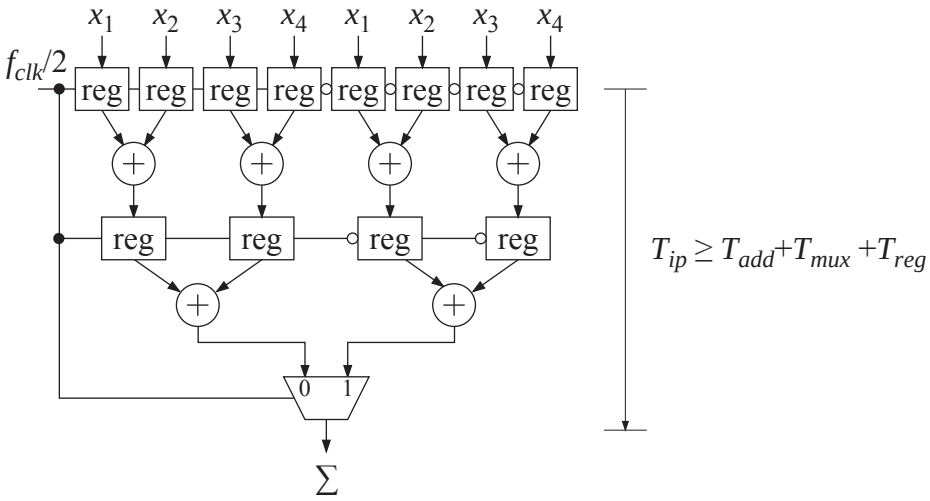
Minimal clock frequency in pipelined circuit: $T_{\text{pipe}} \geq T_{\text{add}} + T_{\text{reg}}$. That is, the minimal clock period is T_{pipe} shorter than the original tree structure. For this case, the additional throughput can be traded for lower power dissipation if the overhead of the two registers is less than the gain of supply voltage scaling.

c) An interleaved circuit with identical two blocks using four additional registers and one multiplexer is shown on the next page. Note that the overhead in terms of power of the registers is less than normal registers since they should be clocked at half frequency. The minimal clock frequency in the circuit path is $T_{\text{half}} \geq 2T_{\text{add}}+T_{\text{mux}}+T_{\text{reg}}$. However, since the requirement on throughput in each block is halved, the required clock period is

$T_{int} \geq T_{add}+(T_{mux}+T_{reg})/2$, which in many cases should be less than the original T_{clk}. For the interleaved case, the additional throughput can be traded for lower power dissipation if the overhead of the half-speed registers and the multiplexer is less than the gain obtained with voltage scaling.



d) Pipelined and interleaved circuit:



The new critical path will limit the period to an even shorter $T_{ip} \geq (T_{add}+T_{mux}+T_{reg})/2$. This will allow the additional throughput over the earlier cases to be traded for lower power dissipation if the overhead of the twelve half-speed registers and the multiplexer is less than the gain due to voltage scaling.