Linköping Institute of Technology
Department of Electrical Engineering, Integrated Circuits and Systems

Exam TEN1 in TSTE85 Low Power Electronics

Time:	Thursday 25 April 2019, 14:00–18:00
Place:	TER2
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aids:	Calculator and appended formula page
Instructions:	Maximum score is 70 p and minimum score to pass is 30 p
Solutions:	Posted on the course web page
Grades:	Posted through LADOK by Tuesday 14 May 2019
Display:	Time and place will be posted with the grades

1.

a) Describe how the following software strategies can be used to obtain a low power system: *transition strategies, load-change strategies, adaptation strategies*. (3 p)

b) Propose some ways to obtain power efficient analog circuits. (3 p)

c) There is a need of large-value, high-quality inductors in RF circuits. Why is it more power efficient to use an on-chip inductor compared with an external? (2 p)

d) Explain the different contributions to the power dissipation in CMOS circuits. (6 p)

e) Interleaving and pipelining can be used to reduce the power consumption if we are allowed to reduce the power supply voltage. What are the advantages and drawbacks with respective method? (4 p)

2. Consider an ideal three-input NAND gate with independent and uniformly random inputs (a, b, c). What input probabilities $P(a=1)=P(b=1)=P(c=1)$ would cause the highest transition activity at the output? Motivate your answer. (6 p)

3. Consider a digital circuit where the clock is gated with a simple AND gate. The operation of this circuit will then be sensitive with respect to the timing of the inputs of the AND gate. Make a sketch of the waveforms of the input and output of the AND gate where you point out and explain what timing violations that likely would cause problems in the digital circuit. (4 p)

4. The NMOSFET in the CMOS inverter shown in Figure 1 below draws the subthreshold current $0.6e^{-21|V_{GT}|}$ µA from the supply at room temperature when V_{DD} = 1 V, V_{SBn} = 0 V and V_{Tn} = 0.3 V. Channel length modulation is neglected.

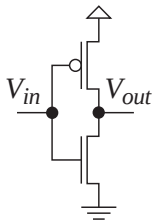

Figure 1. CMOS inverter.

a) What is the subthreshold slope S of the NMOSFET? (4 p)

b) How much relative power would be saved if V_T is increased to 0.4 V? (4 p)

c) Suggest a method to increase V_T. (2 p)

5. The signal flow graph in Figure 2 has the minimal sample period $T_{min} = t_{add} + t_{mul}$. Propagation delays t_{add} and t_{mul} are 0.5 ns for the adders and 1.2 ns for the multipliers, respectively. Delays of registers are neglected.

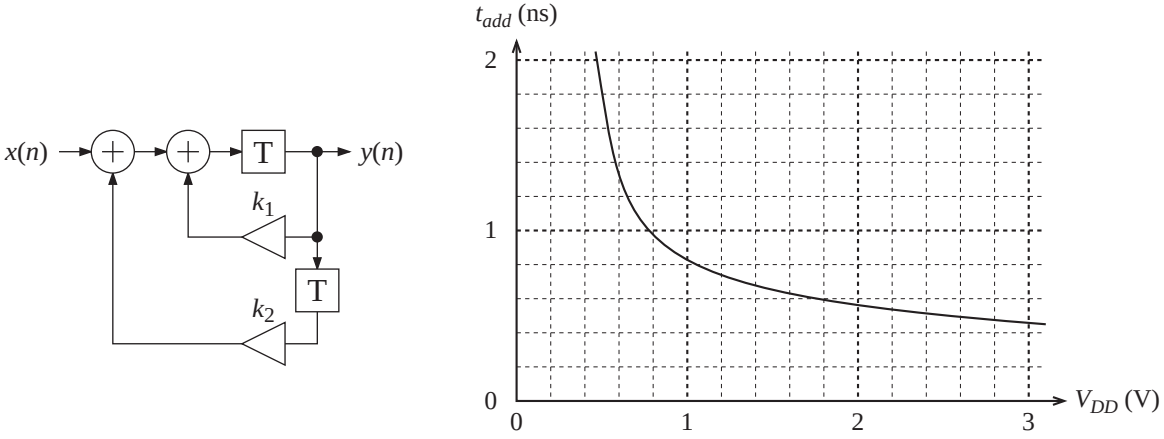

Figure 2. Signal flow graph and $t_{add}(V_{DD})$.

a) What is the critical path for this signal flow graph? (2 p)

b) Retime the delay elements to achieve the theoretical minimal sample period. (4 p)

c) Assume that propagation delay of the multipliers scales in proportion to the adders with a voltage change. What is the relative saving in dynamic power consumption if the retimed algorithm is used and its supply voltage is scaled to maintain the original throughput? Neglect glitches. (4 p)

6. Order the energy harvesting devices below from low to high power generation efficiency.
   A. RF receiver in proximity to WiFi transmitter
   B. Thermoelectric generator attached to human
   C. Thermoelectric generator attached to hot machine
   D. Indoor solar cell
   E. Outdoor solar cell
   F. Solar cell in office (4 p)

7. A FIFO (First In First Out) register of word length of 48 bits and a depth of 24 should be designed.

a) How many registers are needed if no interleaving is used? (2 p)

b) How many registers are needed if the FIFO register is interleaved with the use of two data paths? Sketch the circuit. (2 p)

c) How much power can be saved in the registers in part b) compared with part a) using voltage scaling? Assume $r = 1.5$ and that the original FIFO works properly with a power supply voltage of 1.2 V (V_T = 0.30 V). Neglect delay and power dissipation of the multiplexer required for the interleaving. (4 p)

8. Two unsigned three-bit binary numbers $A = \langle a_2 a_1 a_0 \rangle$ and $B = \langle b_2 b_1 b_0 \rangle$ should be compared as $f = A \geq B$. a_2 and b_2 are the MSBs, and a_0 and b_0 are the LSBs. A straightforward comparator can be designed by adding the two's complement value of B to A, and using the carry output from the MSB position as the result. Since we are not interested in the subtractor output, it is sufficient to only compute the carries, e.g. with the equations shown below.

$$c_0 = 1 \qquad \text{(1 LSB is added for two's complement)}$$

$$c_1 = a_0 \overline{b_0} + c_0 \left(a_0 + \overline{b_0} \right) \qquad \text{(inversions of } b_i \text{ are needed for one's complement)}$$

$$c_2 = a_1 \overline{b_1} + c_1 \left(a_1 + \overline{b_1} \right)$$

$$c_3 = a_2 \overline{b_2} + c_2 \left(a_2 + \overline{b_2} \right)$$

$$f = c_3$$

The task is to design a complete-disabling precomputed comparator.

a) Compute the Observability Don't Care set for $f = c_3(a_2, b_2, c_2)$ with respect to c_2. (5 p)

b) Use the Observability Don't Care set to realize the precomputed comparator. (5 p)

TSTE85 FORMULAS

Circuits

Transition activity $\alpha = \alpha_{01} + \alpha_{10} = 2\alpha_{01} = 2\alpha_{10}$

Switch activity $a = \sum_i \alpha_{01,i} C_i \Big/ \sum_i C_i$

Switched capacitance $C_{sw} = a \sum_i C_i$

Dynamic power consumption $P_d = f_{clk} C_{sw} V_{pp} V_{DD}$

Short-circuit power consumption $P_{sc} = a f_{clk} t_{sc} I_{peak} V_{DD}$

Propagation time $t_p \propto V_{DD} \Big/ \left(V_{DD} - V_T\right)^r$, $1 \le r \le 2$

MOSFETs

Threshold voltage $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$

Weak inversion ($V_{GT} < 0$) $I_D = I_{D0}\left(W/L\right) e^{-\left|V_{GT}\right| / \left(n_s V_\Theta\right)} \left(1 + \lambda V_{DS}\right)$

where

$V_\Theta \approx 26$ mV @ $T = 300$ K

n_s can be calculated from $S = n_s V_\Theta \ln(10)$

Strong inversion ($V_{GT} \geq 0$) $I_D = k'\left(W/L\right) V_{min} \left(\left|V_{GT}\right| - V_{min}/2\right)\left(1 + \lambda V_{DS}\right)$

where

$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$ (corresponding to *saturation*, *resistive*, and *velocity saturation* modes)

Gate-oxide leakage $I_G = k_1 W \left(V_{ox}/t_{ox}\right)^2 e^{-k_2 t_{ox}/V_{ox}}$

Logic

Shannon's expansion theorem $\overline{f\left(x,\, y,\, z,\, \ldots,\, +,\, \cdot\right)} = f\left(\bar{x},\, \bar{y},\, \bar{z},\, \ldots,\, \cdot,\, +\right)$

Cofactors $f_{\bar{x}} = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=0}$, $f_x = f\left(x,\, y,\, z,\, \ldots\right)\Big|_{x=1}$

Expansion in sum and product $f\left(x,\, y,\, z,\, \ldots\right) = \bar{x} \cdot f_{\bar{x}} + x \cdot f_x = \left(x + f_{\bar{x}}\right)\left(\bar{x} + f_x\right)$

Observability Don't Care set $\mathrm{ODC}_x = f_{\bar{x}} f_x + \overline{f_{\bar{x}}}\,\overline{f_x}$