Gate delay vs. supply voltage

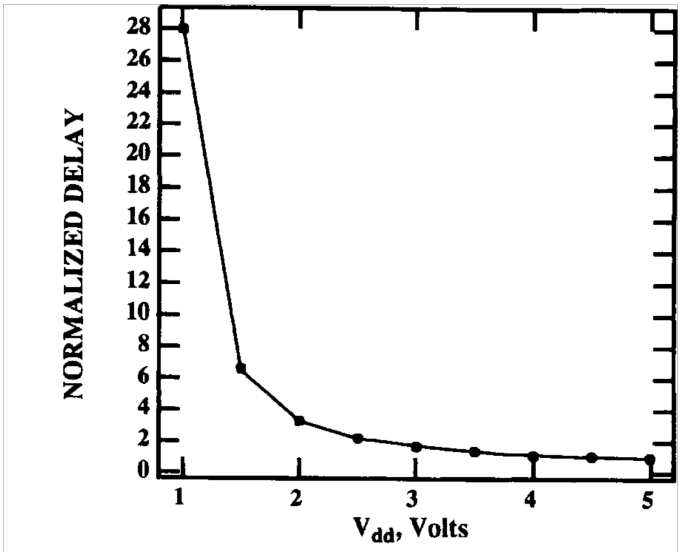
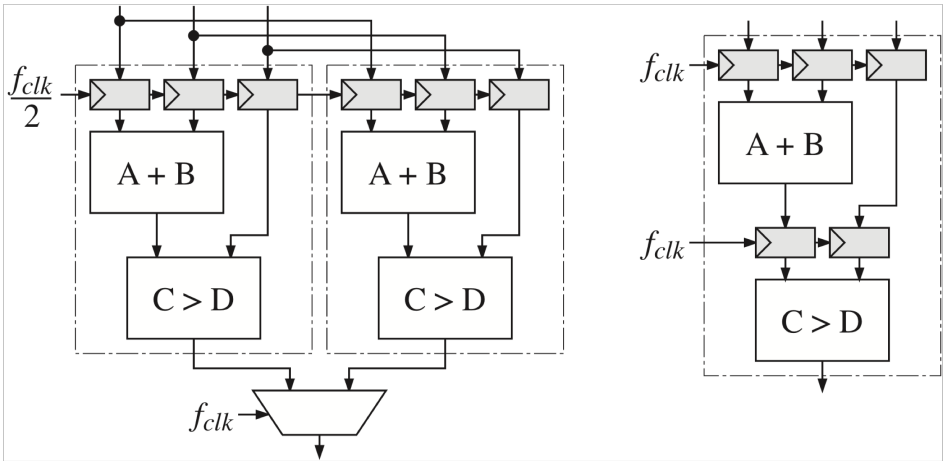


Fig. 7. Normalized delay versus V_{dd} for a typical gate in a standard CMOS process.

Supply voltage scaling



Parallel

Pipeline

Example on supply voltage scaling

- Double throughput $\Rightarrow$ $V'_{DD} \approx 0.58\ V_{DD}$
- Increased capacitance $\Rightarrow$ $C_{par} \approx 2.15\ C$
  $C_{pipe} \approx 1.15\ C$

Architecture	V'_{DD} [V]	Norm. area	Norm. power
Original	5	1	1
Parallel	2.9	3.4	0.36
Pipeline	2.9	1.3	0.39
Pipeline-parallel	2	3.7	0.2

Reference

03.pdf **Minimizing power consumption in digital CMOS circuits**

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