TSTE85 Low Power Electronics

Course responsible and teacher

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Course home page

http://www.isy.liu.se/edu/kurs/TSTE85/

Course material

Collection of journal papers, Exercise problems, Lab-PM, Project assignment

Lectures and lessons

Lectures 12 x 2h/exercises 12 x 2h

1 — Introduction
2 — System level
3 — Algorithm level
4 — Architecture level
5 — Register transfer level
6 — Logic level
7 — Circuit level
8 — Synchronization
9 — Low power components
10 — Special techniques
11 — Analog circuits *(Guest lecturer: J Jacob Wikner)*
12 — RF circuits *(Guest lecturer: Ted Johansson)*

Laboratory and project work

Laboratory work 2 x 4h

1 — Power estimation using Design Analyzer – tutorial

2 — FIFO lab – Nanosim tutorial

Project

Low power design of a high-speed parallel multiplier

Grading

UPG1 Project work 1.5 p

TEN1 Written exam 4.5 p

Outline of today's lecture

- History and motivation
- Current trends
- Sources of power dissipation
- Limits on power dissipation

History of low power electronics

- 1947
  - Invention of the transistor
- 1958
  - Invention of the integrated circuit
- Historical motivation for low power electronics
  - Need for portable battery equipment such as
    - wrist watches
    - pocket calculators
    - cell phones
    - hearing aids
    - pacemakers
    - military equipment

Development of low power principles

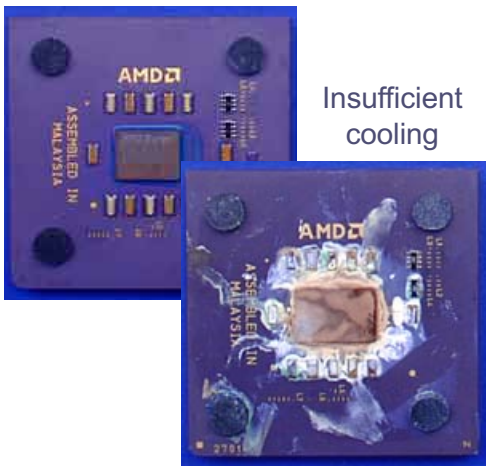
- 60's
  - Use lowest V_{DD} possible
  - Prefer analog solutions to avoid high standby I of logic
  - Choose technology with small geometry and large f_T, and scale I
  - Use extra electronics to reduce total I
  - Specify system performance carefully and optimize on all levels
- 70's
  - Power management
- 80's
  - Shift from bipolar to CMOS technology

Motivation for low-power design

- Stationary equipment
  - Cooling costs
  - Packaging costs
- Costs
  - +10 °C ⇒ double failure rate
- Portable equipment
  - Long battery life
  - Low battery weight
  - Li-Ion:
    - ~150 Wh/kg
    - ~500 Wh/L

Power constraints

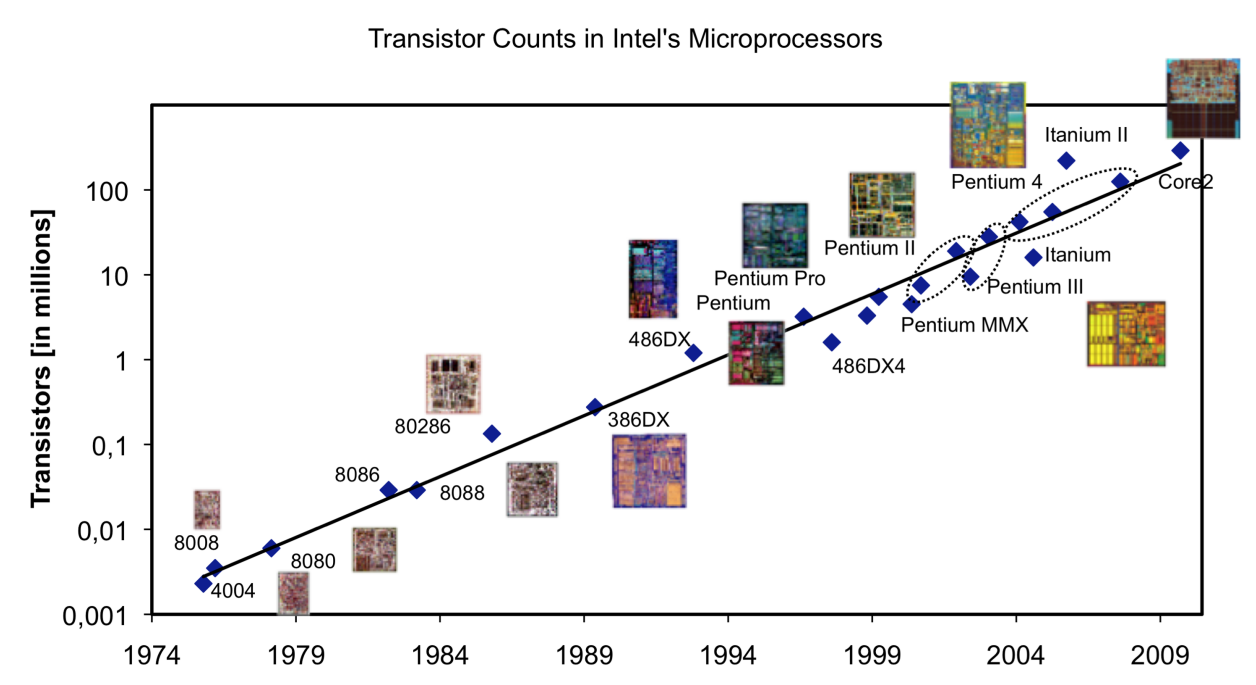
- Average power
  - cooling
  - packaging
  - battery life
- Peak power
  - electrical limits
  - distribution network
  - battery type
  - signal integrity: voltage drops from
    - *R i*
    - *L di/dt*



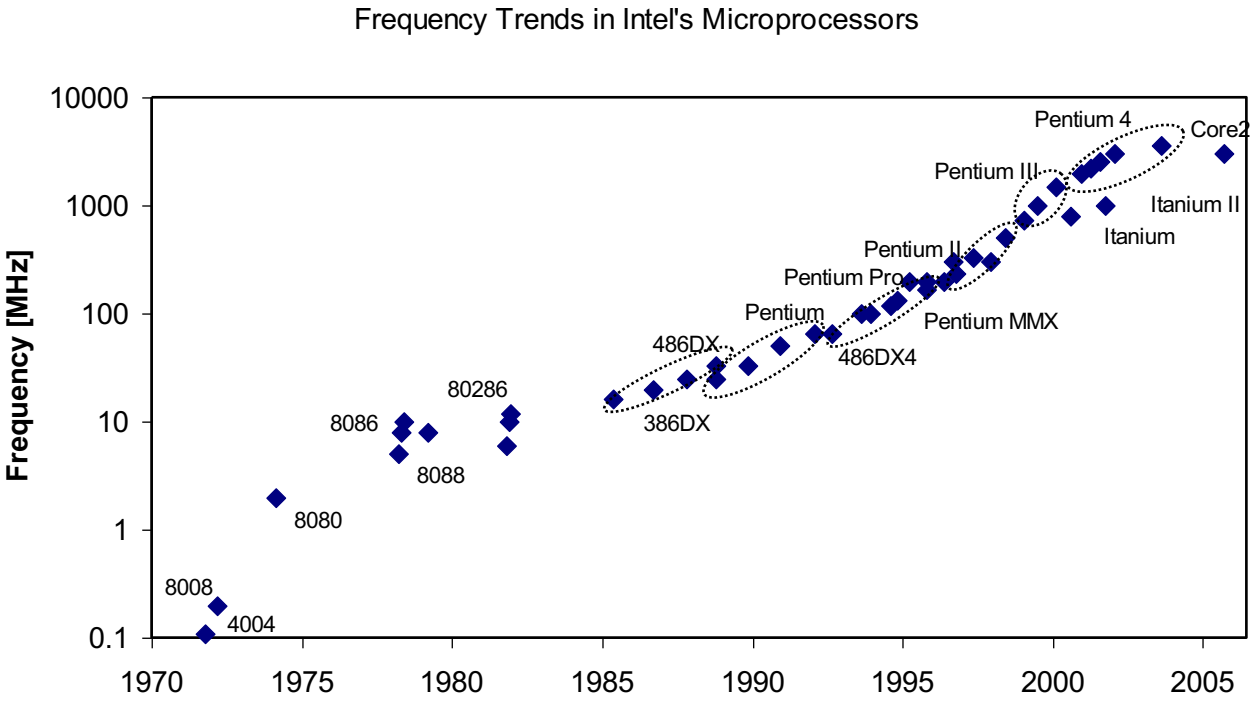
Insufficient cooling

*Pictures from http://www.tomshardware.com/2001/09/17/hot_spot/

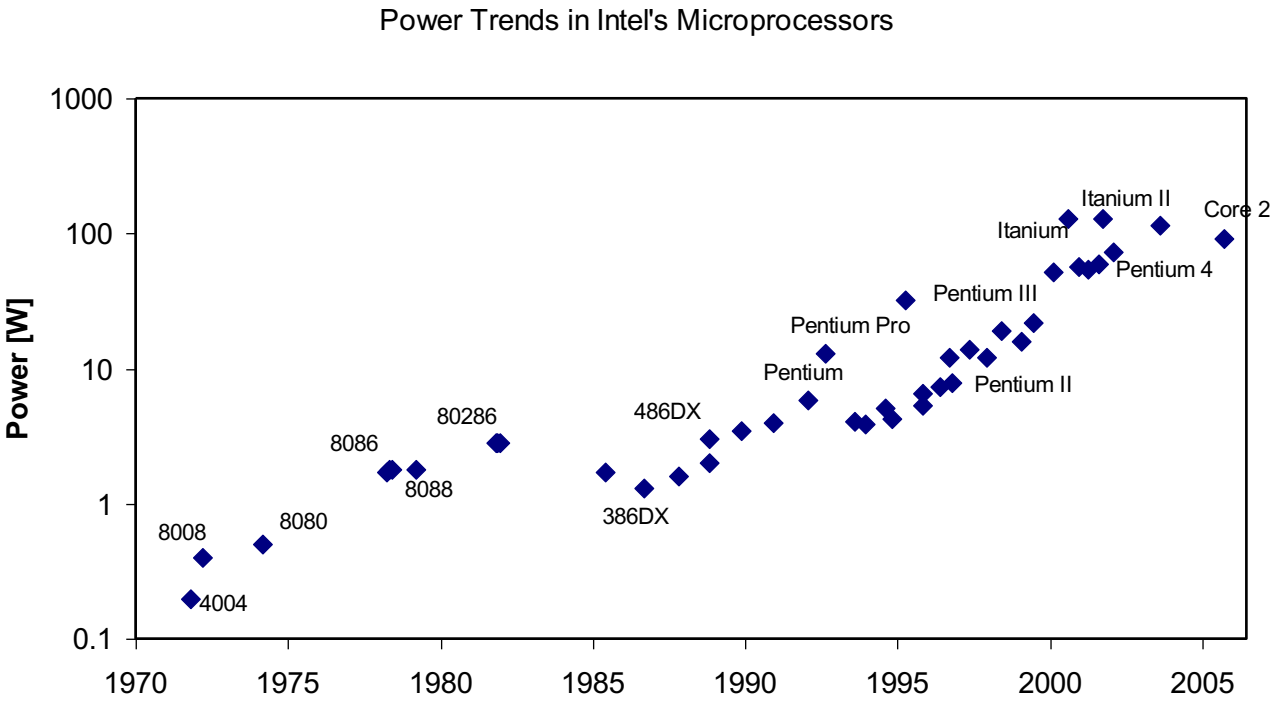
Trend in transistor count



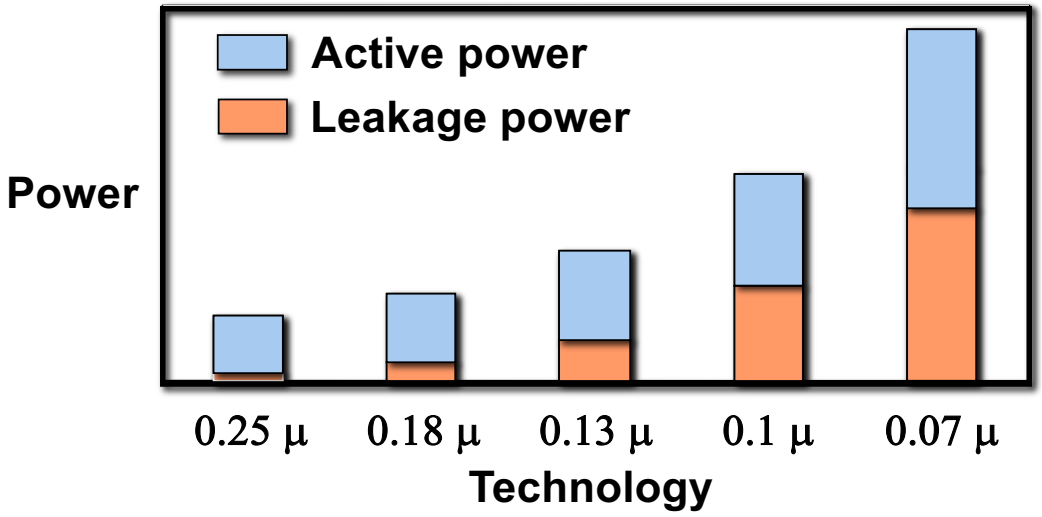
Trend in clock frequency



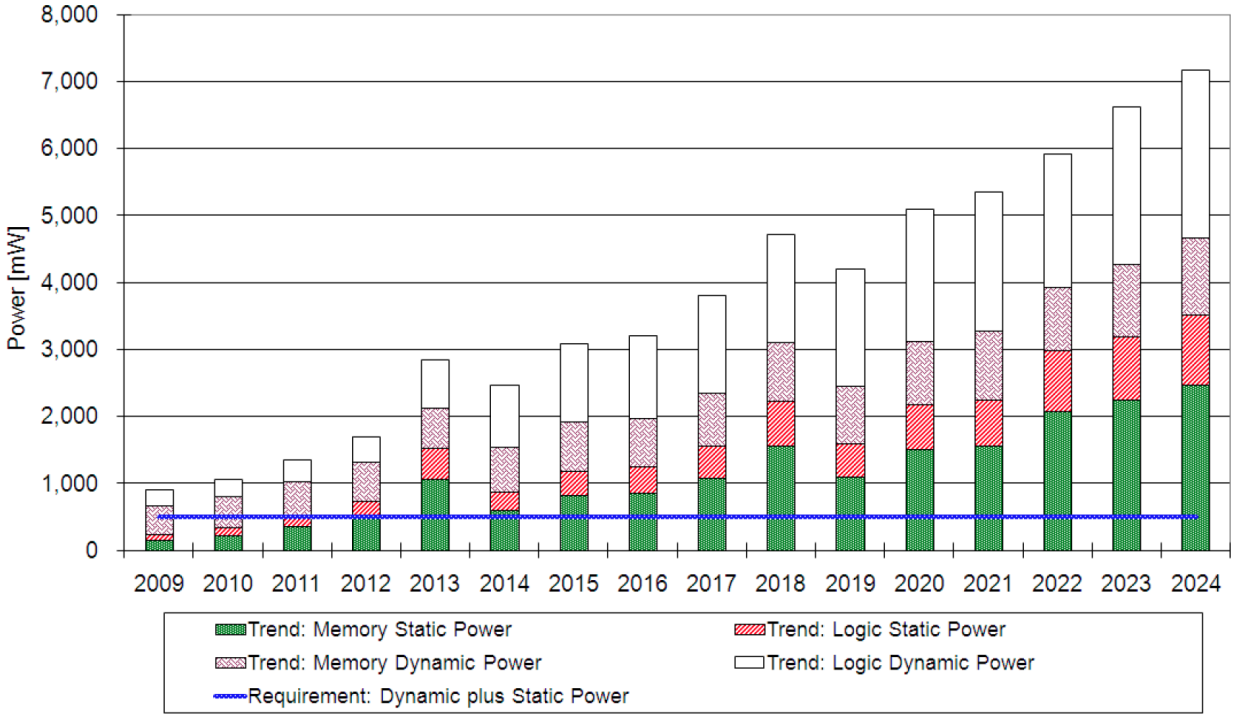
Trend in power dissipation



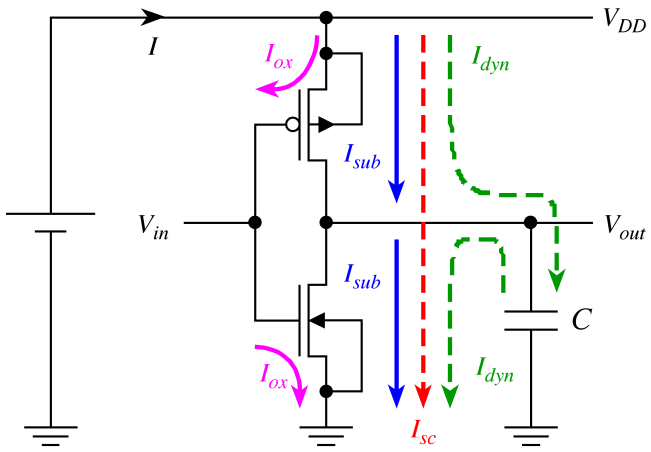
Trend in leakage power



Trend in portable power dissipation [*ITRS* 2010]



Power dissipation in CMOS circuits



	Dynamic dissipation		Static dissipation
	Logic transitions	Short-circuit dissipation	Leakage
P_{total} =	P_{switch} +	$P_{short\text{-}circuit}$ +	$P_{leakage}$

Power limits

Hierarchical Matrix of Limits

	Theoretical	Practical
5. System		
4. Circuit		
3. Device		
2. Material		
1. Fundamental		

Fig. 1. Hierarchical matrix of limits on GSI.

Fundamental power limits

- Limits derived from basic principles of
  - Thermodynamics
  - Quantum mechanics
  - Electromagnetics

Fundamental limits on power and delay

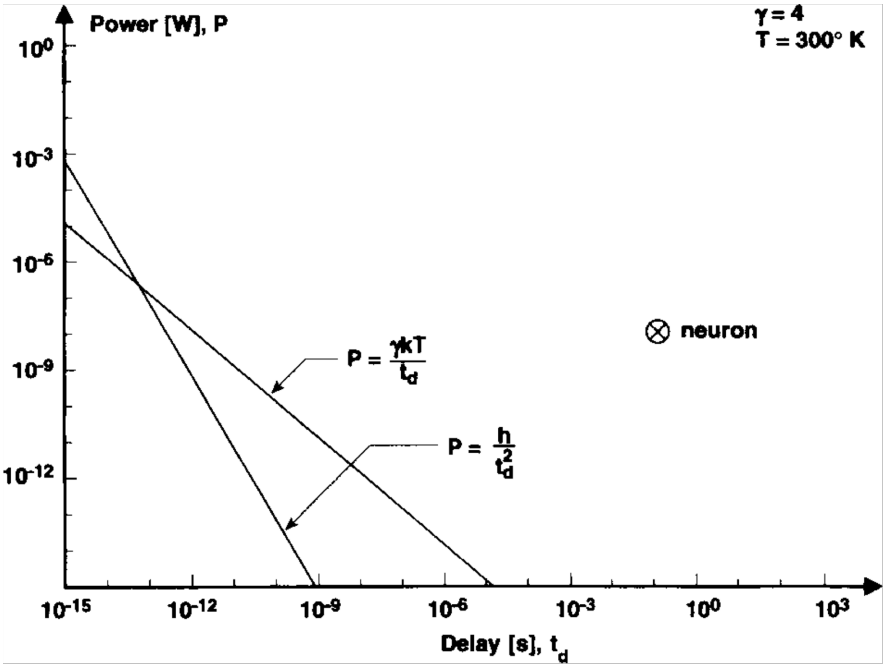
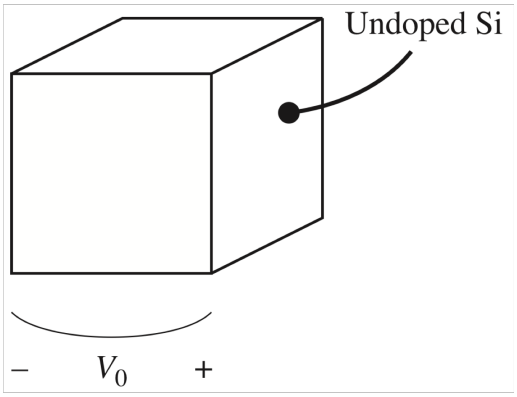


Fig. 6.

Material limits

- Semiconductor
  - Electrostatic energy



V_0 = 1.0 V $\Rightarrow$ min switching t_{Si} = 0.33 ps
t_{GaAs} = 0.25 ps

- Interconnect
  - Speed of light

$$t_d \geq \frac{L}{c_0 / \sqrt{\varepsilon_r}}$$

Material limits

- Thermal conductivity

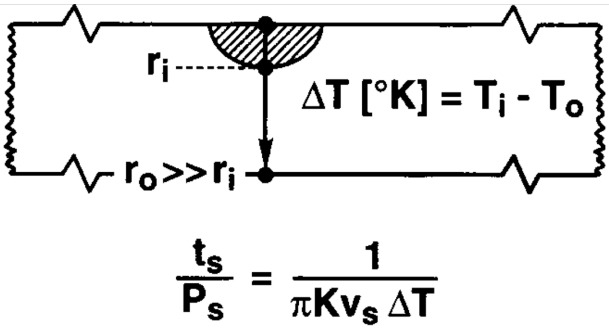


Fig. 10. Model for derivation of material limit based on heat conduction.

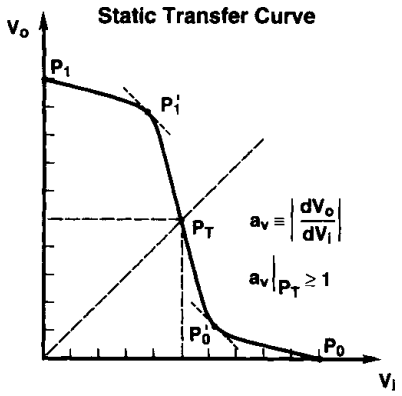
$\Delta T = 100$ K $\Rightarrow$ $(t/P)_{Si} = 0.21$ ns/W
$(t/P)_{GaAs} = 0.69$ ns/W

Device limits

- Allowable minimum effective channel length of a MOSFET
  - Problems with decreasing V_T
  - Determines switching energy limit
- *RC* product in interconnect

Circuit limits

- Limits on MOSFET gate and supply voltage □
  - Minimum circuit switching energy/transition (ring oscillator)
  - Limits on driving interconnect



$$V_{DD} \geq \frac{\gamma kT}{q}$$

$$T = 300\,\mathrm{K} \Rightarrow V_{min} \approx 0.1\,\mathrm{V}$$

(Note that $V_{DD} \approx 0.1$ V would cause excessive leakage)

Fig. 16. Static transfer characteristic of a nonideal CMOS inverter.

System limits

- Chip architecture
- Power-delay product of the CMOS technology
- Heat removal capacity of package
- Clock frequency
- Physical size

References

01.pdf **Low power microelectronics: retrospect and prospect**

J.D. Meindl

Proceedings of the IEEE, volume 83, issue 4, April 1995, pages 619-635

[ITRS10] **International Technology Roadmap for Semiconductors**

www.itrs.net