Lab 3 Power electronics

Contents

Introduction

This lab focus on operation and measurements on MOSFET based full-bridge PWM inverter. The inverter, which is implemented on a dedicated PCB (Printed Circuit

Board), will be controlled through a program in LabVIEW using signal interface through the ELVIS prototyping board.

The target is to get “hands on” experience of a power electronic circuit where you after the lab:

- shall be able to identify the main components on the inverter unit
- understand the basic sub-circuits and its functionality
- understand and define the control parameters for the inverter PWM.

Initial setup

The LabVIEW files and other files used in the lab can be copied from **/site/edu/eks/TSTE19/current/material/Lab3_files** in Linux or from **U:\eks\ TSTE19\current\ material\Lab3_files** in Windows. Put the copied files into your home directory, for example in /edu/<userid>/TSTE19/ on Linux or H:\TSTE19 on Windows.
Please note that the software only works on Windows. You can thus only run the software in the Transistorn lab.

Verifying correct LabVIEW interface with ELVIS

Before loading the LabVIEW interface we need to check the ELVIS device number related to the specific setup on your Lab computer. Start the NI Elvis Instrument Launcher found through Start ->All Programs ->National Instruments ->NI ELVIS mx for NI Elvis -> NI Elvis Instrument Launcher

1. Turn-on the main power to the ELVIS board using switch (1), Figure 1.
2. Start the Digital Multimeter.
3. Check the ELVIS device number shown in the drop down menu in the lower left of the Digital Multimeter, Figure 2.

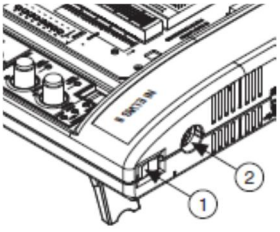

Figure 1 ELVIS main power switch

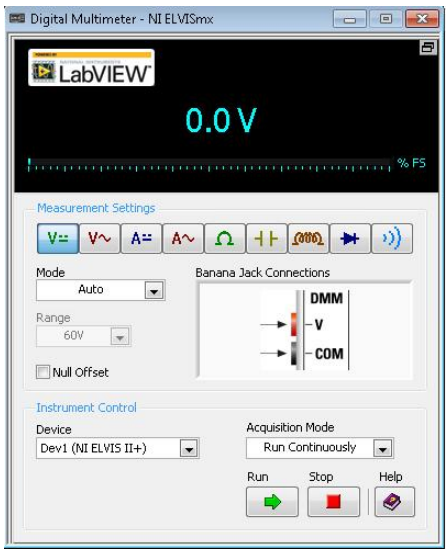

Figure 2 ELVIS device number

Starting the LabVIEW software

The software is started by **Start ->All Programs ->National Instruments ->LabVIEW 2015 ->LabVIEW 2015**
The windows shown below will appear, where you shall load the LabVIEW project file from your home directory using the **Open Existing** button.

Depending on the ELVIS device number in your setup, you shall load the corresponding LabVIEW project file. This found by the end of the file name.

Open the file: **FB_Inv_Lab3_dev7** (if your ELVIS has device no 7)

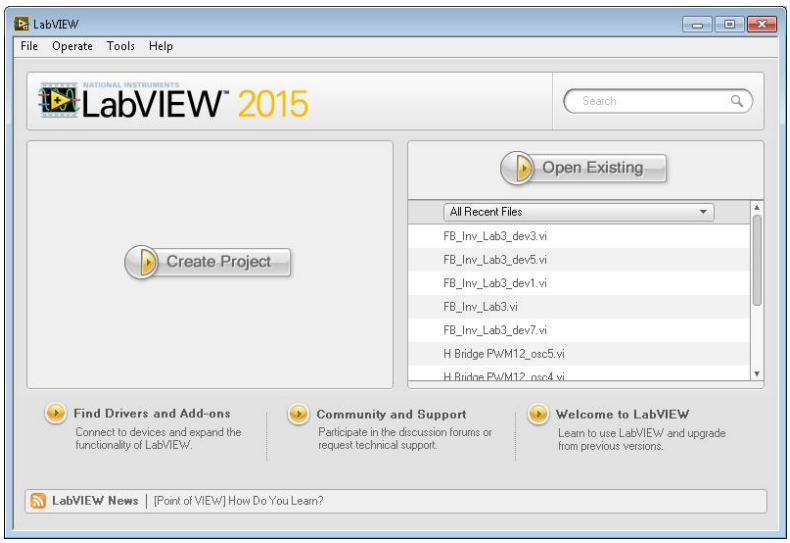

Figure 3 LabVIEW startup window

When the project file is loaded the control interface of the Full-bridge inverter will appear as shown Figure 4.

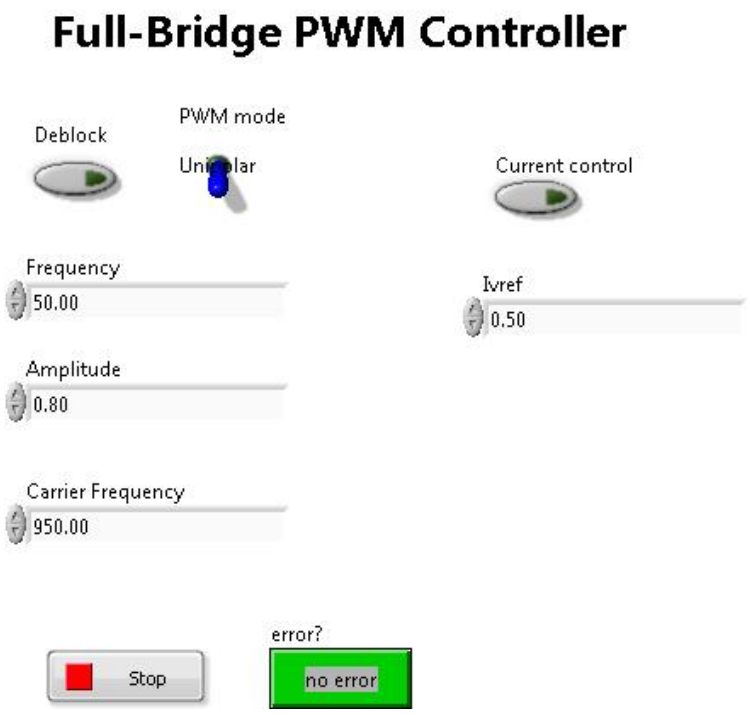

Figure 4 LabVIEW control interface to the FB-Inverter.

LabVIEW FB-Inverter control interface

The purpose of the LabVIEW program is to provide user interface and the PWM control resulting in the 4 gate signals to the FB-Inverter board. The PWM control can either be setup with a fixed voltage reference or based on feedback load current control. The program will also provide the measurement interface for the eight analog signals from the inverter board. An overview of the whole program is presented in Figure 5.

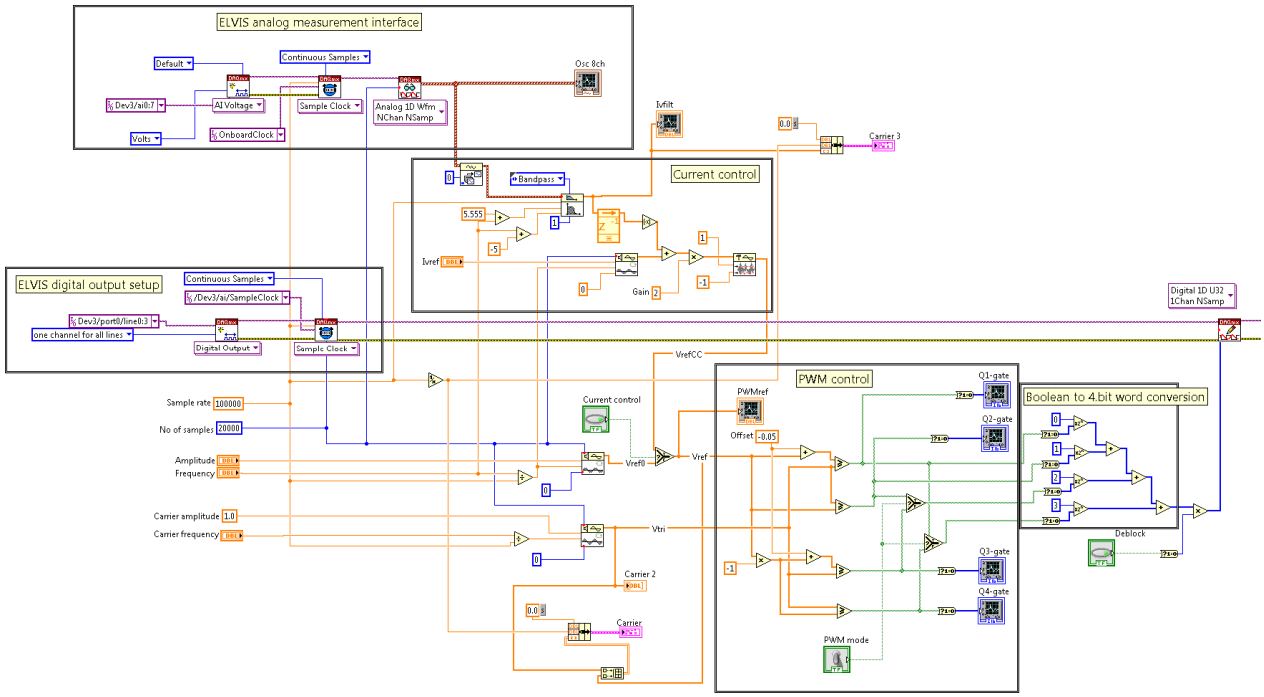

Figure 5 LabVIEW FB-Inverter control interface

PWM control

A more detailed view of the PWM control part is shown below:

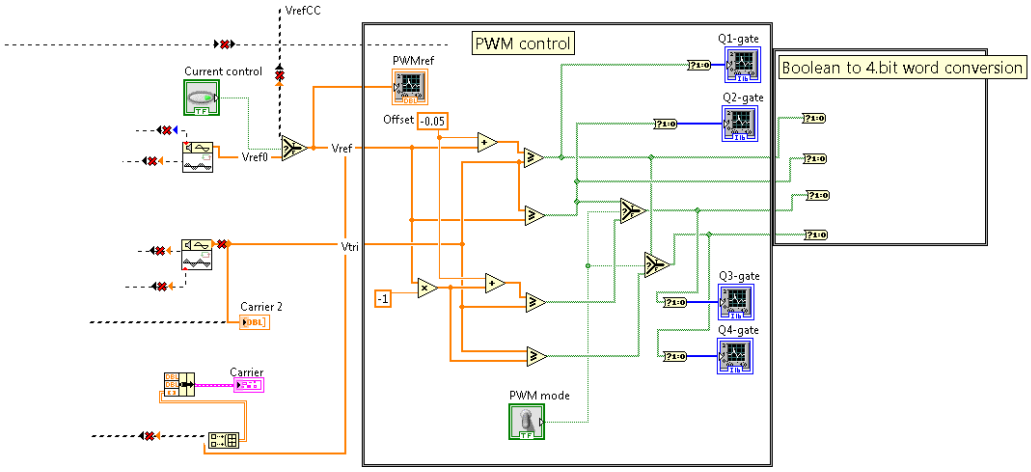

Figure 6 PWM control

The input to the PWM control are the control voltage reference (Vref) and the triangular carrier wave (Vtri). The two upper comparators defines the gate 1 and 2 signals, where an offset is included in order to provide blanking. Unipolar PWM is defined through the lower comparators based on the inverse of Vref. Bipolar PWM can be selected through the switch "PWM mode" resulting in gate 3 to be synchronized to gate 2 and gate 4 to gate 1.

The amplitude and frequency of the PWM voltage reference can be changed from the user interface. The carrier frequency can also be changed.

The gate signals are enabled by pressing the DEBLOCK-button.

The PWM results in control of the output voltage (Vop-Von) such as the magnitude is defined by the following expression.

$$\hat{V}_{op-on} = m_a(V_{dc} - \Delta V_{FB})$$

Equation 1

The actual output voltage will drop from V_{dc} by ΔV_{FB} due to the resistors R1 and R3 (see Figure 28) and the voltage drop of MOSFETs.

In Equation 1, m_a is the amplitude of the PWM reference Vref. Consequently, the output voltage is based on the references given in LabVIEW (Amplitude and Frequency) defined as:

$$V_{op-on} = Amplitude \cdot (V_{dc} - \Delta V_{FB}) \cdot \sin(2\pi \cdot Frequency)$$

PWM control details

The PWM is setup for unipolar switching where G1 and G2 corresponds to one leg of the full-bridge converter and G3 and G4 of the other. The gate pulse G1 and G2 are derived using the Vref signal while G3 and G4 referred to the inverse of Vref. Blanking time is included through an offset of -0.05 in the comparators of G1 and G3. Thereby the following expressions can be written corresponding to the gate pulse generation:

G1 = Vref-0.05 > Vtri
G2 = Vtri > Vref
G3 = -1*Vref-0.05 > Vtri
G4 = Vtri > -1*Vref

Through the addition of the negative offset to Vref for G1 a blanking interval is obtained with respect to G2. This is explained by the fact that for increasing triangle wave, the intersection with Vref will come earlier through the negative offset, resulting in G1 turn-off earlier than the G2 turn-on. The opposite applies to interval with decreasing triangle wave, where the negative offset will delay the intersection with Vref, resulting in a later G1 turn-on compared to the G2 turn-off.

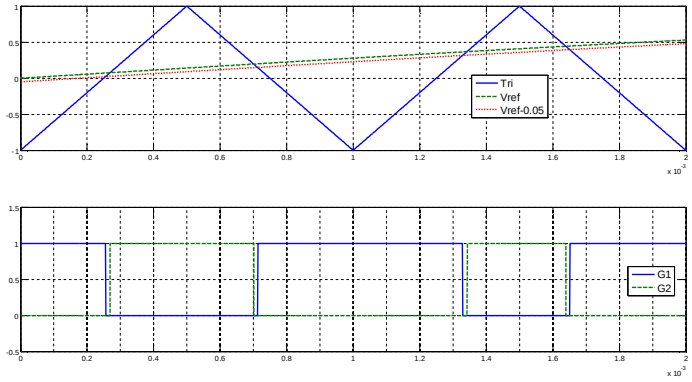

Figure 7 PWM

The blanking time obtained with the offset is defined by the rate of change of the triangle wave according to the following equation:

$$t_{blank} = \frac{|offset|}{dV_{tri}/dt} = \frac{|offset|}{4f_s}$$

For f_s = 1 kHz and an offset = -0.05 a blanking time of 12.5 µs is obtained.

Current control

By pressing the switch Current Control, the PWM voltage reference will be taken from the current control instead of the fixed reference.

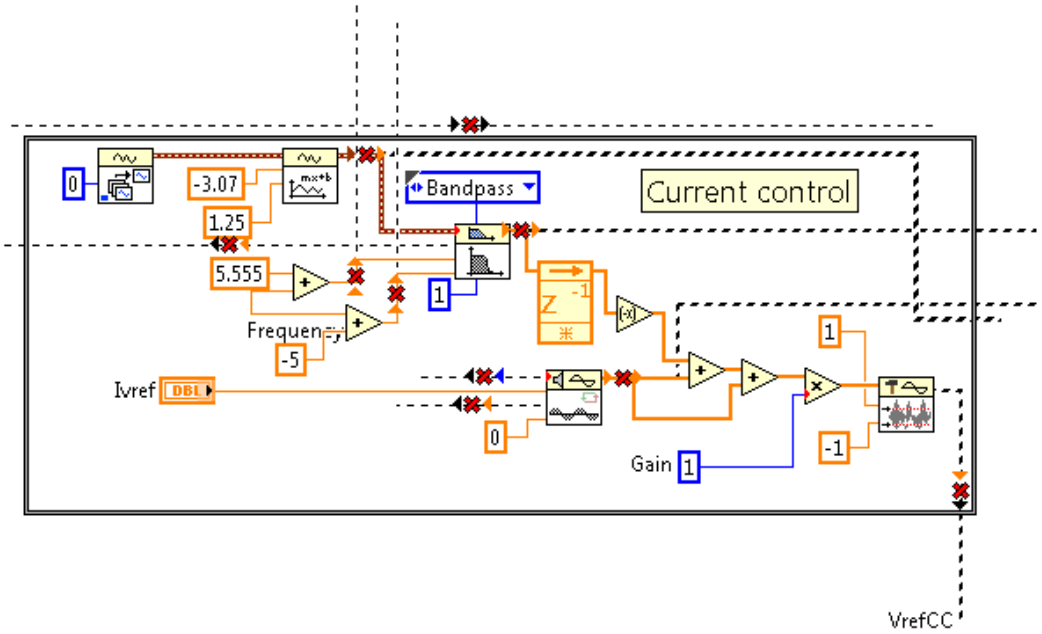

Figure 8 Current control

The current control is based on the on-board load current sense of the FB-Inverter, which is read as analog input channel 0. The measured current is filtered through a 1st order bandpass filter with a center frequency corresponding to the fundamental frequency given in the user interface. The bandpass filter is defined by upper and lower cutoff frequencies being Frequency+5.555 Hz and Frequency-5.0 Hz, respectively. The center frequency defined as $\sqrt{f_{c,hi} \cdot f_{c,lo}}$ will thereby be very close to the given Frequency.

The current control reference is a sinusoidal signal with an amplitude defined by Ivref at the user interface. The frequency is given by “Frequency”.

Current control is proportional with a gain of 1 and an output limiter between -1 and 1 in order not to cause over-modulation. Since the current controller output has an amplitude corresponding to the modulation index, a level equal to 1 gives an output voltage Feed-forward of the current reference is used corresponding to the output voltage required

Measurement interface

Eight analog signals are read from the ELVIS unit, corresponding to AI 0-7, which should be connected to the FB-Inverter, can be visualized through the LabVIEW

control interface. Description of the available analog inputs are found in sub-section "Measurement signals".

The following plots are available:

1. 8 analog inputs
2. PWM voltage ref and carrier
3. Gate pulses G1 – G4
4. Fundamental component of load current (Iv)
5. Differential signal Ux1 – Ux2
6. Fundamental component of Ux1 – Ux2
7. Load current Iv and the current reference Ivref
8. FFT spactra of Iv and Ux1-Ux2
9. Currents in Q1 and Q2
10. Measured voltages Ux3, Ux4, Ux5
11. Differential voltage Ux3-Ux4.

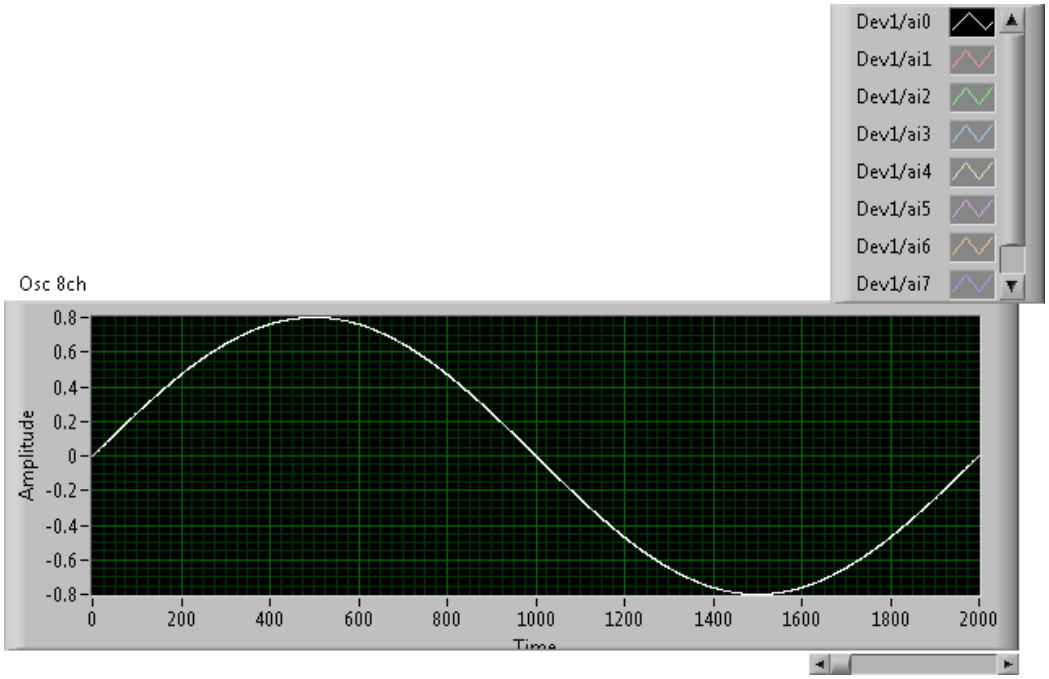

Figure 9 Analog measurement plot

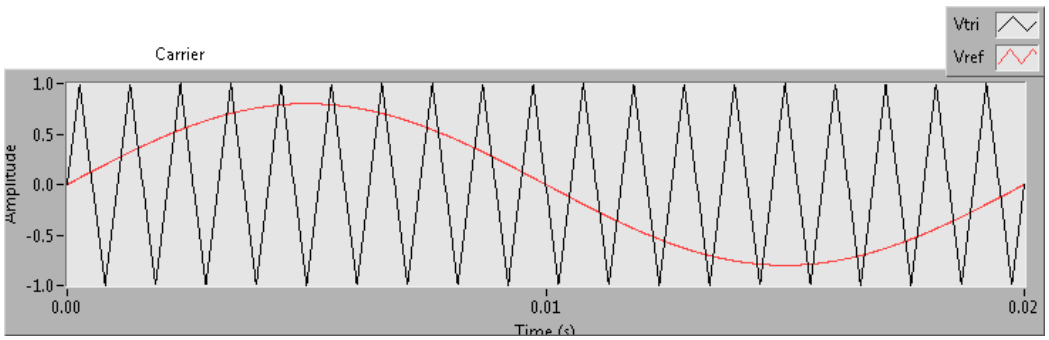

Figure 10 Plot of PWM voltage reference and carrier

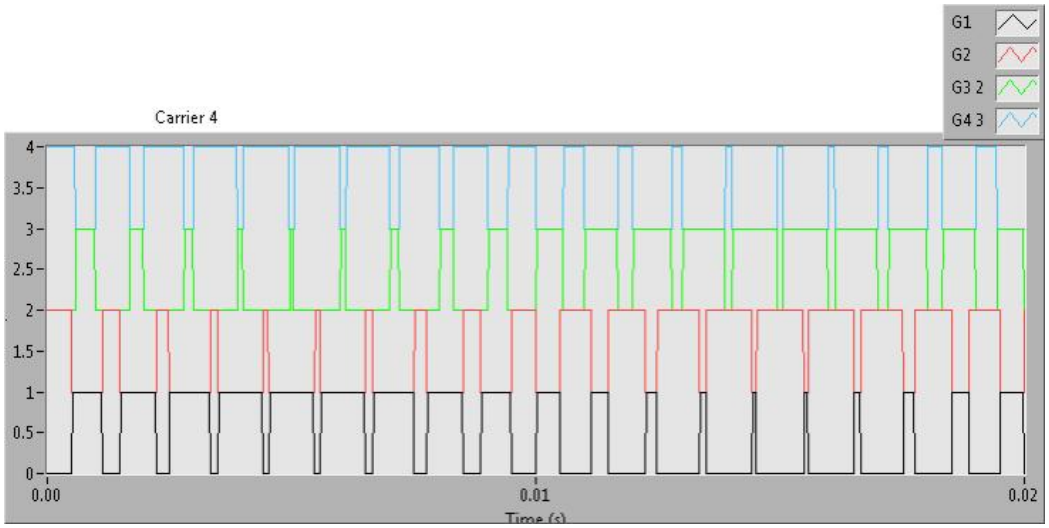

Figure 11 Plot of gate pulses

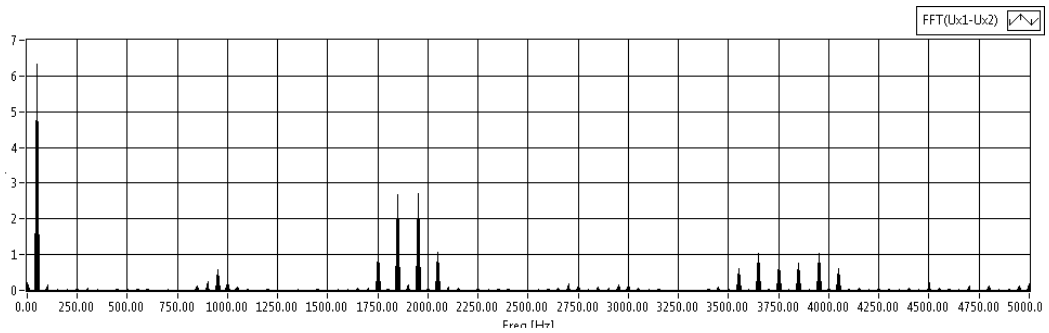

Figure 12 FFT of output voltage

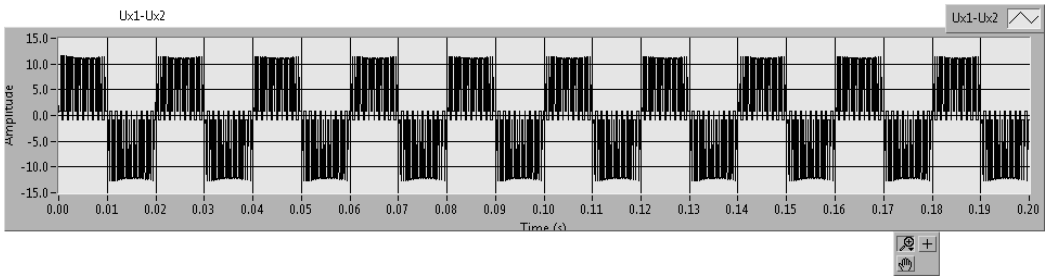

Figure 13 Plot of output voltage Uop-Uon

The graph properties such as scaling of x- and y-axis can be done by right hand clicking the graph and selecting properties. This will open the window shown below. Zooming of the graph can also be made by clicking the zoom symbol under the graph and selecting window zoom, x-zoom or y-zoom. Before making a zoom while running first disable Auto-scale by right-hand clicking the graph, and going to X-scale or Y-scale menus.

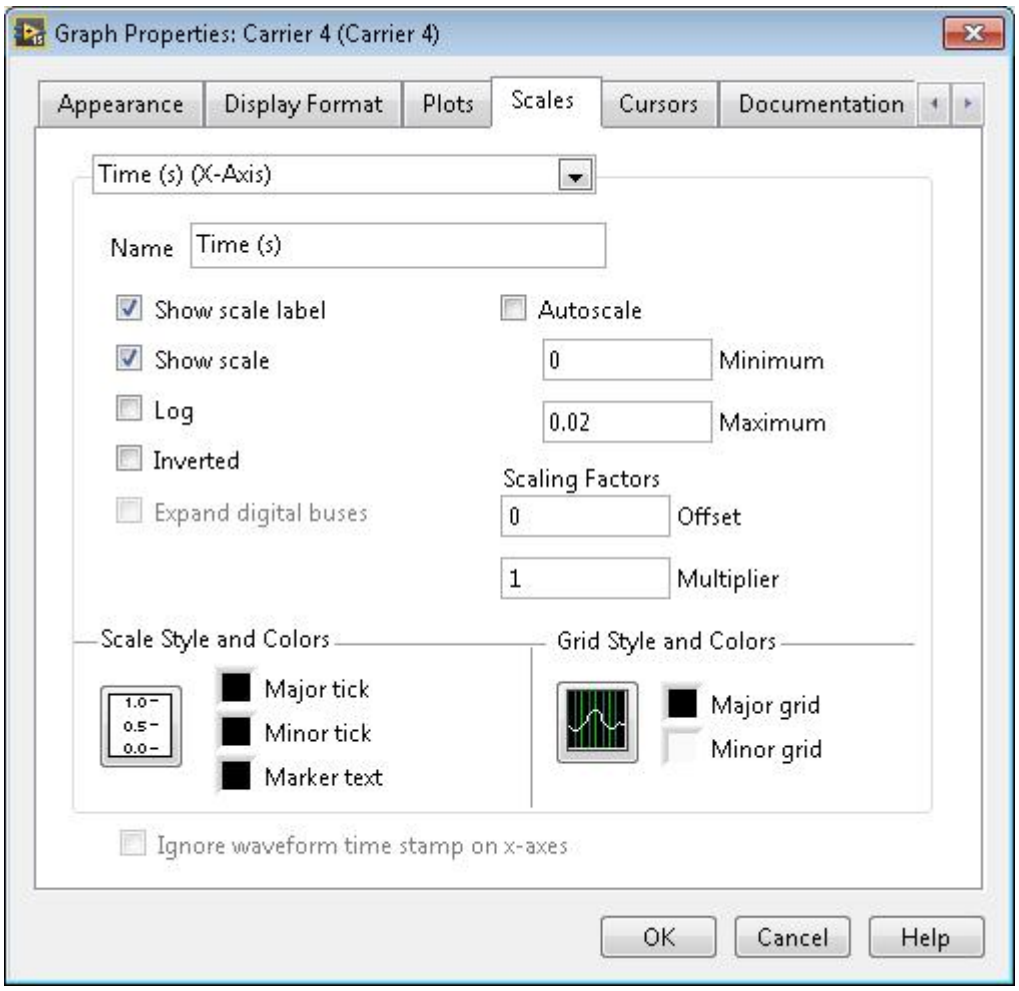

Figure 14 Graph properties window

Copying LabVIEW graphs

To copy graphs from LabVIEW to your report you shall right-hand click the graph and select Export -> Export simplified image. Then select `Bitmap` and `Export to clipboard` as shown below, before pasting into your report.

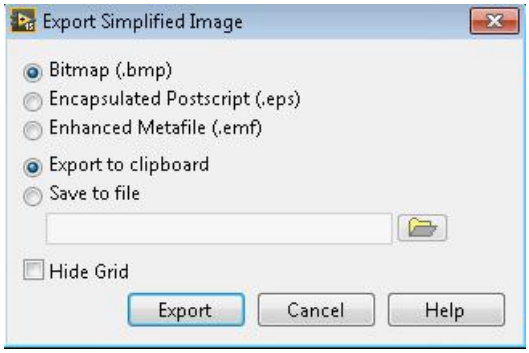

Figure 15

Full-bridge inverter board

We will here get familiarized with the design of the Full-bridge (FB) Inverter. The block diagram is presented in Figure 16, where the functional units are placed in a similar way as on the physical FB-Inverter board in Figure 17. The FB-inverter is sub-divided into the following blocks:

- Gate pulse logic (Gate pulse interlocking)
- Gate drives for Q1-Q4
- FB-Inverter core (The main FB circuit containing MOSFETs and diodes)

The functional description of the different sub-blocks is found in the corresponding sub-sections further on in this manual.

The detailed view of the FB-Inverter sub-blocks can be found through the corresponding pdf-files found in the Lab3 system folder.

The main circuit for the load current is indicated by the bold red line, starting from the positive outputs from the full-bridge (V_op), passing through the load current sense resistor R28, the external load connections (IO1 and IO2) then back through the on-board power resistor R2 to the negative output of the full-bridge (V_on). The external load connections, IO1 and IO2, are here shorted but can be used to include an external load in series with the 10 ohm power resistor.

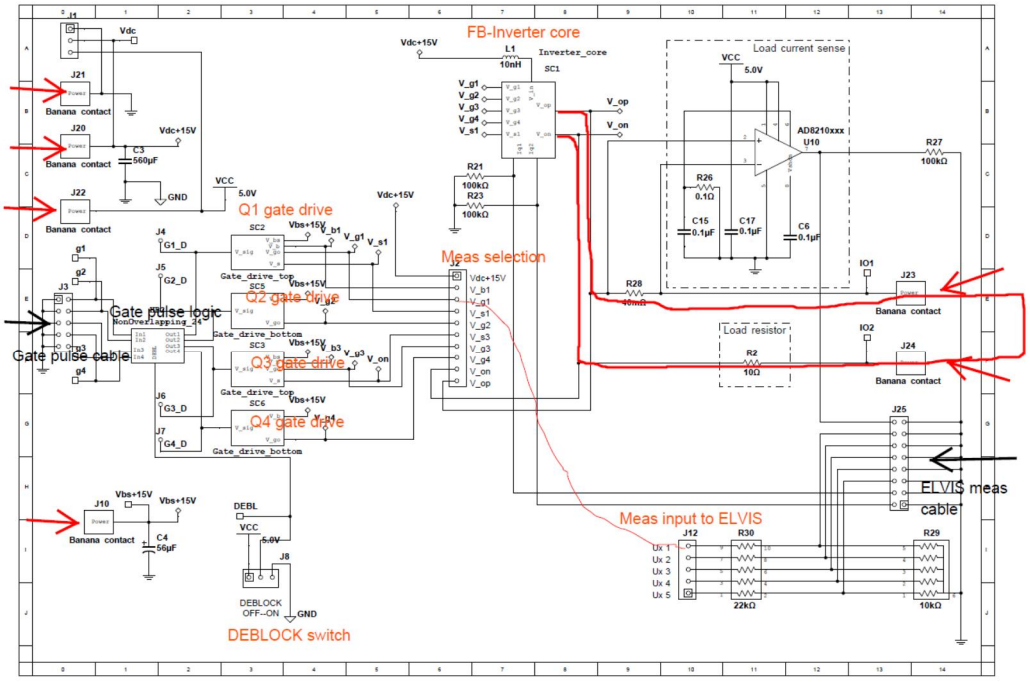

Figure 16 FB-Inverter circuit overview

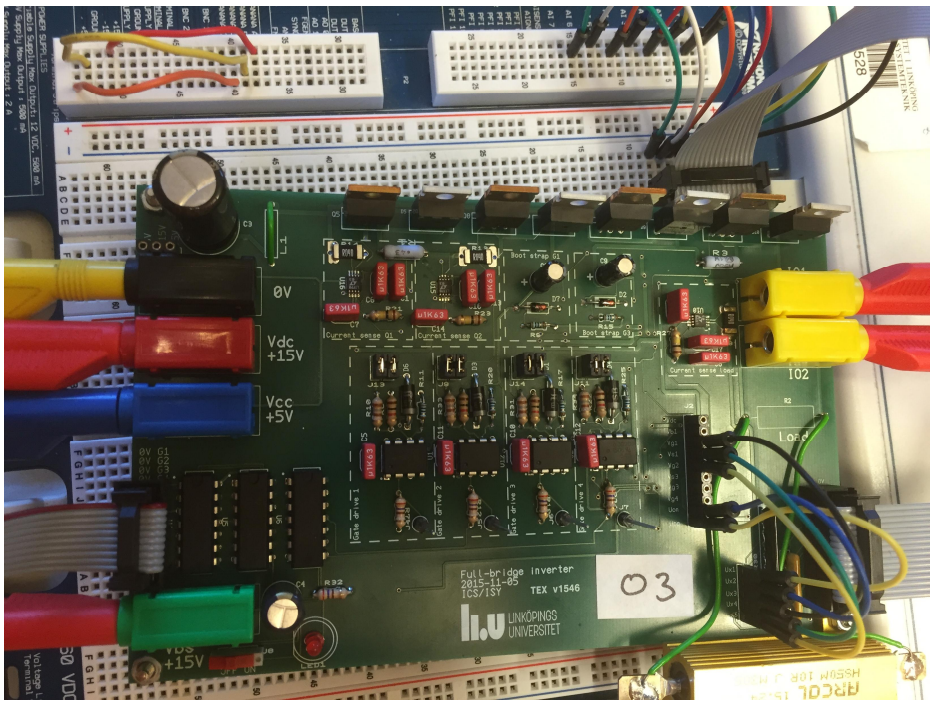

Figure 17 FB-Inverter board

Cable connections

The physical cables required for power supply and signal interface are indicated in Figure 16 by arrows. On the left hand side the 4 banana sockets for power supply connections are found. From the top:

1. 0 V (Black)
2. Vdc +15V (Red). The main dc-voltage supply to the FB-inverter.
3. Vcc +5V (Blue). Supply to digital logic circuits.
4. Vbs +15V (Green). Supply to gate drive circuits including bootstrap of Q1 and Q3

Two yellow banana sockets are located on the opposite side for connection of external load. By connecting these two, the on-board power resistor will be the sole load.

Two flat cables are required to connect gate signals to the full-bridge and to allow measurement signals to be sent back. The flat cable connectors are indicated by black arrows in Figure 16.

1. Gate signals. Left hand side connection in Figure 16 and the lower connection on the physical board (Figure 19).
2. Measurement signals. Right hand side connection in Figure 16 and the upper connection on the physical board (Figure 19).

Check the pin-header is inserted correctly in the flat cable connector according to Figure 18.

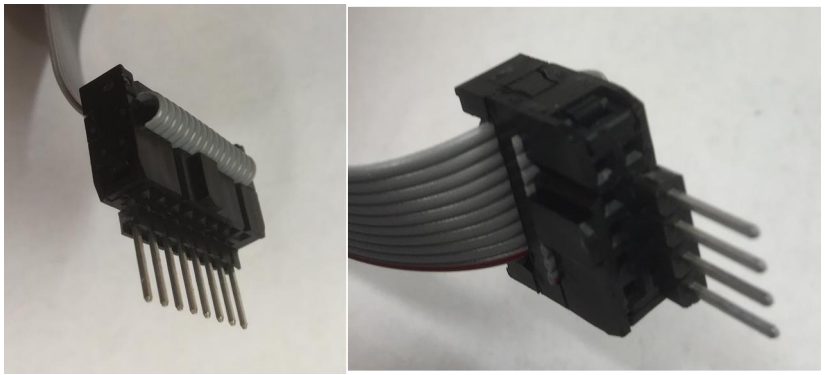

Figure 18 Flat cable pin-header location

Furthermore, there are a total of 8 measurement signals which can be used from the FB-inverter. 3 of these are dedicated to current sensing while 5 are flexible to setup by selecting among the 10 measurement points, as listed in sub-section “Measurement signals”. Selection of the 5 flexible measurement signals are done by installing wires between the corresponding point on the “Meas selection connector” and the “Meas input to ELVIS” as indicated in Figure 16.

Setting up the physical connections between the FB-Inverter unit and NI ELVIS

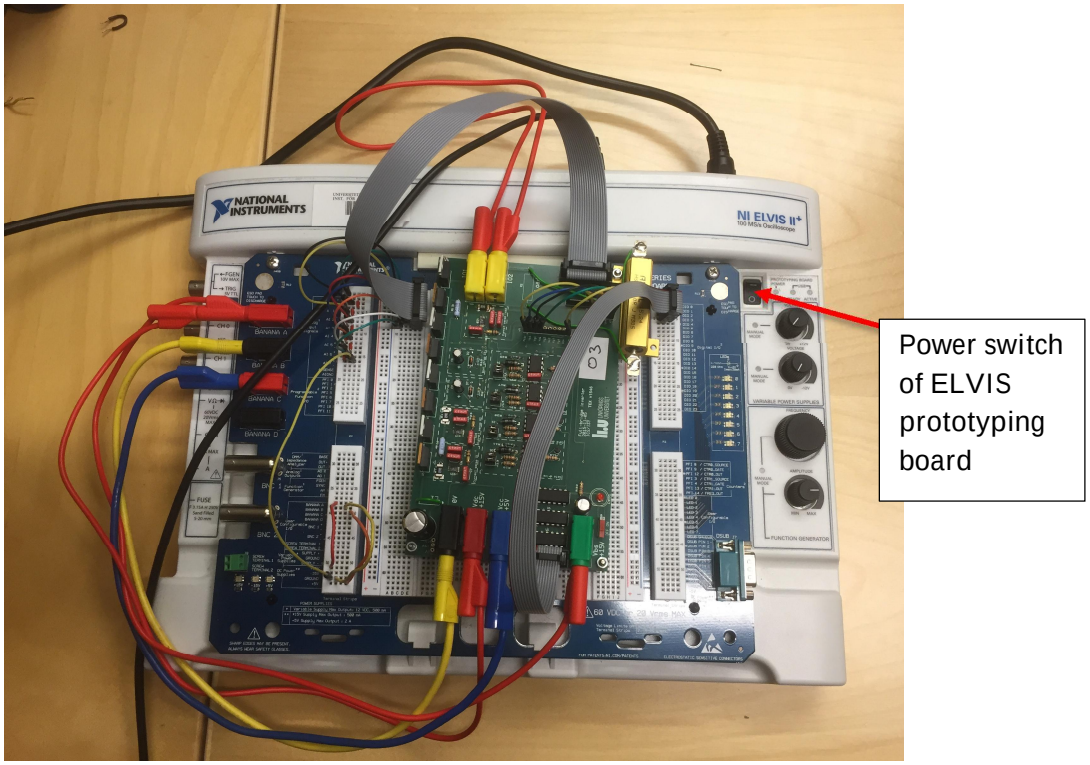

Figure 19 Physical setup of the FB-Inverter board on NI ELVIS

Follow the steps below to setup the connections to the FB-Inverter board:

1. Ensure the power switch of the ELVIS prototyping board is off.
2. Make wire connections of +15V, Ground and +5V to the Banana A, B and C connections on ELVIS (see Figure 20).
    a. Banana A (red): +15V
    b. Banana B (black): Ground
    c. Banana C (red): +5V
3. Connect the flat cable (8pole) for the analog measurements from the FB-Inverter board to the upper left part of the ELVIS prototyping board, where the 8-pin connector is plugged in order to make room for wiring according to the next step (see Figure 21). The left side of the flat cable as plugged into the board shall be facing to the top (AI 0) on the ELVIS board.
4. Make wire connections to the analog inputs the positive poles of AI0 to AI7 from the eight rows of the upper left part of the ELVIS prototyping board corresponding to the pins from the flat cable (see Figure 21).

5. Connect test leads from Banana A, B and C to the supply inputs of the FB-Inverter board for Vdc+15V, oV, Vcc+5V and Vbs+15V (see Figure 19).
    a. 0V (black): Black test lead to Banana B (black)
    b. Vdc+15V (red): Red test lead to Banana A (red)
    c. Vcc+5V (blue): Blue test lead to Banana C (red)
    d. Vbs+15V (green): Red test lead to Banana A (red)
6. Connect the flat cable (4-pole) related to gate signals to the digital I/O-port 0, DIO 0-3 in the upper right of ELVIS prototyping board (see Figure 22). The red wire in the flat cable shall be facing to the top (DIO 0) on the ELVIS board.
7. Make sure no connection is done to the two yellow Banana sockets (IO1, IO2) on the top of the FB-Inverter board. We will connect here later, after correct operation of the FB-Inverter is verified.
8. Make sure the DEBLOCK switch on the FB-Inverter board is in the OFF position.
9. Get acknowledge of correct wiring from the Lab assistant.
10. Locate the 3 supply voltage indicator LEDs on the lower left of ELVIS.
11. Switch on the ELVIS prototyping board supply.
12. Confirm all 3 supply voltage indicator LEDs are green.
13. Now the cable interface to the FB-Inverter is completed.

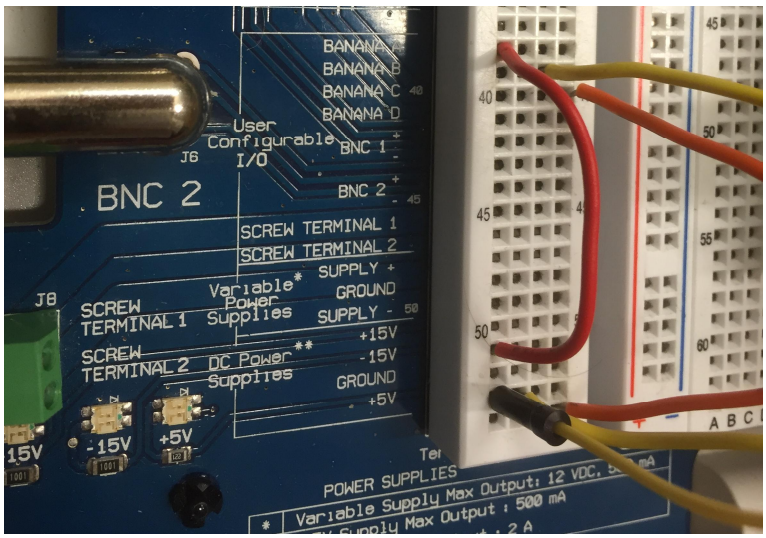

Figure 20 Power supply voltage setup to Banana A, B and C

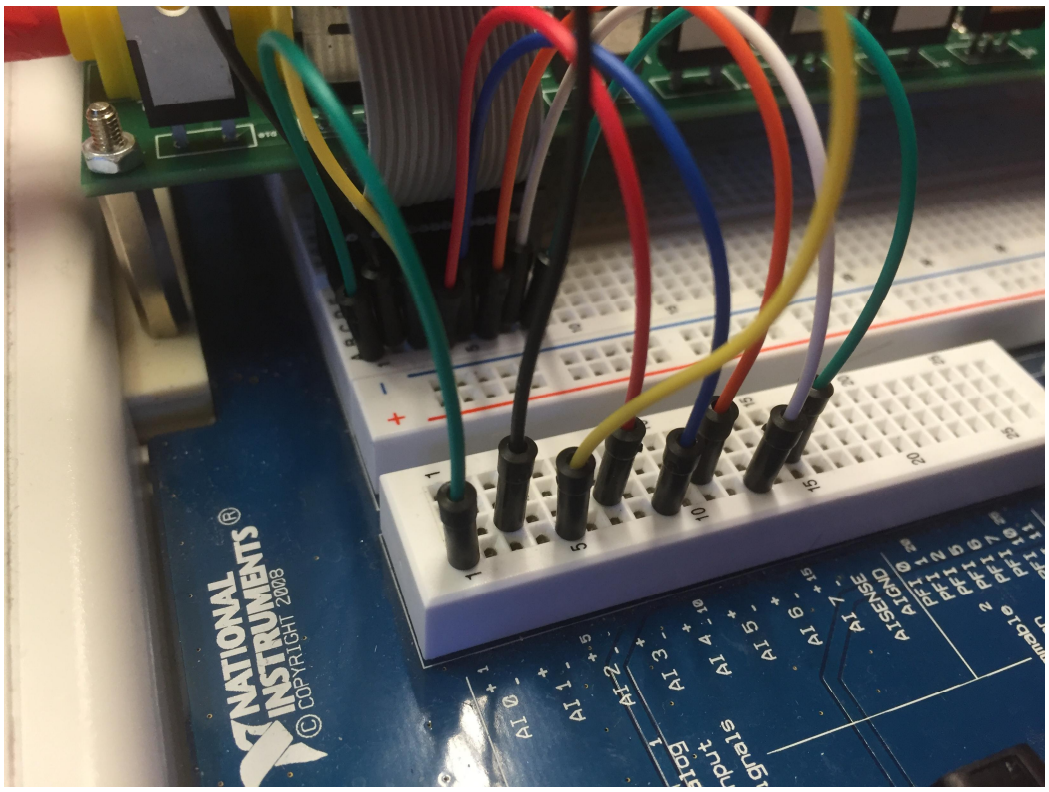

Figure 21 Setup of measurement interface to the ELVIS analog input: AI 0-7

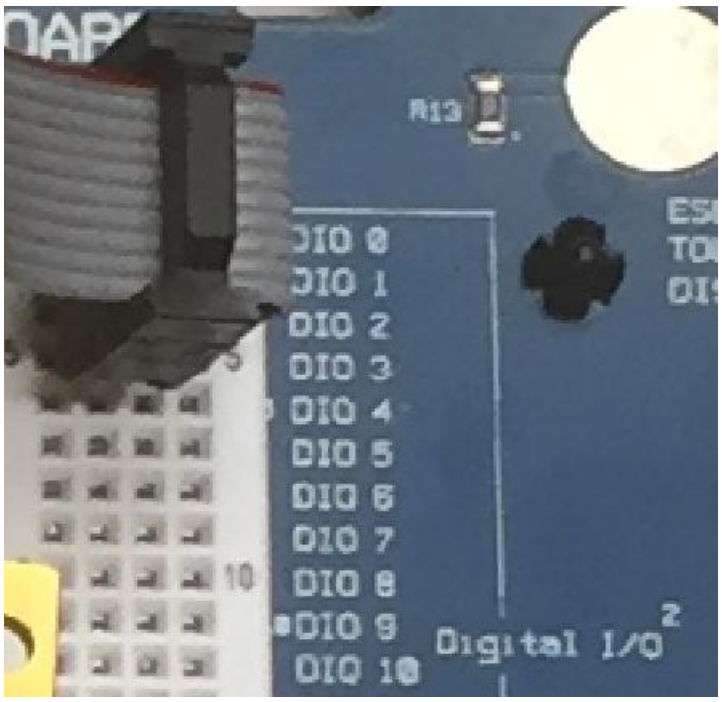

Figure 22 Gate signal input from Digital I/O port 0, DIO 0-3

14. Setup LabView for Unipolar switching with Frequency=50 Hz, Amplitude=0.8, Carrier frequency=950 Hz and Current control OFF (see Figure 4).
15. Start LabVIEW program to run continuously as shown by Figure 29.
16. Press the DEBLOCK button on the LabVIEW front panel.
17. Set DEBLOCK switch on the board ON.
18. Confirm correct switching is obtain in the output voltage, Ux1-Ux2. Compare with Figure 23.
19. Set DEBLOCK switch on the board OFF.
20. Switch off the ELVIS prototyping board supply.
21. Interconnect the two yellow Banana sockets (IO1, IO2) on the top of the FB-Inverter board with a yellow test lead.
22. Switch on the ELVIS prototyping board supply.
23. Confirm all 3 supply voltage indicator LEDs are green.
24. Confirm LabVIEW program is running and DEBLOCK button is green.
25. Set DEBLOCK switch on the board ON.
26. Confirm correct waveform is obtained in the load current, Iv. Compare with Figure 24.
27. Now correct operation of the FB-Inverter board is verified.
28. Set DEBLOCK switch on the board OFF.
29. Go to the Lab 3 tasks.

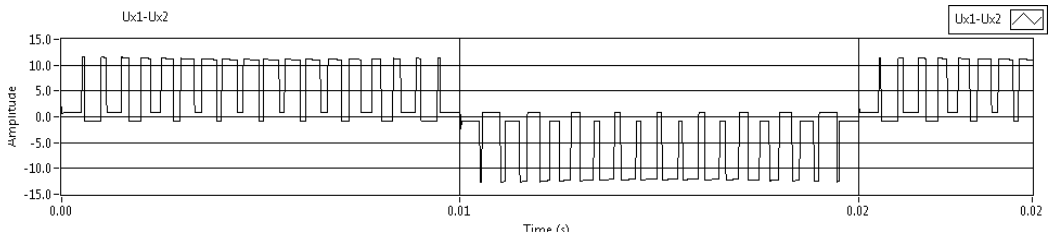

Figure 23 Measured output voltage Uop-Uon

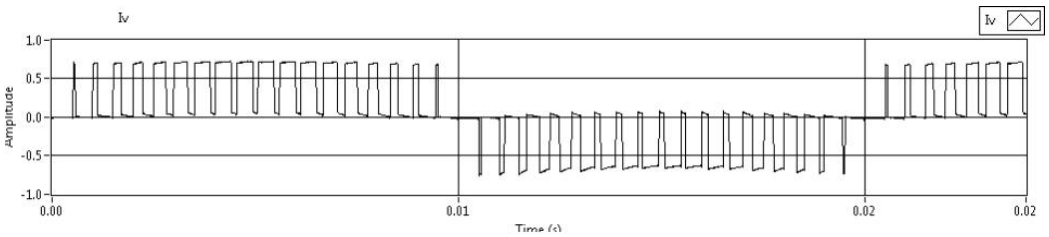

Figure 24 Measured load current Iv

Functional description of the FB-Inverter

Gate pulse interlocking

The next block after PWM control is “NonOverlapping” and contains logic to obtain interlocking between G1/G2 and G3/G4 to prevent simultaneous on-state. When G1 is on, G2 must equal zero in order to permit turn-on through G1. The same applies to the other combinations of G1 – G4. The logic also contains a deblock signal which when equal to zero sets all gate pulses to off-state. Enabling of normal switching is done with deblock=1.

Gate drive circuits

The PWM gate pulses are converted into the final gate-source voltage through the circuit showed below:

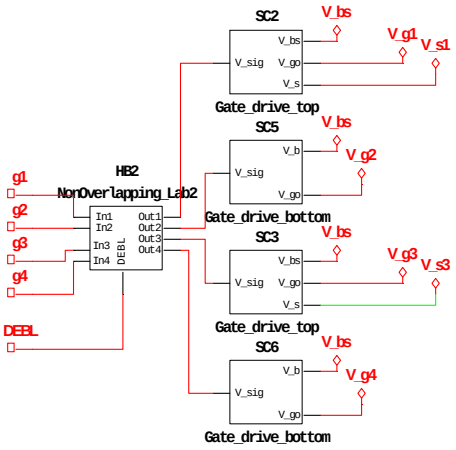

Figure 25 gate drive overview

The gate drive blocks provide isolation in addition to the actual driving of the required gate current for the proper turn-on and turn-off.

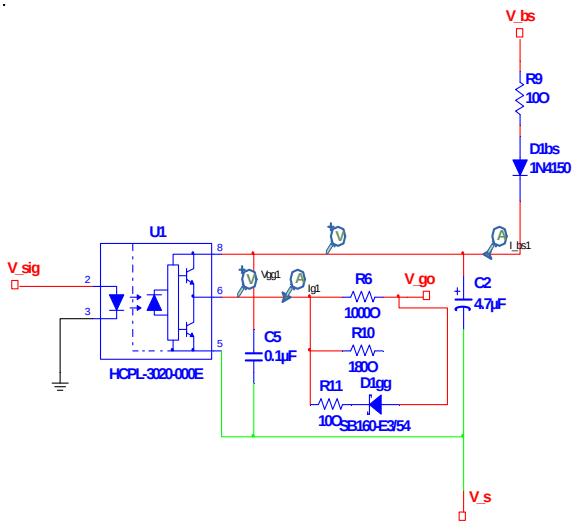

Figure 26 Gate drive of upper switches (Q1 & Q3)

Isolation is provided through the opto-coupler U1 of the type HCPL-3020 by AVAGO Technologies. The data sheet is found in the Lab2 system folder.
The supply to the gate drive is provided by the bootstrap circuit constituted by R9, D1bs and C2 in Figure 26. Bootstrapping is required since the upper switches will see a potential of the source (and gate) that changes through the switching operation. The bootstrap is fed by the dc-voltage source Vdc_bs in Figure 16. Charging of the bootstrap capacitor C2 will commence at the initial turn-on of the main switch Q2 (see Figure 28). The initial charging current will be limited by R2,

which also sets a time constant together with the capacitor which defines the speed of charging.

The gate drive provides separate gate resistance for turn-on and turn-off. Turn-on is determined by R6 (can be paralleled by R10) and turn-off by R11 in series with the schottky diode D1gg.

The gate drive for the lower switches Q2 and Q4 does not need the bootstrap circuit due to grounding of the source terminals, allowing the drive circuit to be connected to a normal voltage supply.

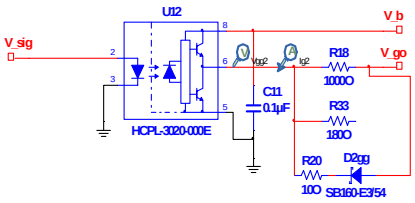

Figure 27 Gate drive for lower switches (Q2 & Q4)

Inverter main circuit

The full-bridge inverter circuit is defined by the "Inverter_core" block in Figure 16, where the following external terminals are found:

V_in: The dc-side voltage
V_op: The positive ac-output terminal
V_on: The negative ac-output terminal

Inside "Inverter-core" the detailed full-bridge inverter circuit is defined as shown by Figure 28. Please note the labeling of the main MOSFETs and diodes not being as per the general notation. The labeling shown in Figure 28 corresponds to labeling found on the FB-Inverter board. However, for general notation the following translation shall be made:

Q1/D1 = Q5/D5
Q2/D2 = Q8/D8
Q3/D3 = Q7/D9
Q4/D4 = Q6/D10

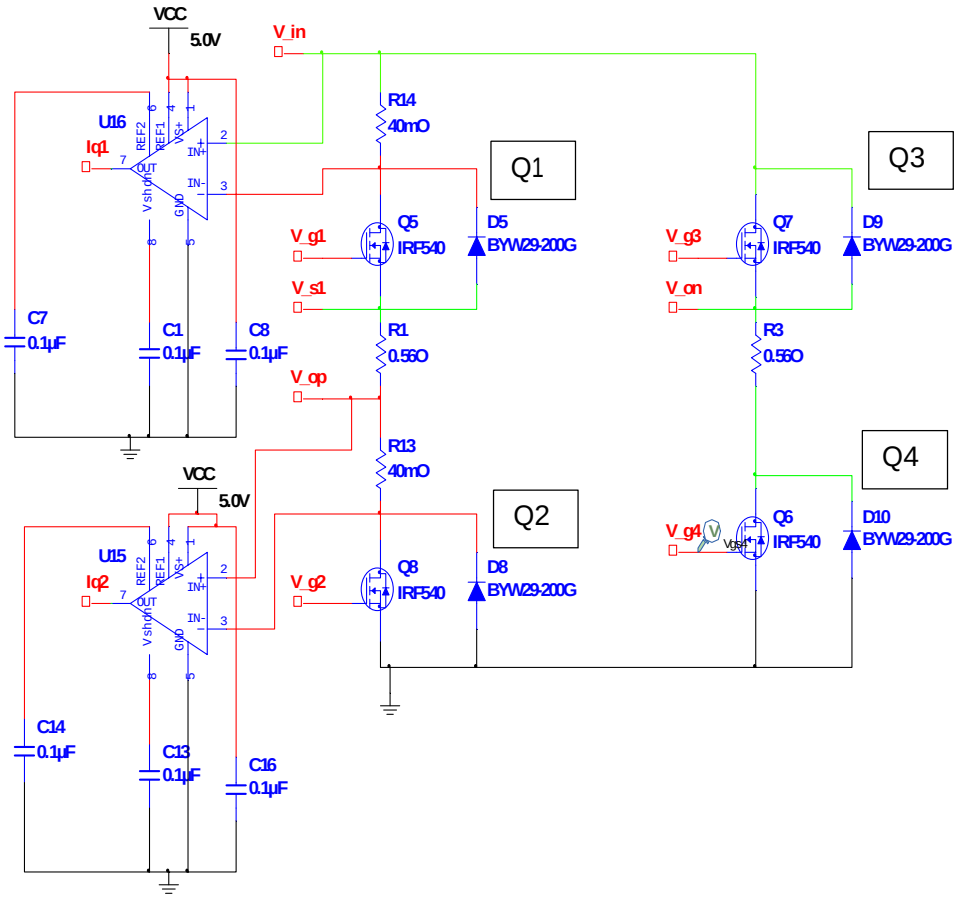

Figure 28 Full-bridge inverter circuit

The full-bridge is designed with MOSFET switches Q1-Q4 of type IRF540 by VISHAY. An antiparallel diode is included with each MOSFET as D1-D4 of the type BYW29E-200. The data sheets for the MOSFET and the diode is found in the Lab2 system folder.

Current sense circuit are included to monitor the current through Q1/D1 (Q5/D5) and Q2/D2 (Q8/D8). The scale factor of the current is 0.4 V/A related to 0.04 ohm current sense resistor and a gain of 10 for the current sense amplifier.

Measurement signals

The FB-Inverter board are setup for output of 8 analog measurement signals. 3 current measurements and 5 voltage measurements. The current signals are derived from current sense amplifiers LT1999IMS-10. As described in previous sub-section, two current sense circuits are monitoring the Q1/D1 and Q2/D2 currents while a third current sense is measuring the load current as shown in Figure 16.

The output of the current sense amplifiers has an offset of 2.5 V with the superimposed voltage related to the measured current with a scaling of 0.4 V/A. Consequently, since the current sense amplifier has a supply voltage of 5V, the peak current that can be measured is 5 A, corresponding to a voltage signal between 0.5 V and 4.5 V.

The five available voltage signals, Ux1-Ux5, are scaled with a factor 0.31 V/V and through flexible wiring selected from the following 10 measurement points.

1. Vdc +15V, the internal dc-side voltage, Vdc, of the full-bridge.
2. V_b1, the bootstrap supply of Q1
3. V_g1, the gate voltage of Q1. [Note: to get Vgs of Q1 the V_g1-V_s1 has to be externally calculated.]
4. V_s1, the source voltage of Q1
5. V_g2, the gate voltage of Q2
6. V_s3, the source voltage of Q3
7. V_g3, the gate voltage of Q3. [Note: to get Vgs of Q3 the V_g3-V_s3 has to be externally calculated.]
8. V_g4, the gate voltage of Q4
9. V_on, The negative output voltage with respect to ground (Voltage between Q3 and Q4). [Note: to get the total load voltage V_op-V_on has to be externally calculated.]
10. V_op. The positive output voltage with respect to ground (Voltage between Q1 and Q2).

The 8 analog measurements provided are:

1. Load current. (0.4 A/V with 2.5 V offset)
2. Ux1. (0.31 V/V)
3. Ux2. (0.31 V/V)
4. Ux3. (0.31 V/V)
5. Ux4. (0.31 V/V)
6. Ux5. (0.31 V/V)
7. Q1/D1 current. (0.4 A/V with 2.5 V offset)
8. Q2/D2 current. (0.4 A/V with 2.5 V offset)

Converter ratings

The MOSFET based full-bridge converter described here has the following ratings:

- V_{dc} = 15 V (17 V is max for load resistor without heatsink)
- V_{bs} = 10 V – 20 V (V_{GS} max = 20V)
- V_{out} (m_a = 0.9, V_{dc} = 15 V) = 9.5 Vrms
- I_{out} (R_{load} = 10 ohm, m_a = 0.9, V_{dc} = 15 V) = 0.95 Arms
- P_{out} = 9.1 W

- Power resistor $P_{out,max}$ (without heatsink) = 14 W @ Ta=25C
- MOSFET (IRF540) main data:
  - $V_{DS,max}$ = 100 V
  - $I_{D,max}$ = 20 A (T_{case} = 100C)
  - I_{DM} = 110 A (pulsed drain current)
  - $V_{GS,\ max}$ = 20V
  - R_{DSon} = 0.077 ohm

Lab 3 tasks

Setup the following signals for analog measurement from the FB-Inverter board:

1. Ux1 = U_op (output voltage Q1-Q2 leg)
2. Ux2 = U_on (output voltage Q3-Q4 leg)
3. Ux3 = V_g2 (Q2 gate voltage)
4. Ux4 = V_g4 (Q4 gate voltage)
5. Ux5 = Vdc +15V

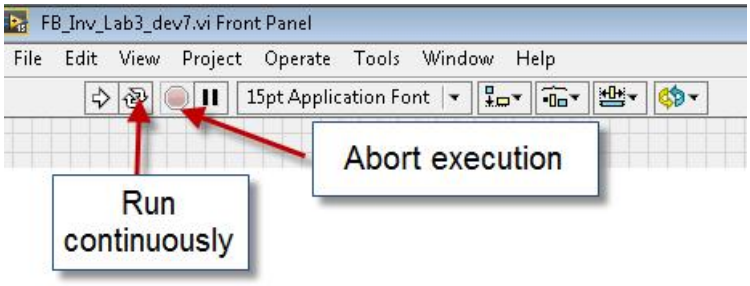

Figure 29 Program execution control in LabVIEW

BE AWARE THAT THE LOAD RESISTOR WILL BE HOT!!

3-1 Bipolar switching, with fixed modulation

1. Start LabVIEW program to run continuously as shown by Figure 29.
2. Select Bipolar PWM
3. Turn-off current control
4. Set carrier Vtri frequency to 950 Hz
5. Set PWM Vref amplitude = 0.9
6. Set PWM Vref frequency = 50 Hz
7. Set DEBLOCK switch on the board ON.
8. Freeze measurement update in LabVIEW by stopping execution using the “Abort execution” button according to Figure 29.

9. Save graphs for a 20 ms interval related to the cycle time of the fundamental for:
    a. Vref and Vtri,
    b. gate pulse graph (G1-G4),
    c. Output voltage (Ux1-Ux2),
    d. Fundamental component of (Ux1-Ux2),
    e. FFT of Ux1-Ux2,
    f. Load current,
    g. FFT of load current.
10. Set DEBLOCK switch on the board OFF.
11. Verify the magnitude of the output voltage corresponding to Equation 1 in section “PWM control”. Calculate the voltage drop of MOSFETs and resistances in Figure 28. The MOSFET data is given in section “Converter ratings”.

3-2 Unipolar switching, with fixed modulation, ma=0.9

1. Start LabVIEW program to run continuously as shown by Figure 29.
2. Select Unipolar PWM
3. Turn-off current control
4. Set carrier Vtri frequency to 950 Hz
5. Set PWM Vref amplitude = 0.9
6. Set PWM Vref frequency = 50 Hz
7. Set DEBLOCK switch on the board ON.
8. Freeze measurement update in LabVIEW by stopping execution using the “Abort execution” button according to Figure 29.
9. Save graphs for a 20 ms interval related to the cycle time of the fundamental for:
    a. Vref and Vtri,
    b. gate pulse graph (G1-G4),
    c. Output voltage (Ux1-Ux2),
    d. Fundamental component of (Ux1-Ux2),
    e. FFT of Ux1-Ux2,
    f. Load current,
    g. FFT of load current.
10. Set DEBLOCK switch on the board OFF.

3-3 Unipolar switching, with fixed modulation, ma=0.3

1. Start LabVIEW program to run continuously as shown by Figure 29.
2. Select Unipolar PWM
3. Turn-off current control
4. Set carrier Vtri frequency to 950 Hz

5. Set PWM Vref amplitude = 0.3
6. Set PWM Vref frequency = 50 Hz
7. Set DEBLOCK switch on the board ON.
8. Freeze measurement update in LabVIEW by stopping execution using the "Abort execution" button according to Figure 29.
9. Save graphs for a 20 ms interval related to the cycle time of the fundamental for:
    a. Vref and Vtri,
    b. gate pulse graph (G1-G4),
    c. Output voltage (Ux1-Ux2),
    d. Fundamental component of (Ux1-Ux2),
    e. FFT of Ux1-Ux2,
    f. Load current,
    g. FFT of load current.
10. Set DEBLOCK switch on the board OFF.
11. Run tests with variation of the Vref frequency, for a magnitude of 0.8. Check the range from 10 Hz to 200Hz
12. Run tests with variation of the Vtri, PWM carrier frequency. Check range from 400 Hz to 10 kHz. Observe the FFT harmonic spectra for the output voltage.

3-4 Unipolar switching, with current control

1. Start LabVIEW program to run continuously as shown by Figure 29.
2. Select Unipolar PWM
3. Turn-on current control
4. Set carrier Vtri frequency to 950 Hz
5. Set Ivref amplitude = 0.5
6. Set PWM Vref frequency = 50 Hz
7. Set DEBLOCK switch on the board ON.
8. Freeze measurement update in LabVIEW by stopping execution using the "Abort execution" button according to Figure 29.
9. Save graphs of Output voltage (Ux1-Ux2), Fundamental component of (Ux1-Ux2), Load current, FFT of load current.
10. Set DEBLOCK switch on the board OFF.

3-5 Thermal conditions of the power resistor

1. Measure or estimate the temperature of the power resistor when the circuit has been in operation for at least 3 minutes.
2. Calculate the thermal resistance, R_{thca} (ambient to case) based on ambient temperature and the power losses in the resistor.

Datasheets

The following data sheets and application notes are available at the Lab2 system folder:

[1] AN-6076, Design and application guide of bootstrap circuit for high-voltage gate drive IC
[2] BYW29E-200, Ultrafast power diode
[3] HCPL-30200302-04-Amp-Output-Current-IGBT-Gate-Drive-Optocoupler
[4] IR MOSFET basics
[5] IRF540, Power MOSFET
[6] Power MOSFET basics VISHAY
[7] ARCOL HS50, Power resistor
[8] SB160 Schottky barrier rectifier