

# Hand-in problems 3 for TSTE18 Digital Arithmetic

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September 4, 2017

The solutions to the hand-in problems should be submitted at most one week after the corresponding seminar to result in prioritized corrections.

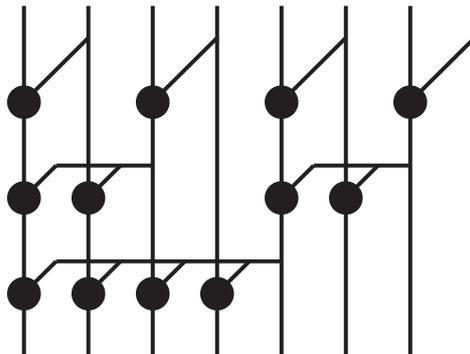
These problems should be solved on an **individual** basis. Each student has a consecutive number assigned during the first seminar (or through email contact with the examiner) and should solve the problems using the corresponding data.

Note that the problems should be solved **“by hand”**. Hence, you will need to provide some evidence that you actually solved the problem and not just ran some software for it.

**On each sheet of paper write name, personal id number, and student-id, as well as the consecutive number assigned to you.**

## 1 Parallel-prefix addition

Add the following numbers on an eight-bit Ladner-Fischer based adder shown below. Show all propagate and generate signals in the adder.



Student	Number 1	Number 2
1	00110011	10100101
2	11101011	01001110
3	10000010	11001000
4	00101100	11110011
5	11001011	10011110
6	01001011	10010001
7	10010101	11111110
8	11011111	11110111
9	10111000	01111100
10	11110001	10001100
11	01010110	01111010
12	10111110	10011110
13	11001001	11111110
14	11110111	10011001
15	11110111	00111100
16	00101110	01100110
17	10100011	10011000
18	11101001	10011010
19	10000010	10011010
20	11000000	00100111

## 2 Parallel-prefix trade-offs

Derive eight-bit parallel prefix networks using as few dot operators as possible for all depths between three and seven dot operators. Count the number of dot operators.

## 3 Non-power-of-two wordlength parallel prefix adders

Derive a Ladner-Fischer like parallel prefix network for a 10-bit adder. Compare the number of operators, depth, and maximum fan-out with a pruned (i.e. one where you remove unused parts) 16-bit Ladner-Fischer adder.

## 4 Carry-select adders

Assume that the gate delay is 2 ns for both carry and sum outputs of a full adder and 1 ns for a two-to-one multiplexer. Ignore wire and load delays. Derive a 12-bit carry-select adder with as small total delay as possible.