SOLUTIONS. Exam August 22, 2009
TSEI05 Analog and Discrete-time Integrated Circuits.

Exercise 1.

As the small signals $V_{gs2} = 0$ and $V_{bs2} = 0$ we can sketch following SSEC:

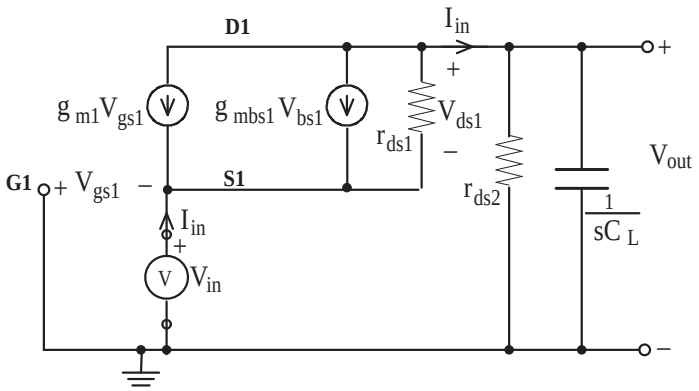

Figure 1: Amplifier. Small-signal analysis. Small-signal equivalent circuit

KCL in node D1 gives: (Note that $r_{ds} = 1/g_{ds}$)

$$(V_{out} - 0)(g_{ds2} + sC_L) + V_{ds1}g_{ds1} + g_{m1}V_{gs1} + g_{mbs1}V_{bs1} = 0 \tag{1}$$

SSEC also gives: $V_{ds1} = V_{out} - V_{in}$ and $V_{gs1} = -V_{in}$.
Because bulk is grounded $V_{bs1} = 0 - V_{in}$.

(1) now gives:

$$V_{out}(g_{ds2} + sC_L) + (V_{out} - V_{in})g_{ds1} - g_{m1}V_{in} - g_{mbs1}V_{in} = 0 \tag{2}$$

(2) gives $H(s)$:

$$\underline{\underline{H(s)}} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2} + sC_L} = \underline{\underline{\frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2}} \cdot \frac{1}{1 + \frac{sC_L}{g_{ds1}+g_{ds2}}}}} \tag{3}$$

$s = 0$ in (3) gives DC gain A_0:

$$\underline{\underline{A_0 = \frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2}}}}$$

Exercise 2.

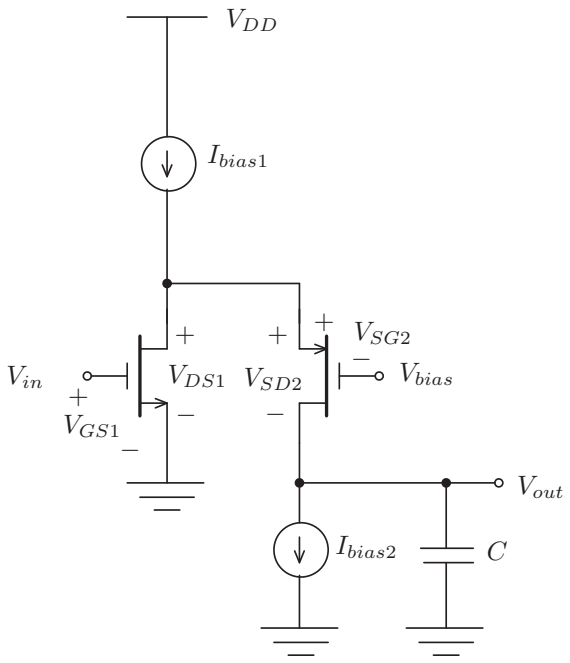

Figure 2: Folded casacode stage.

$$\text{KVL: } V_{out} + V_{SD2} - V_{DS1} = 0 \Rightarrow V_{out} = V_{DS1} - V_{SD2} \tag{4}$$

$$V_{SD2} = V_{SG2} - V_{tp} \tag{5}$$

$$V_{SG2} = V_{S2} - V_{G2} = V_{DS1} - V_{bias} \tag{6}$$

$$(5), (6) \Rightarrow V_{SD2} = V_{DS1} - V_{bias} - V_{tp} \tag{7}$$

$$(4), (7) \Rightarrow V_{out} = V_{DS1} - (V_{DS1} - V_{bias} - V_{tp}) = V_{bias} + V_{tp} \tag{8}$$

Choosing $V_{bias} = V_{in} - V_{tp}$ gives $V_{out} = V_{in}$ which was to be proved.

Exercise 3.

In **Figure 3** V_{DSi}, V_{GSi} and I_{Di}; $i = 1 - 9$ have been introduced. For determing $CMR = [V_{in,min}, V_{in,max}]$ and $OR = [V_{out,min}, V_{out,max}]$ we notice that, when all nMOS transistors are saturated, $V_{DSi,min} = V_{effi} = V_{GSi} - V_{tni} = \sqrt{\frac{I_{Di}}{\alpha_i}}$ and corresponding $V_{GSi} = \sqrt{\frac{I_{Di}}{\alpha_i}} + V_{tni}$.
Corresponding for pMOS-transistors.
Notice that $V_{DSi,min} - V_{GSi} = -V_{tni}$, for nMOS-tansistors, and $V_{SDi,min} - V_{SGi} = -V_{tpi}$ for pMOS-transistors. V_{tpi} as well as V_{tni} are positive.
When gate and source are connected $V_{DSi} = V_{GSi} = \sqrt{\frac{I_{Di}}{\alpha_i}} + V_{tni}$.
Corresponding for pMOS transistors.

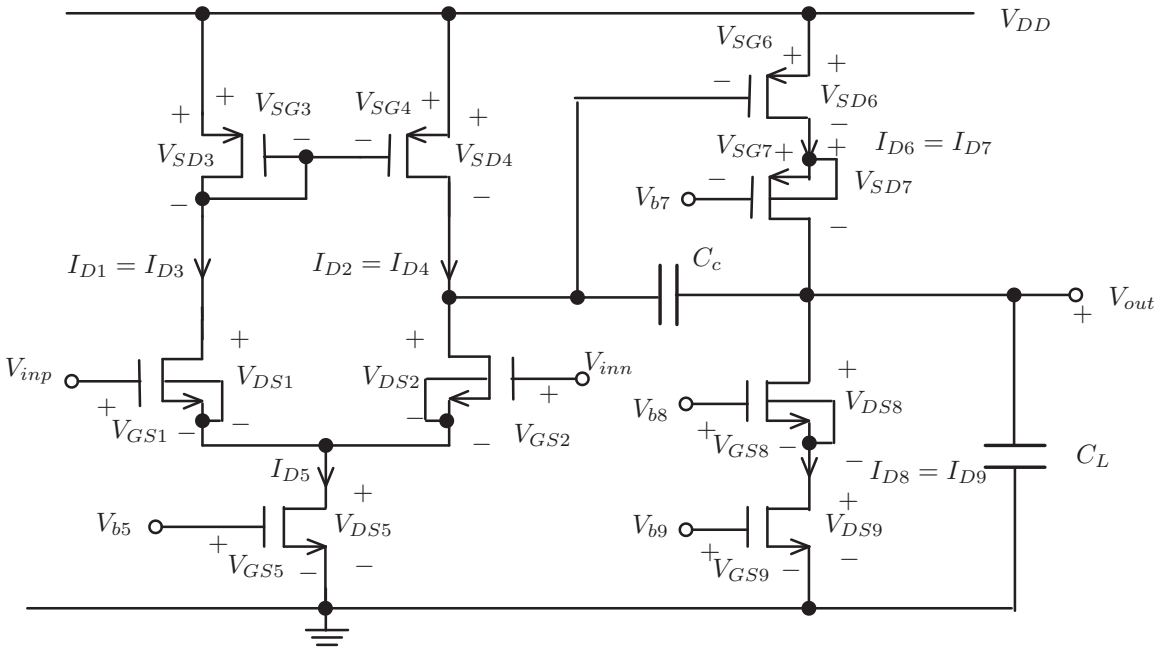

Figure 3: Transistor circuit.

– To determine $V_{in,min}$ compare all different paths from ground to V_{inn} and from ground to V_{inp}. I.e. $V_{in,min}$ will be the **maximum** of following two expressions:

$$\begin{aligned} V_{DS5,min} + V_{GS1} = &\quad \sqrt{\tfrac{I_{D5}}{\alpha_5}} + \sqrt{\tfrac{I_{D1}}{\alpha_1}} + V_{tn1} \\ V_{DS5,min} + V_{GS2} = &\quad \sqrt{\tfrac{I_{D5}}{\alpha_5}} + \sqrt{\tfrac{I_{D2}}{\alpha_2}} + V_{tn2} \end{aligned} \tag{9}$$

– To determine $V_{in,max}$ compare all paths from V_{DD} to V_{inn} and from V_{DD} to V_{inp}. I.e. $V_{in,max}$ will be the **minimum** of following four expressions:

$$\begin{aligned} V_{DD} - V_{SG3} - V_{DS1,min} + V_{GS1} = &\quad V_{DD} - \sqrt{\tfrac{I_{D3}}{\alpha_3}} - V_{tp3} + V_{tn1} \\ V_{DD} - V_{SG3} - V_{DS1,min} + V_{GS2} = &\quad V_{DD} - \sqrt{\tfrac{I_{D3}}{\alpha_3}} - V_{tp3} - \sqrt{\tfrac{I_{D1}}{\alpha_1}} + \sqrt{\tfrac{I_{D2}}{\alpha_2}} + V_{tn2} \\ V_{DD} - V_{SD4,min} - V_{DS2,min} + V_{GS2} = &\quad V_{DD} - \sqrt{\tfrac{I_{D4}}{\alpha_4}} + V_{tn2} \\ V_{DD} - V_{SD4,min} - V_{DS2,min} + V_{GS1} = &\quad V_{DD} - \sqrt{\tfrac{I_{D4}}{\alpha_4}} - \sqrt{\tfrac{I_{D2}}{\alpha_2}} + \sqrt{\tfrac{I_{D1}}{\alpha_1}} + V_{tn1} \end{aligned} \tag{10}$$

– To determine $V_{out,min}$ compare all different paths from ground to V_{out}. Here we have actually just one way from V_{DD} to V_{out}; via **M9** and **M8**. I.e.:

$$V_{out,min} = V_{DS9,min} + V_{DS8,min} = \sqrt{\frac{I_{D9}}{\alpha_9}} + \sqrt{\frac{I_{D8}}{\alpha_8}} \tag{11}$$

– To determine $V_{out,max}$ compare all paths from V_{DD} to V_{out}. Here we have actually just one way from V_{DD} to V_{out}; via **M6** and **M7**. I.e.:

$$V_{out,max} = V_{DD} - V_{SD6,min} - V_{SD7,min} = V_{DD} - \sqrt{\frac{I_{D6}}{\alpha_6}} - \sqrt{\frac{I_{D7}}{\alpha_7}} \tag{12}$$

Answer:
CMR=[max of expressions (9) above, min of expressions (10) above]
OR=$\left[\sqrt{\frac{I_{D9}}{\alpha_9}} + \sqrt{\frac{I_{D8}}{\alpha_8}}, V_{DD} - \sqrt{\frac{I_{D6}}{\alpha_6}} - \sqrt{\frac{I_{D7}}{\alpha_7}}\right]$

Exercise 4.

Figure 4a) gives a small-signal equivalent circuit, including noise-sources. (OBS! $R_n = V_n^2(f)$)

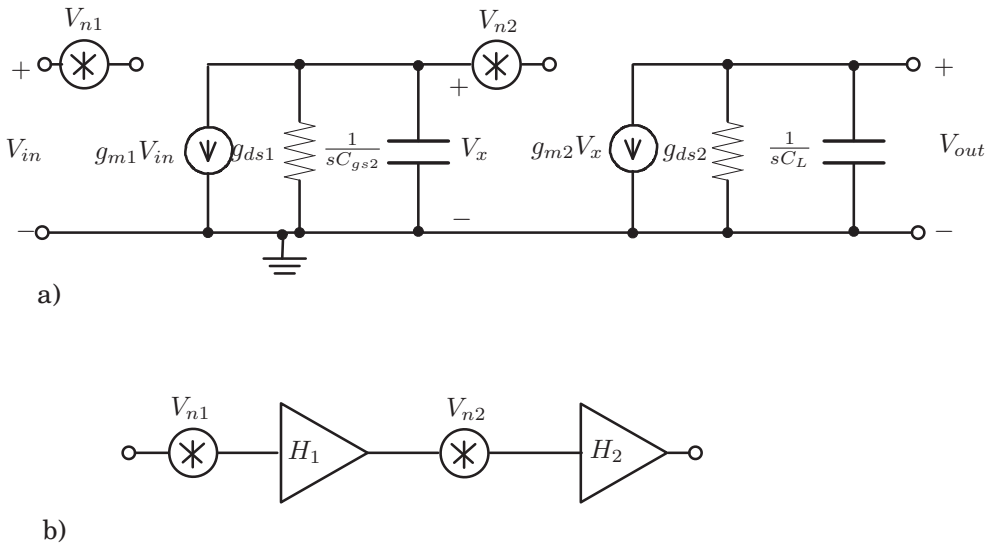

Figure 4: a) A small-signal equivalent. b) Equivalent circuit for determing output noise spectral density

As the noise sources are uncorrelated the output noise spectral density can be computed as **Figure 4b)** discribes, i.e. by the following formula

$$R_{out}(\omega) = |H_1(\omega)|^2 |H_2(\omega)|^2 R_{n1}(\omega) + |H_2(\omega)|^2 R_{n2}(\omega) \tag{13}$$

where $H_1(\omega)$ is the transfer function for the first stage and $H_2(\omega)$ the transfer function for the second stage.

From **Figure 4a)** $H_1(s) = V_x(s)/V_{in}(s)$ and $V_x(s) = -g_{m1}V_{in}(s) \cdot \frac{1}{g_{ds1}+sC_{gs2}}$ which yiels

$$H_1(s) = -\frac{g_{m1}}{g_{ds1} + sC_{gs2}} \Rightarrow H_1(\omega) = -\frac{g_{m1}}{g_{ds1} + j\omega C_{gs2}} \tag{14}$$

In the same way $H_2(s)$ is calculated to:

$$H_2(s) = -\frac{g_{m2}}{g_{ds2} + sC_L} \Rightarrow H_2(\omega) = -\frac{g_{m2}}{g_{ds2} + j\omega C_L} \tag{15}$$

Equations (13)-(15) gives following spectral density of the output noise (here we also utilize that $g_{m1} = g_{m2} = g_m$ and $g_{ds1} = g_{ds2} = g_{ds}$):

$$R_{out}(\omega) = R_{n1}(\omega)\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} \cdot \frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2} + R_{n2}(\omega)\frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2} \tag{16}$$

Using that $R_{n1}(\omega) = R_{n2}(\omega) = \frac{8kT}{3}\frac{1}{g_m}$ (from enclosed page of formulas) equation (16) gives:

$$R_{out}(\omega) = \frac{8kT}{3} \cdot \frac{1}{g_m} \cdot \frac{g_m^2}{g_{ds}^2 + \omega^2 C_L^2}\left(\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} + 1\right) \tag{17}$$

Which gives the answer:

$$\underline{\underline{R_{out}(\omega) = \frac{8kT}{3} \cdot \frac{g_m}{g_{ds}^2 + \omega^2 C_L^2}\left(\frac{g_m^2}{g_{ds}^2 + \omega^2 C_{gs2}^2} + 1\right)}} \tag{18}$$

Exercise 5

Figure 5 shows the construction of a box that splits the signal into two rooms. Note that the wires to both rooms also have the impedance 75 ohm, and that $75//75 = 37.5$ ohm. The seriel resistor 37.5 ohm then gives the impedance $37.5 + 37.5 = 75$ ohm together with those two wires, which yields that the box will give no reflection.

The disadvantage with this construction is that you loose 50 % of the power in the resistor.

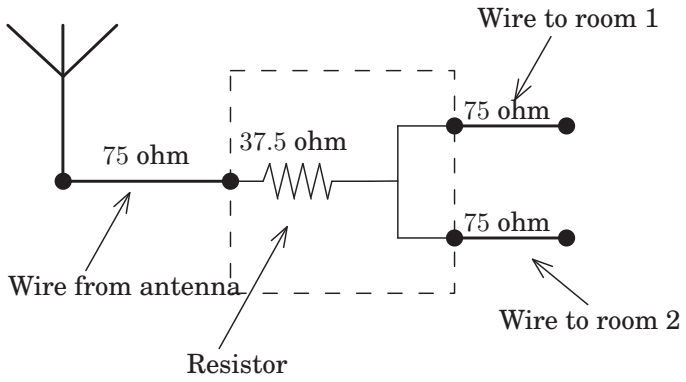

Figure 5: Construction of box.