SOLUTIONS. Exam June 12, 2009
TSEI05 Analog and Discrete-time Integrated Circuits.

Exercise 1.

Figure 1 a) gives the small signal equivalent circuit and **Figure 1 b)** it has been rewritten. Note that $V_{gs2} = 0$.

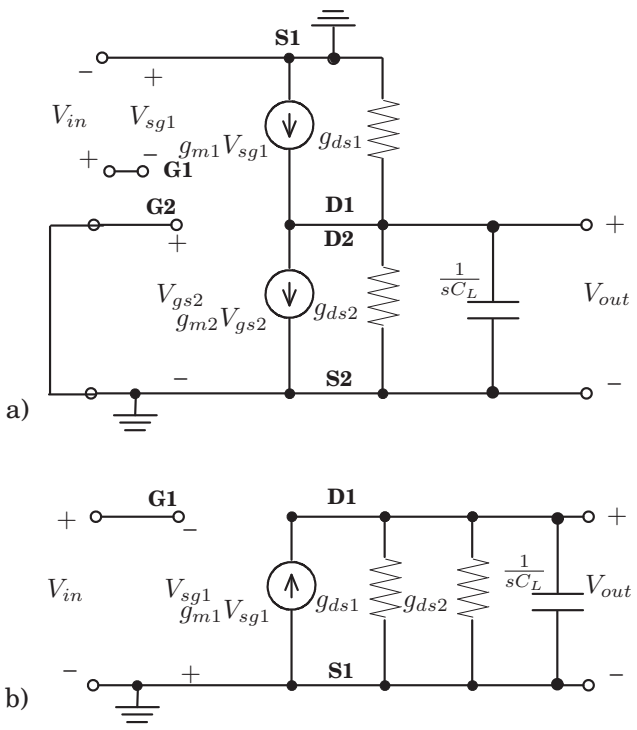

Figure 1: Small signal equivalent circuit.

As $V_{sg1} = -V_{in}$ **Figure 1 b)** gives following expression for V_{out} :

$$V_{out} = -g_{m1}V_{in} \cdot \frac{1}{g_{ds1} + g_{ds2} + sC_L} \Rightarrow H(s) = \frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L}$$

$H(s)$ can be rewritten as: $H(s) = -\dfrac{g_{m1}}{g_{ds1} + g_{ds2}} \cdot \dfrac{1}{1 + \frac{sC_L}{g_{ds1}+g_{ds2}}}$

$s = 0$ gives DC-gain $A_0 = -\frac{g_{m1}}{g_{ds1}+g_{ds2}}$

To determine the bandwidth we look att $H(j\omega)$: $H(j\omega) = \dfrac{A_0}{1 + \frac{j\omega C_L}{g_{ds1}+g_{ds2}}}$

The 3-dB bandwidth gives from the value of ω that gives $|H(j\omega)| = |A_0|/\sqrt{2}$. I.e. bandwidth will be $\omega_0 = (g_{ds1} + g_{ds2})/C_L$ which gives the gain-bandwidth-product

$|A_0| \cdot \dfrac{g_{ds1} + g_{ds2}}{C_L} = \dfrac{g_{m1}}{C_L}$

Answer: $H(s) = -\dfrac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L}$; DC-gain $A_0 = -\dfrac{g_{m1}}{g_{ds1} + g_{ds2}}$; gain-bandwidth-product $= \dfrac{g_{m1}}{C_L}$

Exercise 2.

In **Figure 2** V_{DSi}, V_{GSi} and I_{Di}; $i = 1 - 9$ have been introduced. For determing $CMR = [V_{in,min}, V_{in,max}]$ and $OR = [V_{out,min}, V_{out,max}]$ we notice that, when all nMOS transistors are saturated, $V_{DSi,min} = V_{effi} = V_{GSi} - V_{tni} = \sqrt{\frac{I_{Di}}{\alpha_i}}$ and corresponding $V_{GSi} = \sqrt{\frac{I_{Di}}{\alpha_i}} + V_{tni}$.
Corresponding for pMOS-transistors.
Notice that $V_{DSi,min} - V_{GSi} = -V_{tni}$, for nMOS-tansistors, and $V_{SDi,min} - V_{SGi} = -V_{tpi}$ for pMOS-transistors. V_{tpi} as well as V_{tni} are positive.
When gate and source are connected $V_{DSi} = V_{GSi} = \sqrt{\frac{I_{Di}}{\alpha_i}} + V_{tni}$.
Corresponding for pMOS transistors.

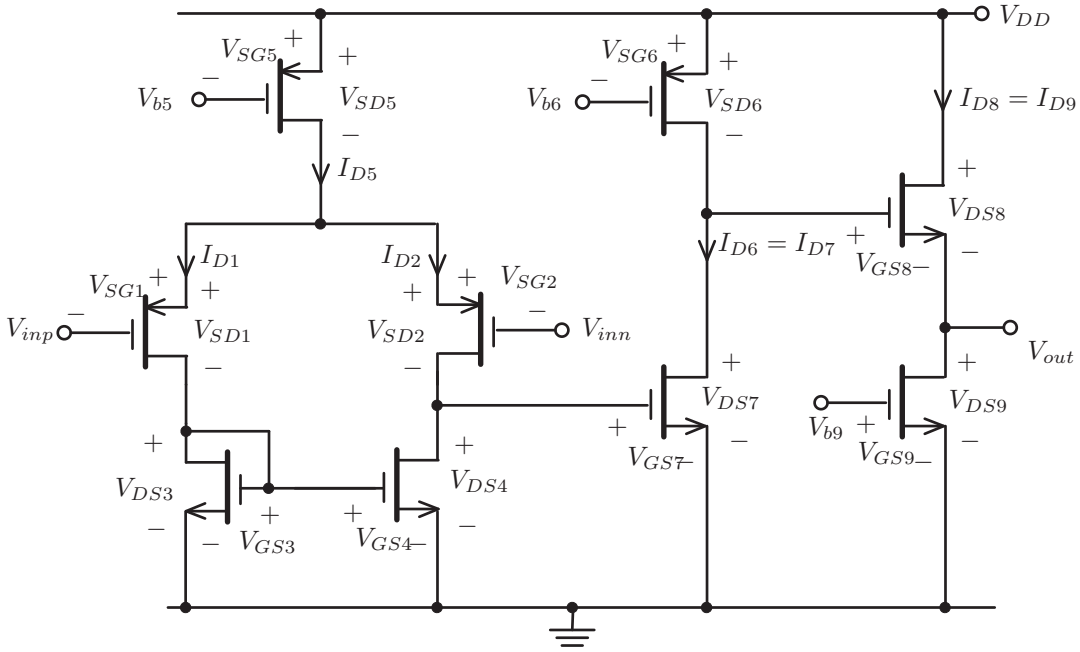

Figure 2: Transistor circuit.

– To determine $V_{in,min}$ compare all different paths from ground to V_{inn} and from ground to V_{inp}. I.e. $V_{in,min}$ will be the **maximum** of following four expressions:

$$\begin{aligned}
V_{GS3} + V_{SD1,min} - V_{SG1} = &\quad \sqrt{\tfrac{I_{D3}}{\alpha_3}} + V_{tn3} - V_{tp1} \\
V_{DS4,min} + V_{SD2,min} - V_{SG1} = &\quad \sqrt{\tfrac{I_{D4}}{\alpha_4}} + \sqrt{\tfrac{I_{D2}}{\alpha_2}} - \sqrt{\tfrac{I_{D1}}{\alpha_1}} - V_{tp1} \\
V_{GS3} + V_{SD1,min} - V_{SG2} = &\quad \sqrt{\tfrac{I_{D3}}{\alpha_3}} + V_{tn3} + \sqrt{\tfrac{I_{D1}}{\alpha_1}} - \sqrt{\tfrac{I_{D2}}{\alpha_2}} - V_{tp2} \\
V_{DS4,min} + V_{SD2,min} - V_{SG2} = &\quad \sqrt{\tfrac{I_{D4}}{\alpha_4}} - V_{tp2}
\end{aligned} \tag{1}$$

– To determine $V_{in,max}$ compare all paths from V_{DD} to V_{inn} and from V_{DD} to V_{inp}. I.e. $V_{in,max}$ will be the **minimum** of following two expressions:

$$\begin{aligned}
V_{DD} - V_{SD5,min} - V_{SG1} = &\quad V_{DD} - \sqrt{\tfrac{I_{D5}}{\alpha_5}} - \sqrt{\tfrac{I_{D1}}{\alpha_1}} - V_{tp1} \\
V_{DD} - V_{SD5,min} - V_{SG2} = &\quad V_{DD} - \sqrt{\tfrac{I_{D5}}{\alpha_5}} - \sqrt{\tfrac{I_{D2}}{\alpha_2}} - V_{tp2}
\end{aligned} \tag{2}$$

– To determine $V_{out,min}$ compare all different paths from ground to V_{out}. I.e. $V_{in,min}$ will be the **maximum** of following two expressions:

$$\begin{aligned} V_{DS9,min} &= \sqrt{\frac{I_{D9}}{\alpha_9}} \\ V_{DS7,min} - V_{GS8} &= \sqrt{\frac{I_{D7}}{\alpha_7}} - \sqrt{\frac{I_{D8}}{\alpha_8}} - V_{tn8} \end{aligned} \tag{3}$$

– To determine $V_{out,max}$ compare all paths from V_{DD} to V_{out}. I.e. $V_{out,max}$ will be the **minimum** of following two expressions:

$$\begin{aligned} V_{DD} - V_{DS8,min} &= V_{DD} - \sqrt{\frac{I_{D8}}{\alpha_8}} \\ V_{DD} - V_{SD6,min} - V_{GS8} &= V_{DD} - \sqrt{\frac{I_{D6}}{\alpha_6}} - \sqrt{\frac{I_{D8}}{\alpha_8}} - V_{tn8} \end{aligned} \tag{4}$$

Answer:
CMR=[max of expressions (1) above, min of expressions (2) above]
OR=[max of expressions (3) above, min of expressions (4) above]

Exercise 3.

a) A PMOS transistor is saturated when $V_{SD} > V_{eff} = V_{SG} - V_{tp}$.

Transistor **M1**: $V_{SD1} = V_{DD} - V_x = V_{SG1}$ i.e. $V_{SD1} > V_{SG1} - V_{tp1}$, so **M1** works in *saturation*.

Transistor **M2**: $V_{SD2} = V_x - V_{bias} = V_{SG2}$ i.e. $V_{SD2} > V_{SG2} - V_{tp2}$, so **M2** works in *saturation*.

A NMOS transistor is saturated when $V_{DS} > V_{eff} = V_{GS} - V_{tn}$.

Transistor **M3**: $V_{DS3} = V_{bias} - 0 = V_{GS3}$ i.e. $V_{DS3} > V_{GS3} - V_{tn3}$, so **M3** works in *saturation*.

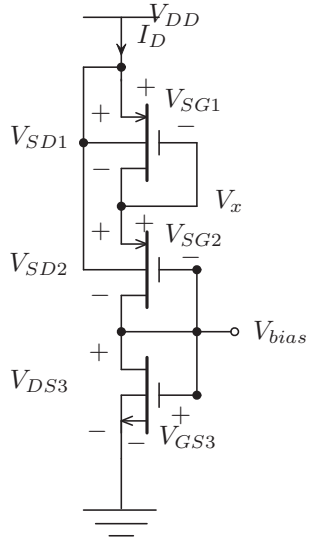

Figure 3: A bias circuit.

b) First note that $I_{D1} = I_{D2} = I_{D3} = I_D$

Transistor **M1**: $V_{SB1} = 0$ i.e. $V_{tp1} = V_{t0p}$.

Enclosed page of formulas gives:

$$\left(\frac{W}{L}\right)_1 = \frac{I_D}{\frac{1}{2}\mu_{0p}C_{oxp}V_{eff1}^2(1+\lambda_p(V_{SD1}-V_{eff1}))} \tag{5}$$

$I_D = 5\ \mu$ A, $\mu_{0p}C_{oxp} = 58.5\ \mu$ A/V^2,
$V_{eff1} = V_{SG1} - V_{t0p} = V_{DD} - V_x - V_{t0p} = 3.3 - 2.05 - 0.62 = 0.63$ V ,
$\lambda_p = 0.05$.
Further $V_{SD1} = V_{SG1}$ gives $V_{SD1} - V_{eff1} = V_{t0p} = 0.62$ V.
Now equation (1) gives:

$$\left(\frac{W}{L}\right)_1 \approx 0.42 \tag{6}$$

Transistor **M2**: $V_{SB2} = V_{S2} - V_{B2} = V_x - V_{DD} = -1.25$ V.

Enclosed page of formulas gives:

$$V_{tp2} = V_{t0p} + \gamma(\sqrt{2\phi_F - V_{SB2}} - \sqrt{2\phi_F}) = 0.62 + 0.41(\sqrt{2.07} - \sqrt{0.82} = 0.8386 \text{ V} \tag{7}$$

$$\left(\frac{W}{L}\right)_2 = \frac{I_D}{\frac{1}{2}\mu_{0p}C_{oxp}V_{eff2}^2(1+\lambda_p(V_{SD2}-V_{eff2}))} \tag{8}$$

$I_D = 5\ \mu$ A, $\mu_{0p}C_{oxp} = 58.5\ \mu$ A/V^2,
$V_{eff2} = V_{SG2} - V_{tp2} = V_x - V_{bias} - V_{tp2} = 2.05 - 0.6 - 0.8386 = 0.6114$ V ,
$\lambda_p = 0.05$.
Further $V_{SD2} = V_{SG2}$ gives $V_{SD2} - V_{eff2} = V_{tp2} = 0.8386$ V.
Now equation (4) gives:

$$\left(\frac{W}{L}\right)_2 \approx 0.44 \tag{9}$$

Transistor **M3**: $V_{BS3} = 0$ i.e $V_{tn3} = V_{t0n} = 0.47$.

$$\left(\frac{W}{L}\right)_3 = \frac{I_D}{\frac{1}{2}\mu_{0n}C_{oxn}V_{eff3}^2(1+\lambda_n(V_{DS3}-V_{eff3}))} \tag{10}$$

$I_D = 5\ \mu$ A, $\mu_{0n}C_{oxn} = 180\ \mu$ A/V^2,
$V_{eff3} = V_{GS3} - V_{t0n} = V_{bias} - 0 - V_{t0n} = 0.6 - 0.47 = 0.13$ V ,
$\lambda_n = 0.03$.
Further $V_{DS3} = V_{GS3}$ gives $V_{DS3} - V_{eff3} = V_{t0n} = 0.47$ V.
Now equation (6) gives:

$$\left(\frac{W}{L}\right)_3 \approx 3.24 \tag{11}$$

Answer: $\left(\frac{W}{L}\right)_1 \approx 0.42$, $\left(\frac{W}{L}\right)_2 \approx 0.44$ and $\left(\frac{W}{L}\right)_3 \approx 3.24$

Exercise 4.

Figure 4 shows the construction of a box that splits the signal into two rooms. Note that the wires to both rooms also have the impedance 75 ohm, and that $75//75 = 37.5$ ohm. The seriel resistor 37.5 ohm then gives the impedance $37.5 + 37.5 = 75$ ohm together with those two wires, which yields that the box will give no reflection.

The disadvantage with this construction is that you loose 50 % of the power in the resistor.

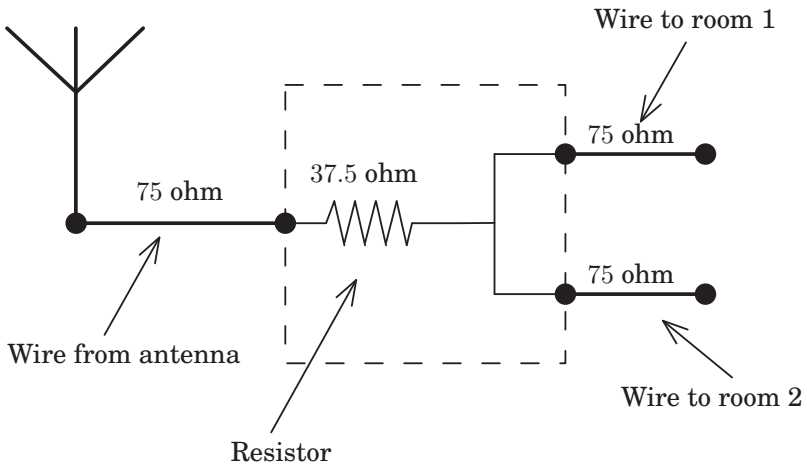

Figure 4: Construction of box.

Exercise 5

a) The output noise spectral density can be computed by the following formula

$$S_{out}(\omega) = |H(\omega)|^2 S_{in}(\omega) \tag{12}$$

where $H(\omega)$ is the transfer function from the noise source output node.

Determin the transfer function from the positive input node to the output of the operational amplifier, while the input voltage is zeroed:

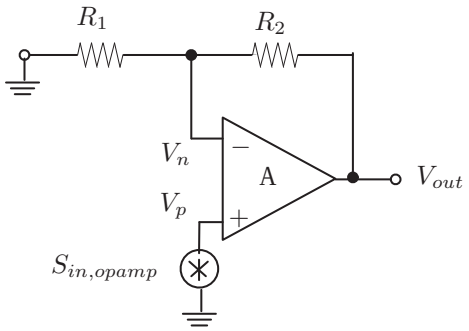

Figure 5: Determing $H = V_{out}/V_p$.

$$\begin{aligned}(0 - V_n)G_1 &= (V_n - V_{out})G_2 \\ (V_p - V_n)A &= V_{out}\end{aligned} \tag{13}$$

Solving this system of equation results in

$$H = \frac{V_{out}}{V_p} = \frac{G_1 + G_2}{G_2 + (G_1 + G_2)/A} = \frac{(G_1 + G_2)g_{m1}}{G_2 g_{m1} + (G_1 + G_2)g_{out}} \tag{14}$$

Hence, the equivalent output noise spectral density is given by

$$S_{out} = |H|^2 \cdot S_{in,opamp} = \left(\frac{(G_1 + G_2)g_{m1}}{G_2 g_{m1} + (G_1 + G_2)g_{out}}\right)^2 \cdot S_{in,opamp} \tag{15}$$

Using the fact that the ratio between the resistors is equal to a gives the answer:

$$\underline{\underline{S_{out} = \frac{(1+a)^2 g_{m1}}{(g_{m1} + (1+a)g_{out})^2} \cdot \frac{16kT}{3}(1 + \frac{g_{m4}}{g_{m1}})}} \tag{16}$$

b) The noise at the output can be decreased by increasing the transconductance g_{m1} of the input stage. This decreases the last term in Equation (16) while the first part is not changed so much. This will increase the gain of the amplifier.