SOLUTIONS. Exam May 29, 2006

TSTE80 Analog and Discrete-time Integrated Circuits.

Excercise 1.

a) Transistor **M2** works in *saturation*.

Enclosed page of formulas gives:

$$I_{D2} = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_2 \left((V_{GS2} - V_{tn})^2\right)(1 + \lambda V_{DS2}) \tag{1}$$

Neglecting channal-length modulation (i.e. $\lambda = 0$) gives:

$$I_{D2} = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{tn})^2 \tag{2}$$

Also transistor **M1** works in *saturation*. Neglecting channal-length modulation gives:

$$I_{D1} = I_0 = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2 \tag{3}$$

As $V_{GS1} = V_{GS2}$ equation (2) and equation (3) gives:

$$\frac{I_{D2}}{I_0} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \Rightarrow I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_0 = K I_0 \tag{4}$$

Figure 1 gives:

$$V_{out} = V_{DD} - R I_{D2} \Rightarrow \underline{\underline{V_{out} = V_{DD} - RK I_0}} \tag{5}$$

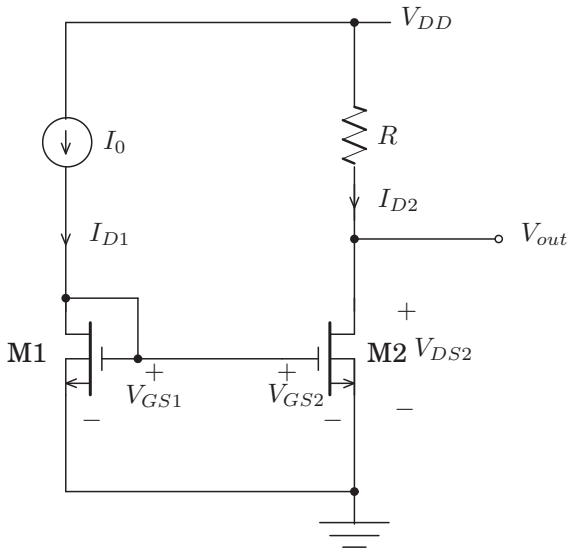

Figure 1: A commonly used analog circuit.

b) Transistor M1 is still in saturation and channel-length modulation still neglects, so:

$$I_{D1} = I_0 = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2 \Rightarrow V_{GS1} - V_{tn} = \sqrt{\frac{I_0}{\alpha_1}} \tag{6}$$

Where $\alpha_1 = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_1$

Transistor M2 works in the linear region. Enclosed page of formula gives:

$$I_{D2} = \frac{\mu_0 C_{ox}}{2} \left(\frac{W}{L}\right)_2 (2(V_{GS2} - V_{tn}) - V_{DS2}) V_{DS2} \tag{7}$$

As $V_{DS2} = V_{out}$, $V_{GS2} = V_{GS1}$ and $\left(\frac{W}{L}\right)_2 = K \left(\frac{W}{L}\right)_1$ (7) can be written as:

$$I_{D2} = K\alpha_1 (2(V_{GS1} - V_{tn}) - V_{out}) V_{out} \tag{8}$$

Inserting (6) in (8) gives:

$$I_{D2} = K\alpha_1 (2\sqrt{\frac{I_0}{\alpha_1}} - V_{out}) V_{out} \tag{9}$$

Inserting (9) in the equation

$$V_{out} = V_{DD} - RI_{D2}$$

gives:

$$V_{out} = V_{DD} - RK\alpha_1 (2\sqrt{\frac{I_0}{\alpha_1}} - V_{out}) V_{out} \tag{10}$$

Rewriting (10) gives:

$$RK\alpha_1 V_{out}^2 - (1 + 2RK\sqrt{\alpha_1 I_0}) V_{out} + V_{DD} = 0 \tag{11}$$

Solving for V_{out} gives the answer:

$$\underline{\underline{V_{out} = \frac{1}{2\alpha_1 KR} + \sqrt{\frac{I_0}{\alpha_1}} \pm \sqrt{\left(\frac{1}{2\alpha_1 KR} + \sqrt{\frac{I_0}{\alpha_1}}\right)^2 - \frac{V_{DD}}{\alpha_1 KR}}}}$$

c) At the limit of saturation region

$$V_{DS} = V_{GS} - V_{tn} \tag{12}$$

In this case

$$\left.\begin{array}{r} V_{DS2} = V_{out} \\ V_{GS2} - V_{tn} = \sqrt{\frac{I_0}{\alpha_1}} \end{array}\right\} \overset{(12)}{\Rightarrow} V_{out} = \sqrt{\frac{I_0}{\alpha_1}} \tag{13}$$

But, as before in a) and b):

$$V_{out} = V_{DD} - RKI_0 \tag{14}$$

Combining (14) and (15) yields

$$\sqrt{\frac{I_0}{\alpha_1}} = V_{DD} - RKI_0 \tag{15}$$

which is reformulated to

$$\underline{\underline{K = \frac{V_{DD} - \sqrt{\frac{I_0}{\alpha_1}}}{RI_0} = \frac{V_{DD}}{RI_0} - \frac{1}{R\sqrt{\alpha_1 I_0}}}} \tag{16}$$

which is the answer.

Exercise 2.

a) **Figure 2 a)** gives the complete small signal equivalent circuit (SSEC) and in **figure 2 b)** this SSEC has been redrawn noticing that:

- $V_{gs1} = V_{in}$
- $V_{gs3} = 0$
- g_{ds3} is parallel to g_{ds1}

Introducing the voltage V_x in node **D1, S2** yields:

- $V_{gs2} = V_{g2} - V_{s2} = 0 - V_x = -V_x$
- $V_{bs2} = V_{b2} - V_{s2} = 0 - V_x = -V_x$

KCL in the output node and in ground node gives:

$$\begin{aligned} -(V_{out} - 0)sC_L + (g_{m2} + g_{bs2})V_x - g_{ds2}(V_{out} - V_x) &= 0 & (17)\\ (V_{out} - 0)sC_L + g_{m1}V_{in} + (g_{ds1} + g_{ds3})(V_x - 0) &= 0 & (18) \end{aligned}$$

$$\begin{aligned} (17) \Rightarrow V_x &= \frac{sC_L V_{out} + g_{ds2}V_{out}}{g_{m2} + g_{ds2} + g_{bs2}} & (19)\\ (18) \Rightarrow V_x &= \frac{-sC_L V_{out} - g_{m1}V_{in}}{g_{ds1} + g_{ds3}} & (20) \end{aligned}$$

I.e.

$$\frac{sC_L V_{out} + g_{ds2}V_{out}}{g_{m2} + g_{bs2} + g_{ds2}} = \frac{-sC_L V_{out} - g_{m1}V_{in}}{g_{ds1} + g_{ds3}} \tag{21}$$

(21) gives:

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{sC_L + \frac{(sC_L + g_{ds2})(g_{ds1} + g_{ds3})}{g_{m2} + g_{bs2} + g_{ds2}}} \tag{22}$$

Rewriting (22) gives the answer:

$$\underline{\underline{H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m2} + g_{bs2} + g_{ds2})}{g_{ds2}(g_{ds1} + g_{ds3}) + sC_L(g_{ds1} + g_{ds3} + g_{m2} + g_{bs2} + g_{ds2})}}}$$

b) Neglecting the bulk effect, i.e. putting $g_{bs2} = 0$, and assuming $g_m >> g_{ds}$ gives following approximation of $H(s)$:

$$H(s) = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1} + g_{ds3}) + sC_L g_{m2}} = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1} + g_{ds3})} \cdot \frac{1}{1 + \frac{sC_L g_{m2}}{g_{ds2}(g_{ds1} + g_{ds3})}} \tag{23}$$

(23) gives:

- DC-gain $A_0 = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1} + g_{ds3})}$

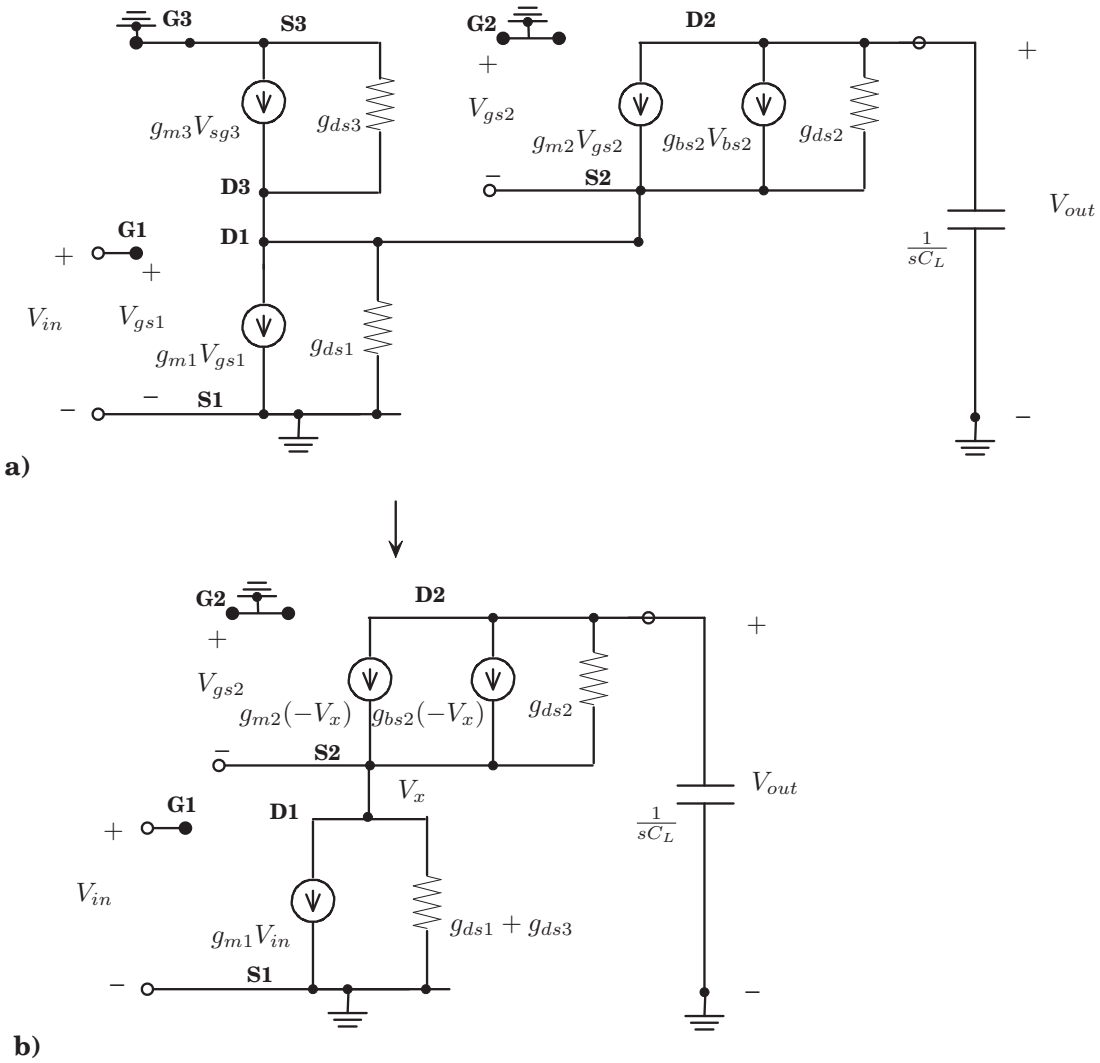

Figure 2: Small signal equivalent circuit.

- First (and only) pole $p_1 = -\frac{g_{ds2}(g_{ds1}+g_{ds3})}{C_L g_{m2}}$
- $$H(\omega) = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})} \cdot \frac{1}{1+\frac{j\omega C_L g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})}} \Rightarrow |H(\omega)| = \frac{g_{m1}g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})} \cdot \frac{1}{\sqrt{1+\left(\frac{\omega C_L g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})}\right)^2}}$$

  Unity-gain frequency ω_u is the frequency when $|H(\omega)| = 1$.

$$|H(\omega)| = 1 \Rightarrow \frac{|A_0|}{\sqrt{1+\frac{\omega^2}{p_1^2}}} = 1 \Rightarrow \omega_u = |p_1|\sqrt{A_0^2-1} \approx |p_1||A_0|$$

In this case:

$$\omega_u \approx |p_1||A_0| = \frac{g_{ds2}(g_{ds1}+g_{ds3})}{C_L g_{m2}} \cdot \frac{g_{m1}g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})} = \frac{g_{m1}}{C_L} \tag{24}$$

Answer: $\underline{\underline{A_0 = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})}, p_1 = -\frac{g_{ds2}(g_{ds1}+g_{ds3})}{C_L g_{m2}}, \omega_u = \frac{g_{m1}}{C_L}}}$

c) As $g_{mi} \sim \sqrt{\frac{W_i}{L_i} I_{Di}}$, $g_{dsi} \sim \frac{1}{L_i} I_{Di}$, and $I_{D2} = I_0$, $I_{D1} = I_0 + I_{D3}$ where I_{D3} is the current for M3. Also $I_{D3} \sim \frac{W_3}{L_3}$ set $I_{D3} = k\frac{W_3}{L_3}$:

$$\underline{\underline{A_0}} = \frac{-g_{m1}g_{m2}}{g_{ds2}(g_{ds1}+g_{ds3})} \sim \frac{\sqrt{\frac{W_1}{L_1}(I_0+I_3)}\sqrt{\frac{W_2}{L_2}I_0}}{\frac{1}{L_2}I_0\left(\frac{1}{L_1}(I_0+I_3)+\frac{1}{L_3}I_3\right)} \tag{25}$$

$$= \frac{\sqrt{W_1L_1W_2L_2}\sqrt{1+\frac{I_3}{I_0}}}{\left(I_0+I_3+\frac{L_1}{L_3}I_3\right)} = \underline{\underline{\frac{\sqrt{W_1L_1W_2L_2}\sqrt{1+\frac{kW_3}{L_3I_0}}}{\left(I_0+\frac{kW_3}{L_3}+\frac{L_1}{L_3}\frac{kW_3}{L_3}\right)}}} \tag{26}$$

Equation (26) yields that:

- $|A_0|$ decrease when I_0 increase.
- $|A_0|$ increase when L_3 increase.
- $|A_0|$ decrease when W_3 increase.

Exercise 3.

a) a) This exercise is solved using the charge redistribution analysis. The voltage at the node between C_1 and C_2 is here denoted $V_x(t)$. First, the reference direction of the charge is chosen. Next, the charge of the capacitors are computed for time t, $t+\tau$, and $t+2\tau$

For time t:

$$\begin{aligned} q_1(t) &= (0 - V_x(t))C_1 \\ q_2(t) &= (0 - V_x(t))C_2 \\ q_3(t) &= (V_{out}(t) - V_x(t))C_3 \\ q_4(t) &= (V_{out}(t) - 0)C_4 \end{aligned} \tag{27}$$

For time $t+\tau$:

$$\begin{aligned} q_1(t+\tau) &= (V_{in}(t+\tau) - 0)C_1 \\ q_2(t+\tau) &= 0 \\ q_3(t+\tau) &= q_3(t) \\ q_4(t+\tau) &= (V_{out}(t+\tau) - 0)C_4 \end{aligned} \tag{28}$$

For time $t+2\tau$:

$$\begin{aligned} q_1(t+2\tau) &= (0 - V_x(t+2\tau))C_1 \\ q_2(t+2\tau) &= (0 - V_x(t+2\tau))C_2 \\ q_3(t+2\tau) &= (V_{out}(t+2\tau) - V_x(t+2\tau))C_3 \\ q_4(t+2\tau) &= (V_{out}(t+2\tau) - 0)C_4 \end{aligned} \tag{29}$$

Equations for the charge conservation:

$$q_2(t) - q_4(t) = q_2(t+\tau) - q_4(t+\tau) \tag{30}$$

$$q_2(t+\tau) = q_2(t+2\tau) \tag{31}$$

$$-q_1(t+\tau) - q_2(t+\tau) - q_3(t+\tau) = -q_1(t+2\tau) - q_2(t+2\tau) - q_3(t+2\tau) \tag{32}$$

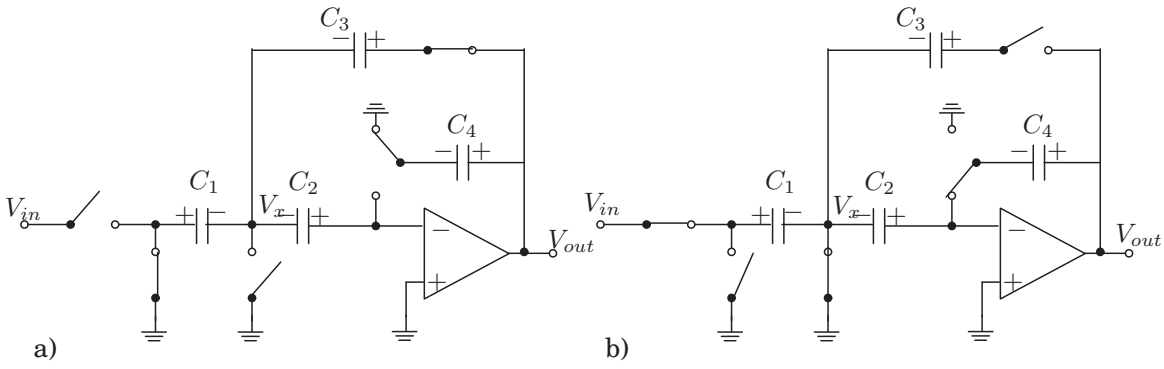

Figure 3: a) SC-circuit in clock phase 1. b) SC-circuit in clock phase 2.

As $q_2(t) = 0$ and $q_2(t + \tau) = q_2(t + 2\tau)$ (26) also $q_2(t + 2\tau) = 0$ and $V_x(t + 2\tau) = 0$, which means that $V_x(t) = 0$ for all t.
Furthermore equation (30) gives:

$$(0 - V_x(t))C_2 - (V_{out}(t) - 0)C_4 = 0 - (V_{out}(t + \tau) - 0)C_4 \tag{33}$$

As $V_x(t) = 0$ equation (33) gives that:

$$V_{out}(t + \tau) = V_{out}(t) \tag{34}$$

As q_2 is zero for all t and $q_3(t + \tau) = q_3(t)$ equation (32) yields:

$$(V_{in}(t+\tau)-0)C_1+(V_{out}(t)-V_x(t))C_3 = (0-V_x(t+2\tau))C_1+(V_{out}(t+2\tau)-V_x(t+2\tau))C_3 \tag{35}$$

Using $V_x = 0$ for all t equation (35) can be simplified to:

$$V_{in}(t + \tau)C_1 + V_{out}(t)C_3 = V_{out}(t + 2\tau)C_3 \tag{36}$$

Since $V_{in}(t + \tau) = V_{in}(t)$ (given in the exercise) equation (36) yields:

$$V_{in}(t)C_1 + V_{out}(t)C_3 = V_{out}(t + 2\tau)C_3 \tag{37}$$

Setting $2\tau = T$ gives the differens equation:

$$C_1V_{in}(t) + C_3V_{out}(t) = C_3V_{out}(t + T) \tag{38}$$

Finally, z-transforming (38):

$$C_1V_{in}(z) + C_3V_{out}(z) = C_3zV_{out}(z) \tag{39}$$

Which gives the answer:

$$\underline{\underline{V_{out}(z) = \frac{C_1}{C_3} \cdot \frac{1}{z - 1} \cdot V_{in}}}$$

b) Switches, capacitors, and the operational amplifier introduce parasitic capacitors into the circuit as is shown in Figure 4.

   * C_{pa} is connected between the ideal input voltage source and ground where the input source can source/sink as much charge as is required. Hence, this parasitics do not change the transfer function.

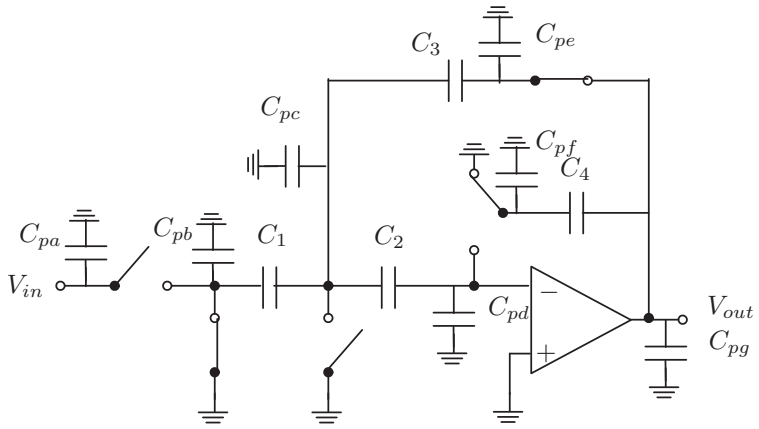

Figure 4: SC-circuit with parasitics in clock phase 1.

- C_{pb} is in one clock phase shorted to ground and the next connected to the ideal voltage source. Thus, the charge on the capacitor does not discharge into a sensitive node and this parasitic will not be part of the transfer function.
- C_{pc} is in one clock phase connected to virtual ground ($V_x = 0$) and the next connected to ground. Hence the transfer function will not be affected.
- C_{pd} is always connected to virtual ground and will not be part of the transfer function.
- C_{pe} is in one clock phase connected to the ideal output and the next connected to a floating node. Hence the transfer function will not be affected.
- C_{pf} is either shorted to ground or connected to virtual ground so the transfer function is not changed.
- C_{pg} is always connected to the ideal output of the operational amplifier and ground and thereby will not be a part of the transfer function.

Hence, the circuit is not sensitive to capacitive parasitics when the transfer function is of concern.

Exercise 4.

a) **Figure 5 a)** shows signal scheme and **figure 5 b)** small signal equivalent circuit (SSEC).

The signal scheme obtains by: 1) replacing voltage sources V_{DD} and V_{bias} with short circuits, 2) replacing current source with open circuit,3) putting input signals to zero and intoduce voltage V_n at ground node.

Following relationships: $g_{ds1} = g_{ds3}$, $g_{ds2} = g_{ds4}$, $g_{m1} = g_{m3}$, $g_{ds01} = g_{ds03}$, $g_{m01} = g_{m02}$, has been used in the SSEC.

Nodal analysis with respect to nodes y, x and out in SSEC gives: (Note that $V_z = V_{out}$ because of symmetri in the circuit.)

$$\text{y:} \quad g_{m02}(V_y - V_n) + g_{ds02}(V_y - V_n) = 0 \Rightarrow V_y = V_n \tag{40}$$

$$\text{x:} \quad 2(-g_{m3}V_x + g_{ds3}(V_{out} - V_x)) = g_{ds02}(V_x - V_n) \tag{41}$$

$$\text{out:} \quad -g_{ds4}V_{out} = g_{ds3}(V_{out} - V_x) - g_{m3}V_x \tag{42}$$

Equations (40)-(42) gives:

$$A_{GND} = \frac{V_{out}}{V_n} = \frac{(g_{m3} + g_{ds3})g_{ds02}}{g_{ds02}(g_{ds3} + g_{ds4}) + 2g_{ds4}(g_{m3} + g_{ds3})}$$

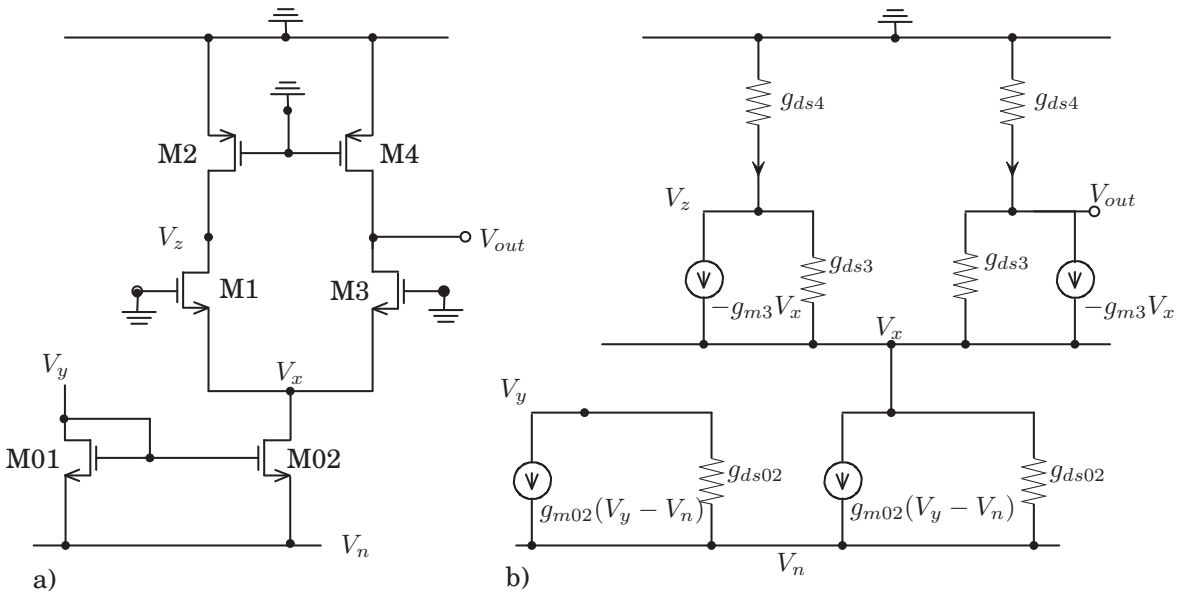

Figure 5: Small signal scheme and SSEC for differential gain-stage with single-ended output.

PSRR with respect to GND obtains from:

$$PSRR_n = \frac{A_{single}}{A_{GND}} = A_{single} \cdot \frac{g_{ds02}(g_{ds3} + g_{ds4}) + 2g_{ds4}(g_{m3} + g_{ds3})}{(g_{m3} + g_{ds3})g_{ds02}}$$

which can redraws as

$$\underline{\underline{PSRR_n = A_{single} \cdot \left(\frac{g_{ds3} + g_{ds4}}{g_{m3} + g_{ds3}} + \frac{2g_{ds4}}{g_{ds02}} \right)}}$$

b) $A_{single} \approx \frac{g_{m3}}{g_{ds3}+g_{ds4}}$ yields

$$PSRR_n \approx \frac{g_{m3}}{g_{ds3} + g_{ds4}} \cdot \left(\frac{g_{ds3} + g_{ds4}}{g_{m3} + g_{ds3}} + \frac{2g_{ds4}}{g_{ds02}} \right) = \frac{g_{m3}}{g_{m3} + g_{ds3}} + \frac{g_{m3}}{g_{ds3} + g_{ds4}} \cdot \frac{2g_{ds4}}{g_{ds02}}$$

Generally $g_m >> g_{ds}$ so the first term in this expression is approximately 1, and as g_{ds} is about the same for all transistors the second term is approximately g_{m3}/g_{ds02} i.e.

$$PSRR_n \approx 1 + \frac{g_{m3}}{g_{ds02}}$$

$PSRR_n$ can be increased by decreasing g_{ds02}, i.e. by increasing the output resistans of the current mirror yielding the source current to be more of an ideal source current.

c) Exactly the same calculations as in a). As, for the fully differential gain-stage, $V_{out} = V_{outp} - V_{outn}$, where $V_{outp} = V_{out}$ and $V_{outn} = V_z$ refering to **figure 5 b**, $V_{out} = 0$ in the fully differential case because $V_{out} = V_z$ refering to the solution in a). Which gives

$$A_{GND} = \frac{V_{out}}{V_n} = 0$$

and

$$PSRR_n = \frac{A_{diff}}{A_{GND}} = \infty$$

This indicates one of the benefits of a fully differential structure, i.e. it suppresses variations in source voltages better than a single-ended topology.

d) If mismatch exists between transistors M2 and M4, as well as between M1 and M3 the relationship $V_{outp} = V_{outn}$ no longer will be correct, as the circuit isn´t symmetric any more, whereby A_{GND} no longer is zero and $PSRR_n$ decreases.

Exercise 5.

a) The output noise spectral density can be computed by by the following formula

$$S_{out}(\omega) = |H(\omega)|^2 S_{in}(\omega) \tag{43}$$

where $H(\omega)$ is the transfer function from the noise source output node.
Determin the transfer function from the positive input node to the output of the operational amplifier, while the input voltage is zeroed:

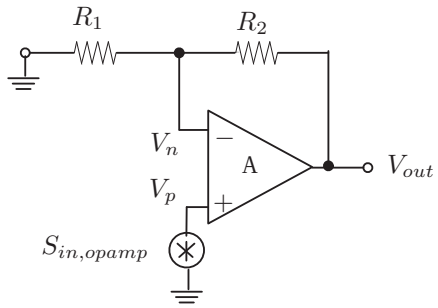

Figure 6: Determing $H = V_{out}/V_p$.

$$\begin{aligned} (0 - V_n)G_1 &= (V_n - V_{out})G_2 \\ (V_p - V_n)A &= V_{out} \end{aligned} \tag{44}$$

Solving this system of equation results in

$$H = \frac{V_{out}}{V_p} = \frac{G_1 + G_2}{G_2 + (G_1 + G_2)/A} = \frac{(G_1 + G_2)g_{m1}}{G_2 g_{m1} + (G_1 + G_2)g_{out}} \tag{45}$$

Hence, the equivalent output noise spectral density is given by

$$S_{out} = |H|^2 \cdot S_{in,opamp} = \left(\frac{(G_1 + G_2)g_{m1}}{G_2 g_{m1} + (G_1 + G_2)g_{out}} \right)^2 \cdot S_{in,opamp} \tag{46}$$

Using the fact that the ratio between the resistors is equal to a gives the answer:

$$\underline{\underline{S_{out} = \frac{(1+a)^2 g_{m1}}{(g_{m1} + (1+a)g_{out})^2} \cdot \frac{16kT}{3}(1 + \frac{g_{m4}}{g_{m1}})}} \tag{47}$$

b) The noise at the output can be decreased by increasing the transconductance g_{m1} of the input stage. This decreases the last term in Equation (47) while the first part is not changed so much. This will increase the gain of the amplifier.