# fpSolutions to Written Test
# TSTE80,
# Analog and Discrete-time Integrated Circuits

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| Date: | August 14, 2004 |
| Time: | 14 – 18 |
| Place: | TER1 |
| Max. no of points: | 70;<br>40 from written test,<br>15 for project, and 15 for assignments. |
| Grades: | 30 for 3, 42 for 4, and 56 for 5. |
| Allowed material: | All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries. |
| Examiner: | Lars Wanhammar. |
| Responsible teacher: | Robert Hägglund.<br>Tel.: 0705 - 48 56 88. |
| Correct (?) solutions: | Solutions and results will be displayed in House B, entrance 25 - 27, ground floor. |

## Good Luck!

# Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

# Solutions

**1. Large-signal analysis**

In analog circuit design, it is common to deal with differential amplifiers, either as a single amplifier or as a part of an operational amplifier. In this assignment, a differential amplifier is to be analyzed. Assume that all the transistors are biased in saturation and neglect the body effect. The current through transistor $M_5$ is $I_{\text{bias}}$.

a) Derive expressions for the common-mode range of the circuit shown in Figure 1.1 as a function of relevant design parameters.

The common-mode range is the range between the minimum and maximum possible input voltage so that all transistors are operating in the saturation region. In saturation the drain-source voltage is larger that the gate-source voltage minus the threshold voltage, i.e., $V_{DS} > V_{GS} - V_T > 0$.

To determine the minimum input voltage we start at the ground terminal and identify the minimum required voltage for each transistor to ensure saturated transistors. In this case

$$V_{in,\,min} = V_{DS,\,sat,\,5} + V_{GS,\,1} = V_{DS,\,sat,\,5} + V_{DS,\,sat,\,1} + V_{T,\,1}$$
$$= \sqrt{\frac{I_{\text{bias}}}{\alpha_5}} + \sqrt{\frac{I_{\text{bias}}}{2\alpha_1}} + V_{T,\,1}\text{‘} \qquad (1.1)$$

For the maximum input voltage, the voltage drop from the power supply to the input is computed. This results in

$$V_{\text{in, max}} = V_{\text{DD}} - V_{SG,\,3} - V_{DS,\,sat,\,1} + V_{GS,\,1} = V_{\text{DD}} - V_{SD,\,sat,\,3} - V_{T,\,3} + V_{T,\,1}$$
$$= V_{\text{DD}} - \sqrt{\frac{I_{\text{bias}}}{2\alpha_3}} - V_{T,\,3} + V_{T,\,1} \qquad (1.2)$$

Hence, the common-mode range can be expressed as

$$\text{CMR} = [V_{\text{in, min}}; V_{\text{in, max}}] \qquad (1.3)$$

b) Derive expressions for the output range of the circuit shown in Figure 1.1 as a function of relevant design parameter. Assume that the

input common-mode DC voltage is $V_{\text{in,DC}} = V_{\text{DD}}/2$.

The minimum possible output voltage for saturated transistors assuming that the input voltage is small is

$$V_{out,\,min} = V_{DS,\,sat,\,5} + V_{DS,\,sat,\,2} = \sqrt{\frac{I_{\text{bias}}}{\alpha_5}} + \sqrt{\frac{I_{\text{bias}}}{2\alpha_2}} \tag{1.4}$$

However, if the input signal is not small, the minimum possible voltage at the output is increased. In order to ensure that the input transistor is operating in the saturation region the following expression must be satisfied

$$V_{GS,\,1} - V_{T,\,1} < V_{DS,\,sat,\,1} \tag{1.5}$$

This can be rewritten as

$$V_{\text{in,\,DC}} - V_c - V_{T,\,1} < V_{\text{out}} - V_c \Rightarrow V_{\text{out}} > V_{\text{in,\,DC}} - V_{T,\,1} \tag{1.6}$$

Hence, the minimum possible output voltage in the DC operation point can be expressed as

$$V_{\text{out,\,min}} = max\left\{\sqrt{\frac{I_{\text{bias}}}{\alpha_5}} + \sqrt{\frac{I_{\text{bias}}}{2\alpha_1}}; V_{\text{in,\,DC}} - V_{T,\,1}\right\} \tag{1.7}$$

where the second term is usually larger than the first term.

The maximum output voltage is only limited by the smallest voltage drop from the power supply voltage. Hence,

$$V_{\text{out,\,max}} = V_{\text{DD}} - V_{SD,\,sat,\,3} = V_{\text{DD}} - \sqrt{\frac{I_{\text{bias}}}{2\alpha_3}} \tag{1.8}$$

The output range is given by

$$\text{OR} = [V_{\text{out,\,min}}; V_{\text{out,\,max}}] \tag{1.9}$$

c) Determine the widths of the transistors $M_1 - M_5$ to obtain $\text{CMR} = [\text{CMR}_{\text{min}}, \text{CMR}_{\text{max}}]$ and $\text{OR} = [\text{OR}_{\text{min}}, \text{OR}_{\text{max}}]$ where $\text{CMR}_{\text{min}}$, $\text{CMR}_{\text{max}}$, $\text{OR}_{\text{min}}$, and $\text{OR}_{\text{max}}$ are given. The lengths of all transistors are $L$. Note that several solutions exists.

The width of transistors $M_3$ and $M_4$ is computed from Eq. (1.8) according to

$$\text{OR}_{\text{max}} = V_{\text{DD}} - \sqrt{\frac{I_{\text{bias}}}{2\alpha_3}} \Rightarrow \alpha_3 = \frac{2I_{\text{bias}}}{(V_{\text{DD}} - \text{OR}_{\text{max}})^2} \Rightarrow W_3 = \frac{I_{\text{bias}} L}{\mu_o C_{ox} (V_{\text{DD}} - \text{OR}_{\text{max}})^2}$$

The minimum output voltage is set directly by the common-mode voltage at the input as long as $V_{DS,\,sat,\,5} + V_{DS,\,sat,\,1} < V_{\text{in,\,DC}} - V_{T,\,1}$.

The maximum common-mode voltage results in a lower bound on the device size of transistor $M_5$.

$$\mathrm{CMR}_{\max} = V_{\mathrm{DD}} - \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}} - V_{T,3} + V_{T,1} \Rightarrow$$

$$\Rightarrow W_5 > \frac{I_{\mathrm{bias}} L}{\mu_o C_{ox}(V_{\mathrm{DD}} - \mathrm{CMR}_{\max} - V_{T,3} + V_{T,1})^2} \tag{1.10}$$

This results in that $V_{DS,sat,5} < \sqrt{I_{\mathrm{bias}} / W_{5,\min}}$. We also know that

$$V_{DS,sat,1} + V_{DS,sat,5} \leq V_{\mathrm{in,min}} - V_{T,1} \tag{1.11}$$

and

$$V_{DS,sat,1} + V_{DS,sat,5} \leq V_{\mathrm{out,min}} \tag{1.12}$$

Using Eq. (1.10) –Eq. (1.12) we can determine an expression for the size of the input transistors.

$$V_{DS,sat,5} = \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}} \tag{1.13}$$

Hence,

$$V_{DS,sat,1} \leq V_{\mathrm{in,min}} - V_{T,1} - \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}} \Rightarrow$$

$$\Rightarrow W_1 \geq \frac{I_{\mathrm{bias}} L}{\mu_0 C_{ox}\left(V_{\mathrm{in,min}} - V_{T,1} - \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}}\right)^2} \tag{1.14}$$

and

$$V_{DS,sat,1} \leq V_{\mathrm{out,min}} - \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}} \Rightarrow$$

$$\Rightarrow W_1 \geq \frac{I_{\mathrm{bias}} L}{\mu_0 C_{ox}\left(V_{\mathrm{out,min}} - \sqrt{\frac{I_{\mathrm{bias}}}{\alpha_5}}\right)^2} \tag{1.15}$$

d) Show that $V_x = V_{\mathrm{out}}$ in the operation point ($V_{\mathrm{in},a} = V_{\mathrm{in},b}$) for the circuit in Figure 1.1 given that the transistors $M_1$, $M_2$ and $M_3$, $M_4$ are perfectly matched. Hint: Assume that $V_{\mathrm{out}} > V_x$ and show that it will result in a contradiction.

Assume that $V_{\mathrm{out}} > V_x$. This results that the current through $M_3$ is larger than through $M_4$. However, the gate-source voltage of both input transistors is equal, the current through transistor $M_2$ must be larger than through transistor $M_1$, since the drain-source voltage is larger for M2. Hence, this is a contradiction. The same procedure can be carried out for the case $V_{\mathrm{out}} < V_x$. Hence, in the DC operation point with perfectly matched devices the following equation must hold $V_{\mathrm{out}} = V_x$.

e) Compute the output voltage, $V_{\mathrm{out,DC}}$, in the operation point

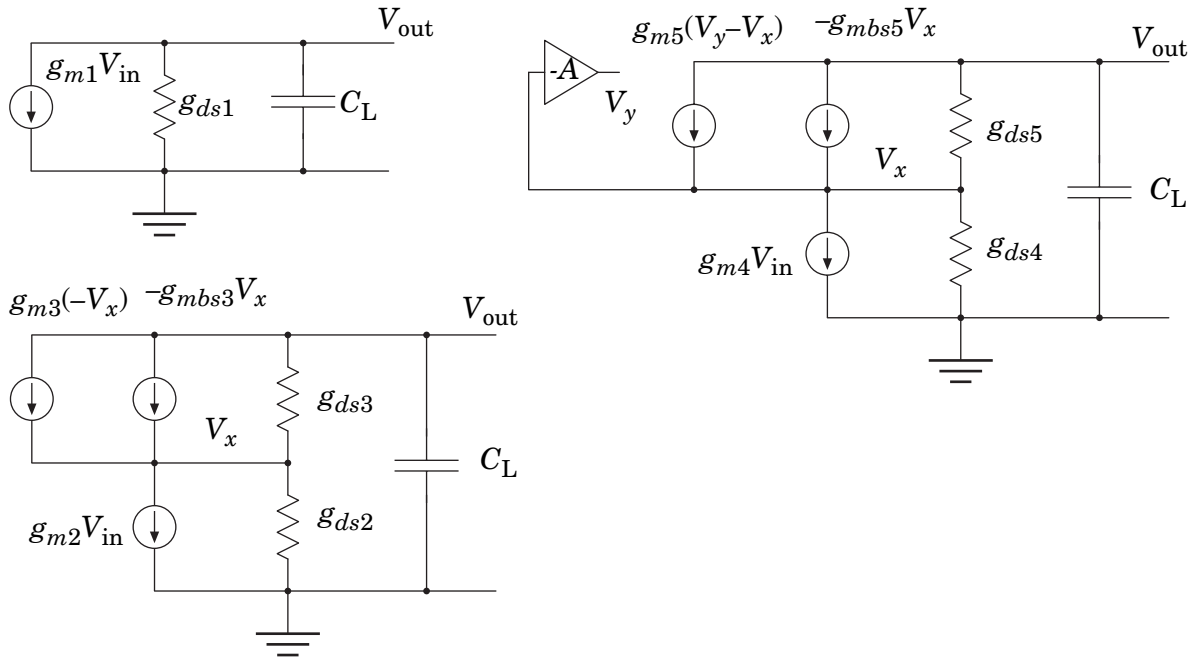


***Figure 2.1*** The small-signal model of the common-source amplifier with cascodes.

($V_{\text{in},a} = V_{\text{in},b}$) as a function of the bias current and transistor sizes. Neglect the influence of the channel-length modulation.

We from the previous assignment know that $V_{\text{out}} = V_x$. The voltage in $V_x$ can be expressed as

$$0.5I_{\text{bias}} = \alpha_3(V_{SG,3} - V_{T,3})^2 = \alpha_3(V_{\text{DD}} - V_x - V_{T,3})^2 \qquad (1.16)$$

Hence,

$$V_x = V_{\text{DD}} - V_{T,3} - \sqrt{\frac{I_{\text{bias}}}{2\alpha_3}} \qquad (1.17)$$

## 2. Small-signal analysis

The transistors in the circuits shown in Figure 2.1a-c are biased in the saturation region and their sizes are equal, i.e., $W_i/L_i = W/L$ for all $i$. Further, the load capacitances are also equally large and $A \gg 1$. Neglect the influence of all internal parasitics in the transistors.

a) Derive approximate expressions for $g_{m,i}$ and $g_{ds,i}$ for $i = 2, 3, 4, 5$ as a function of $g_{m,1}$ and $g_{ds,1}$, respectively.

The sizes of all the transistors are equal and the same current is passing through the transistors. Hence, all the transconductances are equal and the same applies for the output conductances.

b) Draw the small-signal models of the three amplifiers shown in Figure 2.1 a-c. Do not neglect the influence of the bulk effect.

The small-signal model of the amplifier is shown in Figure 2.1

c) Compute the small-signal transfer functions, $H(s) = V_{\text{out}}(s)/V_{\text{in}}(s)$, for the circuits shown in Figure 2.1a-c. Neglect the influence of the bulk

effect.

Starting with the common-source amplifier and perform a nodal analysis in the output node. The result is

$$g_{m1}V_{\text{in}} + g_{ds1}V_{\text{out}} + sC_L V_{\text{out}} = 0 \tag{2.1}$$

And the transfer function is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{g_{m1}}{g_{ds1}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}}{C_L}}} \tag{2.2}$$

The next stage is the common-source amplifier with cascodes. Here two equations are obtained from the nodal analysis.

$$g_{m2}V_{\text{in}} + g_{ds2}V_x + g_{m3}V_x + (V_x - V_{\text{out}})g_{ds3} = 0 \tag{2.3}$$

$$g_{m3}V_x + (V_x - V_{\text{out}})g_{ds3} - V_{\text{out}}sC_L = 0 \tag{2.4}$$

Solving for $V_x$ in Eq. (2.4) results in

$$V_x = \frac{g_{ds3} + sC_L}{g_{m3} + g_{ds3}}V_{\text{out}} \tag{2.5}$$

Inserting this into Eq. (2.3) gives

$$g_{m2}V_{\text{in}} = V_{\text{out}}\left(g_{ds3} - (g_{m3} + g_{ds2} + g_{ds3})\frac{g_{ds3} + sC_L}{g_{m3} + g_{ds3}}\right) \tag{2.6}$$

and the transfer function is

$$\begin{aligned}\frac{V_{\text{out}}}{V_{\text{in}}} &= -\frac{g_{m2}(g_{m3} + g_{ds3})}{g_{ds2}g_{ds3}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds2}g_{ds3}}{(g_{m3} + g_{ds2} + g_{ds3})C_L}}} \approx \\ &\approx -\frac{g_{m2}}{\dfrac{g_{ds2}g_{ds3}}{g_{m3}}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds2}g_{ds3}}{g_{m3}C_L}}}\end{aligned} \tag{2.7}$$

The last stage is the common-source amplifier with gain-boosting. Here, only two equations are required.

$$g_{m2}V_{\text{in}} + g_{ds2}V_x + g_{m3}V_x(1 + A) + (V_x - V_{\text{out}})g_{ds3} = 0 \tag{2.8}$$

$$g_{m3}V_x(1 + A) + (V_x - V_{\text{out}})g_{ds3} - V_{\text{out}}sC_L = 0 \tag{2.9}$$

Solving for $V_x$ in Eq. (2.9) gives the following result

$$V_x = \frac{g_{ds3} + sC_L}{g_{m3}(1+A) + g_{ds3}} V_{\text{out}} \tag{2.10}$$

Inserting this into Eq. (2.8) results in

$$g_{m2} V_{\text{in}} = V_{\text{out}} \left( g_{ds3} - (g_{m3}(1+A) + g_{ds2} + g_{ds3}) \frac{g_{ds3} + sC_L}{g_{m3}(1+A) + g_{ds3}} \right) \tag{2.11}$$

and the resulting transfer function is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{g_{m2}(g_{m3}(1+A) + g_{ds3})}{g_{ds3} g_{ds2}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{ds3} g_{ds2}}{(g_{m3}(1+A) + g_{ds2} + g_{ds3}) C_L}}} \approx$$

$$\approx -\frac{g_{m2}}{\dfrac{g_{ds3} g_{ds2}}{g_{m3} A}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{ds2} g_{ds3}}{g_{m3} A C_L}}} \tag{2.12}$$

d) Rank the three stages with respect to the DC gain, first pole, and gain-bandwidth product.

The three stages are the common-source amplifier, common-source with cascodes, and common-source with gain-boosting.

If high gain is required gain-boosting is a good choice since this stage has highest DC gain. The cascode stage is on second place while the regular common-source amplifier has lowest DC gain.

The opposite ranking is the case for the first pole, i.e., common-source amplifier has the first pole highest up in frequency.

The gain-bandwidth product of the amplifiers are approximately equal since the

$$A_0 p_1 \approx \frac{g_{m,\text{in}}}{g_{\text{out}}} \frac{g_{\text{out}}}{C_L} = \frac{g_{m,\text{in}}}{C_L} \approx \text{constant} \tag{2.13}$$

## 3. Operational amplifiers

A commonly used building block in analog filtering applications is shown in Figure 3.1.

a) Derive the transfer function from the input of the circuit to its output, i.e., $H(s) = V_{\text{out}}(s)/V_{\text{in}}(s)$. Assume that all operational amplifiers are ideal.

The transfer function can be derived into several partial transfer functions (see Figure 3.1).

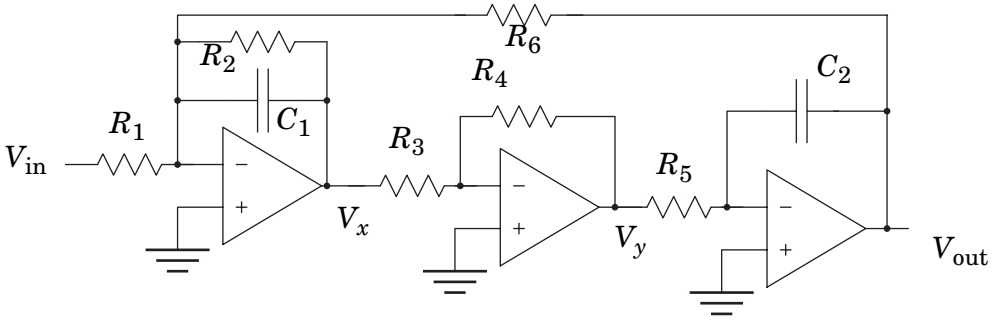


***Figure 3.1*** A Tow-Thomas biquad.

$$V_{\text{out}}(s) = -\frac{1}{sC_2R_5}V_y(s) \tag{3.1}$$

$$V_y(s) = -\frac{R_4}{R_3}V_x(s) \tag{3.2}$$

$$V_x(s) = -\frac{R_2}{R_1(1+sR_2C_1)}V_{\text{in}}(s) - \frac{R_2}{R_6(1+sR_2C_1)}V_{\text{out}}(s) \tag{3.3}$$

Substituting Eq. (3.2) and Eq. (3.3) into Eq. (3.1) yields

$$V_{\text{out}}(s) = -\frac{1}{sC_2R_5}\frac{R_4}{R_3}\left(\frac{R_2}{R_1(1+sR_2C_1)}V_{\text{in}}(s) + \frac{R_2}{R_6(1+sR_2C_1)}V_{\text{out}}(s)\right)$$

which is reformulated to

$$V_{\text{out}}(s)\left(1 + \frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_6(1+sR_2C_1)}\right) = -\frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_1(1+sR_2C_1)}V_{\text{in}}(s)$$

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{-\frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_1(1+sR_2C_1)}}{1 + \frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_6(1+sR_2C_1)}} = -\frac{R_2}{R_1}\frac{R_4R_6}{(1+sR_2C_1)sC_2R_3R_5R_6 + R_2R_4} =$$

$$-\frac{R_2}{R_1}\frac{R_4R_6}{R_2R_4 + sC_2R_3R_5R_6 + s^2C_1C_2R_2R_3R_5R_6}$$

b) Consider only the second stage, consisting of resistors $R_3$ and $R_4$ and the operational amplifier. The input terminal is to the left of resistor $R_3$, $V_x$, and the output is at the output of the operational amplifier, $V_y$. For this stage, compute the input and output referred noise spectral densities caused by the thermal noise generated by the resistors. Assume that the operational amplifier is noiseless and has the following transfer function.

$$\frac{V_{\text{op amp, out}}}{V_{\text{op amp, in, diff}}} = A_0 \tag{3.4}$$

The input terminal is to the left of resistor $R_3$, $V_x$, and the output is at the output of the operational amplifier, $V_y$.

The characteristics of the amplifier is as follows.

$$V_y = A_0(V_\text{p} - V_\text{n}) = -A_0 V_\text{n} \tag{3.5}$$

where $V_\text{n}$ is the voltage at the negative input terminal of the operational amplifier. Further, the rest of the circuit can be expressed by a single nodal equation at $V_\text{n}$ according to

$$(V_x - V_\text{n})G_3 + (V_y - V_\text{n})G_4 = 0 \tag{3.6}$$

Combining these equations results in

$$V_x G_3 + V_y G_4 = -\frac{1}{A_0}(G_3 + G_4)V_y \tag{3.7}$$

Solving for $V_y$ gives

$$-V_x G_3 A_0 = (G_3 + G_4 + G_4 A_0)V_y \tag{3.8}$$

and

$$H_1 = \frac{V_y}{V_x} = -\frac{G_3 A_0}{G_3 + G_4 + A_0 G_4} \tag{3.9}$$

The transfer functions from the noise caused by the resistors to the output are also required. Starting with the noise generated by $R_3$. Here, we model the noise source as a current noise source in parallel with the resistor. The noise current source spectral density is

$$I_{R3}^2(f) = \frac{4kT}{R_3} \tag{3.10}$$

Solving for the transfer function gives

$$I_{R3} + (0 - V_n)G_3 + (V_y - V_n)G_4 = 0 \tag{3.11}$$

Solving for $V_y$ results in

$$H_2 = \frac{V_y}{I_{R3}} = -\frac{A_0}{G_3 + G_4 + A_0 G_4} \tag{3.12}$$

For the resistor $R_4$ the transfer function to the output is

$$-V_n G_3 + (V_y - V_n)G_4 + I_{R4} = 0 \tag{3.13}$$

the resulting transfer function is

$$H_3 = \frac{V_y}{I_{R4}} = -\frac{A_0}{G_3 + G_4 + A_0 G_4} \tag{3.14}$$

The equivalent output referred noise spectral density is computed according to

$$S_{\text{out}}(f) = \sum \left|H_i^2\right| S_i(f) = \frac{A_0^2}{(G_3 + G_4(1 + A_0))^2}(I_{R3}^2 + I_{R4}^2) =$$

$$= 4kT\frac{A_0^2}{(G_3 + G_4(1 + A_0))^2}(G_3 + G_4) \tag{3.15}$$

The equivalent input referred noise spectral density is computed according to

$$S_{\text{in}}(f) = \frac{S_{\text{out}}(f)}{\left|H_1\right|^2} = 4kT\frac{(G_3 + G_4)}{G_3^2} = \frac{4kT}{G_3}\left(1 + \frac{G_4}{G_3}\right) \tag{3.16}$$

## 4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time $t$, $t + 2\tau$, $t + 4\tau$, etc. is shown in Figure 4.1. Assume that the input signals are constant between clock phase 1 and 2, i.e., $V_1(t) = V_1(t + \tau)$ and $V_2(t) = V_2(t + \tau)$.

a) Express the output voltage, $V_{\text{out}}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal.

Starting by assigning positive charge at the left plate of capacitor $C_1$, $C_2$, and $C_3$ and to the right of $C_4$.

The next step is to express the charge at the capacitors.

At time $t$

$q_1(t) = C_1 V_1(t)$, $q_2(t) = C_2 V_2(t)$, $q_3(t) = 0$, $q_4(t) = C_4 V_{out}(t)$

time $t + \tau$

$q_1(t + \tau) = C_1 V_2(t + \tau)$, $q_2(t + \tau) = C_2 V_1(t + \tau)$, $q_3(t + \tau) = C_3 V_1(t + \tau)$, $q_4(t + \tau) = C_4 V_{out}(t + \tau)$

and at time $t + 2\tau$

$q_1(t + 2\tau) = C_1 V_1(t + 2\tau)$, $q_2(t + 2\tau) = C_2 V_2(t + 2\tau)$, $q_3(t + 2\tau) = 0$, $q_4(t + 2\tau) = C_4 V_{out}(t + 2\tau)$

The charge conservation equations are

$$q_1(t) + q_4(t) = q_1(t + \tau) + q_4(t + \tau) \tag{4.1}$$

$$q_2(t + \tau) + q_3(t + \tau) + q_4(t + \tau) =$$
$$q_2(t + 2\tau) + q_3(t + 2\tau) + q_4(t + 2\tau) \tag{4.2}$$

The Eq. (4.1) results in

$$C_1 V_1(t) + C_4 V_{out}(t) = C_1 V_2(t + \tau) + C_4 V_{out}(t + \tau) \tag{4.3}$$

Furthermore, Eq. (4.2) results in

$$C_2V_1(t+\tau) + C_3V_1(t+\tau) + C_4V_{out}(t+\tau) = \\ = C_2V_2(t+2\tau) + C_4V_{out}(t+2\tau) \quad (4.4)$$

Solving the system of equations given by Eq. (4.3) and Eq. (4.4) results in

$$C_2V_1(t+\tau) + C_3V_1(t+\tau) + C_1V_1(t) + C_4V_{out}(t) - C_1V_2(t+\tau) = \\ = C_2V_2(t+2\tau) + C_4V_{out}(t+2\tau) \quad (4.5)$$

Further, from the assignment we know that $V_1(t) = V_1(t+\tau)$ and $V_2(t) = V_2(t+\tau)$. This gives the following equation

$$(C_1 + C_2 + C_3)V_1(t) - C_1V_2(t) - C_2V_2(t+2\tau) = C_3(V_{out}(t+2\tau) - V_{out}(t)) \quad (4.6)$$

Performing a Z-transformation on this equation gives the results

$$C_4V_{out}(z)[z-1] = V_1(z)[C_1 + C_2 + C_3] - V_2(z)[C_2z + C_1] \quad (4.7)$$

Hence, the output quantity can be expressed as

$$V_{out}(z) = \frac{1}{C_4}\frac{V_1(z)[C_1 + C_2 + C_3] - V_2(z)[C_2z + C_1]}{z-1} \quad (4.8)$$

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The parasitics of interest are shown in Figure 4.1.

$C_{pa}$, $C_{pb,}C_{pc,}C_{pk}$ do not alter the transfer function since they are always connected to the ideal input source.

$C_{pd}$,$C_{pj}$ are connected between ground and virtual ground or ground and ground and thereby do not change the transfer function.

$C_{pe}$, $C_{ph}$, $C_{pi}$, $C_{pm}$ are shorted between ground and ground and thereby do not change the transfer function.

$C_{pf}$ is connected between ground and virtual ground and thereby does not change the transfer function.

$C_{pg}$ Connected between ground and the output node of the OP amp which can generate and sink as much charge as required. No effect on the transfer function.

$C_{pl}$ Connected between ground and ground or ground and the ideal input voltage source. No effect on the transfer function.

Hence, the circuit is insensitive to capacitive parasitics, when the transfer function is of concern.

c) Express the output voltage, $V_{\text{out}}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA suffers from an offset voltage, $V_{\text{os}}$.

The next step is to express the charge at the capacitors.

At time $t$

$q_1(t) = C_1V_1(t)$, $q_2(t) = C_2(V_2(t) - V_{os})$, $q_3(t) = C_3(0 - V_{os})$, $q_4(t) = C_4(V_{out}(t) - V_{os})$

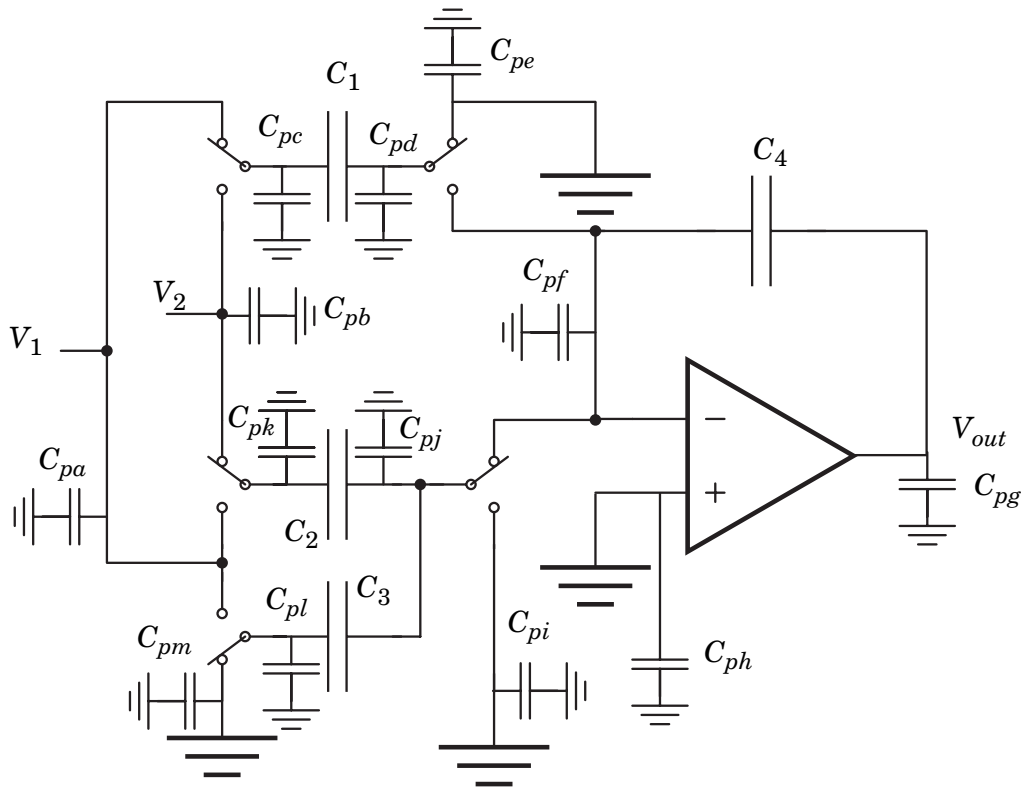


***Figure 4.1*** The SC circuit with capacitive parasitics due to the capacitor and the switches.

time $t + \tau$

$q_1(t+\tau) = C_1(V_2(t+\tau) - V_{os})$, $q_2(t+\tau) = C_2 V_1(t+\tau)$,
$q_3(t+\tau) = C_3 V_1(t+\tau)$, $q_4(t+\tau) = C_4(V_{out}(t+\tau) - V_{os})$

and at time $t + 2\tau$

$q_1(t+2\tau) = C_1 V_1(t+2\tau)$, $q_2(t+2\tau) = C_2(V_2(t+2\tau) - V_{os})$,
$q_3(t+2\tau) = C_3(0 - V_{os})$, $q_4(t+2\tau) = C_4(V_{out}(t+2\tau) - V_{os})$

The charge conservation equations are

$$q_1(t) + q_4(t) = q_1(t+\tau) + q_4(t+\tau) \tag{4.9}$$

$$q_2(t+\tau) + q_3(t+\tau) + q_4(t+\tau) = q_2(t+2\tau) + q_3(t+2\tau) + q_4(t+2\tau) \tag{4.10}$$

The Eq. (4.1) results in

$$C_1 V_1(t) + C_4(V_{out}(t) - V_{os}) = C_1(V_2(t+\tau) - V_{os}) + C_4(V_{out}(t+\tau) - V_{os}) \tag{4.11}$$

Furthermore, Eq. (4.2) results in

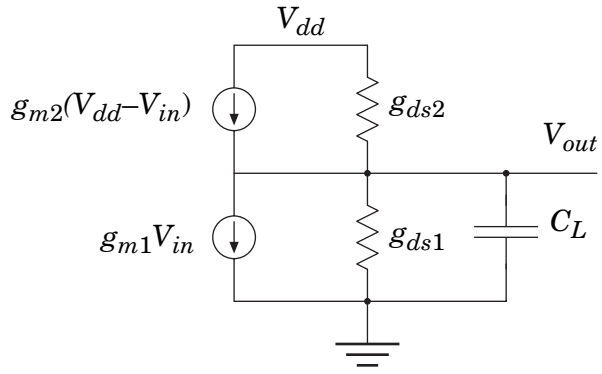


***Figure 5.1*** The small-signal model of a CMOS inverter.

$$C_2V_1(t+\tau) + C_3V_1(t+\tau) + C_4(V_{out}(t+\tau) - V_{os}) = \\ = C_2(V_2(t+2\tau) - V_{os}) + C_3(0 - V_{os}) + C_4(V_{out}(t+2\tau) - V_{os}) \quad (4.12)$$

Solving the system of equations given by Eq. (4.11) and Eq. (4.12) results in

$$C_2V_1(t+\tau) + C_3V_1(t+\tau) + C_1V_1(t) + C_4(V_{out}(t) - V_{os}) - C_1(V_2(t+\tau) - V_{os}) = \\ = C_2(V_2(t+2\tau) - V_{os}) + C_3(0 - V_{os}) + C_4(V_{out}(t+2\tau) - V_{os}) \quad (4.13)$$

Further, from the assignment we know that $V_1(t) = V_1(t+\tau)$ and $V_2(t) = V_2(t+\tau)$. This gives the following equation

$$(C_1 + C_2 + C_3)V_1(t) - C_1V_2(t) + (-C_2V_2(t+2\tau)) + V_{os}(C_1 + C_2 + C_3) = \\ C_4(V_{out}(t+2\tau) - V_{out}(t)) \quad (4.14)$$

Performing a Z-transformation on this equation gives the results

$$C_4V_{out}(z)[z-1] = V_1(z)[C_1 + C_2 + C_3] - V_2(z)[C_2z + C_1] + \\ + V_{os}(z)[C_1 + C_2 + C_3] \quad (4.15)$$

Hence, the output quantity can be expressed as

$$V_{out}(z) = \frac{V_1(z)[C_1 + C_2 + C_3] - V_2(z)[C_2z + C_1]}{C_4(z-1)} + \\ + \frac{V_{os}(z)[C_1 + C_2 + C_3]}{C_4(z-1)} \quad (4.16)$$

## 5. A mixture of questions

a) Compute the power supply rejection ratio from the positive power supply for the circuit shown in Figure 5.1.

The power supply rejection ratio is the ratio between the transfer function from the input to the output divided by the transfer function from the power supply to the output.

The transfer function from the input to the output can be computed by applying nodal analysis in the output node (where $V_{dd} = 0$ in Figure 5.1)

$$g_{m1}V_{in} + g_{m2}V_{in} + (g_{ds1} + g_{ds2} + sC_L)V_{out} = 0 \tag{5.1}$$

This results in the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + sC_L} \tag{5.2}$$

The transfer function from the power supply voltage to the output is (where $V_{in} = 0$ shown in Figure 5.1)

$$g_{m2}V_{dd} + (V_{dd} - V_{out})g_{ds2} + (0 - V_{out})(g_{ds1} + sC_L) = 0 \tag{5.3}$$

which results in

$$\frac{V_{out}}{V_{dd}} = \frac{g_{m2} + g_{ds2}}{g_{ds1} + g_{ds2} + sC_L} \tag{5.4}$$

Hence, the power supply rejection ration is

$$\text{PSRR} = \frac{V_{out}/V_{in}}{V_{out}/V_{dd}} = \frac{-\dfrac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + sC_L}}{\dfrac{g_{m2} + g_{ds2}}{g_{ds1} + g_{ds2} + sC_L}} = -\frac{g_{m1} + g_{m2}}{g_{m2} + g_{ds2}} \tag{5.5}$$

b) Why do we usually design a common-source amplifier so that the transistors operate in the saturation region?

A common-source amplifier usually has high DC gain this is possible to obtain if all transistors are biased in the saturation region. Further, high unity-gain frequency is also only possible if saturated transistors are used.

c) The amplifier stages shown in Figure 5.2 have positive gain. For each gain stage, determine which terminal, i.e., $V_1$ or $V_2$, that is the positive input.

Amplifier stage a) a differential gain stage with nmos transistors as input transistors. Increasing the voltage at terminal $V_1$ will increase the current through the left branch. Hence, the voltage at the diode connection will decrease. This will cause output voltage to increase. Thus, the terminal $V_1$ is the positive input terminal.

Amplifier stage b) a differential gain stage with pmos transistors as input devices. Increasing $V_1$ will decrease the current through the left branch. Thus, the voltage at the diode connection will decrease. This results in an increase at the output voltage. Hence, $V_1$ is the positive input terminal

Amplifier stage c) a twostage amplifier with nmos transistors as input devices. From a) we know that the output voltage of the differential gain stage increases if $V_1$ increases. This causes the output voltage of the whole amplifier to decrease. Hence, the positive input terminal is $V_2$.

d) Typically, when designing analog circuits, a bias network is designed to bias all transistors into their desired operation region. A simple biasing network for both NMOS and PMOS current sources are shown in Figure 5.3. Determine the possible interval of the biasing current for which all transistors in the circuit are saturated. Assume that transistors $M_1$ and $M_2$ are equally large and neglect the channel-length modulation.

Diode connected transistors have only two possible operation regions namely saturation and cut-off. The transistor $M_1$ will always be saturated since it is driven by an ideal current source which can set the voltage at the drain of $M_1$ to an arbitrarily value.

When the channel-length modulation is neglected and both $M_1$ and $M_2$ are saturated the current through $M_2$ equals $M_1$ which is equal to $I_{\text{bias}}$. It also means that

$$I_{\text{bias}} = \alpha_3(V_{\text{bias, 2}} - V_{T3})^2 \Rightarrow V_{\text{bias, 2}} = \sqrt{\frac{I_{\text{bias}}}{\alpha_3}} + V_{T3} \tag{5.6}$$

and

$$I_{\text{bias}} = \alpha_1(V_{DD} - V_{\text{bias, 1}} - V_{T,1})^2 \Rightarrow V_{\text{bias, 1}} = V_{DD} - \sqrt{\frac{I_{\text{bias}}}{\alpha_1}} - V_{T1} \tag{5.7}$$

In order to ensure that all transistors are operating in the saturation region, transistor M2 must be saturated, i.e.,

$$\begin{aligned} &0 < V_{SG,2} - V_{T2} < V_{SD,sat,2} \Rightarrow 0 < V_{DD} - V_{\text{bias, 1}} - V_{T2} < V_{DD} - V_{\text{bias, 2}} \Rightarrow \\ &-V_{DD} < -V_{\text{bias, 1}} - V_{T2} < -V_{\text{bias, 2}} \Rightarrow V_{DD} > V_{\text{bias, 1}} + V_{T2} > V_{\text{bias, 2}} \Rightarrow \\ &V_{DD} > V_{DD} - \sqrt{\frac{I_{\text{bias}}}{\alpha_1}} - V_{T1} + V_{T2} > \sqrt{\frac{I_{\text{bias}}}{\alpha_3}} + V_{T3} \end{aligned} \tag{5.8}$$

The first inequality gives that

$$0 > -\sqrt{\frac{I_{\text{bias}}}{\alpha_1}} \tag{5.9}$$

since $V_{T1} = V_{T2}$, which always is satisfied. The second inequality can be reformulated to

$$V_{DD} - V_{T3} > \sqrt{\frac{I_{\text{bias}}}{\alpha_3}} + \sqrt{\frac{I_{\text{bias}}}{\alpha_1}} \Rightarrow I_{\text{bias}} < \left( \frac{V_{DD} - V_{T3}}{\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_3}}} \right)^2 \tag{5.10}$$

Transistor $M_3$ will be saturated for all biasing currents. Hence Eq. (5.10) must be satisfied to ensure that all transistors are saturated.