Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date:	May 27, 2004
Time:	8 – 12
Place:	T1
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The three amplifiers shown in Figure 1.1 are commonly used in for example operational amplifiers. In this exercise the analysis of these amplifier is considered. All transistor should operate in the saturation region.

a) Determine the width-over-length ratios for the two transistors in Figure 1.1a for a given output range OR, $V_{out,\,DC} = (OR_{min} + OR_{max})/2$, and current through the transistors I. Do not neglect the channel-length modulation nor the body effect.

The output range is given as the voltage in which all transistors are operating in the saturation region. In order to ensure this the drain-source voltage must be at least as large as the effective voltage, i.e., the gate-source voltage minus the threshold voltage. Hence, the effective voltage for the NMOS transistor is OR_{min} while it is $V_{DD} - OR_{max}$ for the PMOS transistor. Further, we can express the currents through the transistors as

$$I = I_{D1} = \alpha_1 V_{eff1}^2 (1 + \lambda V_{out,\,DC}) = \alpha_1 \cdot OR_{min}^2 (1 + \lambda (OR_{min} + OR_{max})/2)$$

$$\begin{aligned} I = I_{D2} &= \alpha_2 V_{eff2}^2 (1 + \lambda (V_{DD} - V_{out,\,DC})) \\ &= \alpha_2 (V_{DD} - OR_{max})^2 (1 + \lambda (V_{DD} - (OR_{min} + OR_{max})/2)) \end{aligned}$$

In these equations the power supply voltage, the output ranges, and the current, I are given in the exercise. Hence, the width-over-length ratio can be derived by a simple rearrange in the equations. This results in

$$\frac{W_1}{L_1} = \frac{I}{OR_{min}^2 (1 + \lambda (OR_{min} + OR_{max})/2)} \cdot \frac{2}{\mu_n C_{ox}} \qquad (1.1)$$

and

$$\frac{W_2}{L_2} = \frac{I}{(V_{DD} - OR_{max})^2 (1 + \lambda (V_{DD} - (OR_{min} + OR_{max})/2))} \cdot \frac{2}{\mu_p C_{ox}}$$

b) Determine the width-over-length ration of the common drain circuit

shown in Figure 1.1b for given valus of the voltages $V_{in,DC}$, $V_{out,DC}$, V_{bias}, and the current through the transistors I. Do not neglect the channel-length modulation nor the body effect.

The current through the transistors is expressed as

$$I = I_{D1} = \alpha_1(V_{in,DC} - V_{out,DC} - V_{T,1})^2(1 + \lambda(V_{DD} - V_{out,DC}))$$

and

$$I = I_{D2} = \alpha_2(V_{bias} - V_{T,2})^2(1 + \lambda V_{out,DC})$$

Note that the threshold voltage for transistor 1 is increased due to the body effect. This results in a threshold voltage

$$V_{T,1} = V_{T0,1} + \gamma(\sqrt{2\phi_f + V_{out,DC}} + \sqrt{2\phi_F})$$

Since the DC output voltage is given in the exercise the threshold voltage, $V_{T,1}$, can be computed directly. Further, all the voltages are fixed due to the specification as well as the current, I. Hence, the width-over-length ratio can be solved by rearranging the two current equations. This results in

$$\frac{W_1}{L_1} = \frac{I}{(V_{in,DC} - V_{out,DC} - V_{T,1})^2(1 + \lambda(V_{DD} - V_{out,DC}))} \cdot \frac{2}{\mu_n C_{ox}}$$

and

$$\frac{W_2}{L_1} = \frac{I}{(V_{bias} - V_{T,2})^2(1 + \lambda V_{out,DC})} \cdot \frac{2}{\mu_n C_{ox}}$$

c) Determine the input range of the common-drain amplifier shown in Figure 1.1b for the same parameters as in exercise 1b. Neglect the channel-length modulation, but not the body effect. (This exercise can be solved even though exercise 1b is not solved.)

The input range is determined as the range in which all transistors are operating in the saturation region. In this case, the input transistor limits the maximum input voltage while the biasing transistor limits the minimum possible input voltage. Starting from the lower limit of the input range. First, the minimum output voltage is determined by ensuring that the bias transistor are operating in saturation. The biasing transistor is saturated if its saturation voltage is larger than the effective voltage, i.e.,

$$V_{out,min} = V_{DS,sat,2} = V_{eff,2} = V_{bias} - V_{T,2} \tag{1.2}$$

The current through the input transistor is then

$$I_{D1} = \alpha_1(V_{in,min} - V_{out,min} - V_{T,1})^2 \tag{1.3}$$

where the threshold voltage in this case is evaluated for the source voltage of $V_{out,min}$. The use of the minimum input and output voltage in Eq. (1.3) is a result of that the circuit is non inverting. From Eq. (1.3) the minimum input voltage can be solve according to

$$V_{in,\,min} = \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{out,\,min} + V_{T,\,1} = \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{bias} - V_{T,\,2} + V_{T,\,1}$$

Note, that the threshold voltage of the two transistors differ.

The maximum input voltage is determined by the input transistor. The drain-source voltage should be larger than the effective voltage, i.e.,

$$V_{DS,\,sat,\,1} = V_{DD} - V_{out,\,max} = V_{eff,\,1} = V_{in,\,max} - V_{out,\,max} - V_{T,\,1}$$

From this equation can solve for $V_{in,\,max} = V_{DD} + V_{T,\,1}$. Notice that the threshold voltage in this case is computed for the source voltage of $V_{out,\,max}$.

d) Determine the output range of the amplifier shown in Figure 1.1c as a function of the bias voltages, current, power supply voltage, and device parameters.

The maximum output voltage is determined by the saturation voltage of the PMOS transistor, i.e.,

$$V_{out,\,max} = V_{DD} - V_{SD,\,sat,\,2} = V_{DD} - V_{eff,\,2} = V_{bias2} - V_{T,\,2}$$

The minimum output voltage is determined as the voltage for which the transistor M1 is saturated. Hence, in this case the $V_{eff,\,1} = V_{DS,\,sat,\,1}$ which results in the following equation

$$V_{bias1} - V_{in,\,min} - V_{T,\,1} = V_{out,\,min} - V_{in,\,min} \tag{1.4}$$

Solving for the minimum output voltage results in

$$V_{out,\,min} = V_{bias1} - V_{T,\,1} \tag{1.5}$$

where $V_{T,\,1}$ is evaluated according to $V_{T,\,1} = V_{T0,\,1}$ since the minimum input voltage is assumed to be ground.

2. Small-signal analysis

The transistor in the circuit shown in Figure 2.1 is biased in the saturation region. Neglect the influence of all internal parasitics in the transistor.

a) Compute the small-signal transfer function of the circuit shown in Figure 2.1, $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect.

The small-signal model of the amplifier is shown in Figure 2.1

The transfer function from the input to the output is computed by for example applying nodal analysis. This gives the following equation

$$g_{m1}V_{in} + V_{out}(G + g_{ds} + sC_L) = 0 \tag{2.1}$$

This gives the transfer function

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{g_{m1}}{G + g_{ds} + sC_L} \tag{2.2}$$

b) How will the DC gain, unity-gain frequency and the first pole be changed when the supply current, I, increases (i.e., when the DC input voltage level is increased). Assume that $g_{ds} \ll 1/R$.

The DC gain, unity-gain frequency, and the first pole are given by

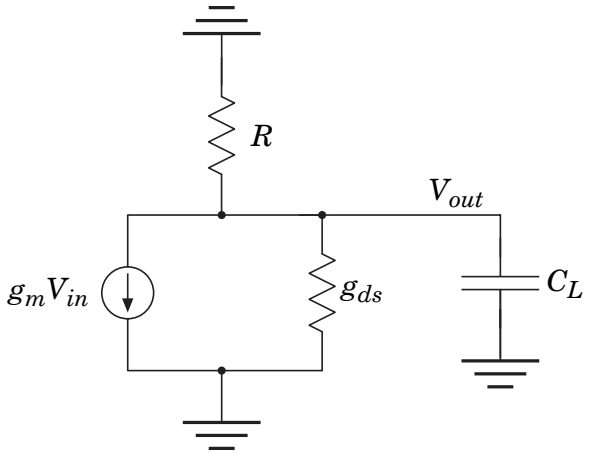

Figure 2.1 The small-signal model of the common-source amplifier with cascodes.

$$A_0 = -\frac{g_m}{g_{ds}+G} \approx -\frac{g_m}{G} \propto \frac{\sqrt{\frac{W}{L}I_{supply}}}{G} \tag{2.3}$$

$$\omega_u \approx |A_0| p_1 \approx \frac{g_m}{C_L} \propto \frac{\sqrt{\frac{W}{L}I_{supply}}}{C_L} \tag{2.4}$$

$$p_1 = \frac{g_{ds}+G}{C_L} \approx \frac{G}{C_L} \tag{2.5}$$

This results in that the DC gain and the unity-gain frequency increases while the first pole is constant when the supply current, I_{supply} increases.

c) The resistor and the transistor generate thermal noise. Compute the input referred noise power within the unity-gain frequency band, i.e., $\omega_u = g_{m1}/C_L$, of the circuit shown in Figure 2.1 caused by the thermal noise. Neglect the channel-length modulation.

The noise spectral density at the output is computed by the formula

$$S_{out}(\omega) = \sum_i |H_i|^2 S_i \tag{2.6}$$

where H_i is the frequency response from the i:th noise source to the output and S_i is the spectral density of the i:th noise source.

Further, the noise spectral density at the input is

$$S_{in}(\omega) = \frac{S_{out}(\omega)}{|H(\omega)|^2} \tag{2.7}$$

where $H(\omega)$ is the frequency response from the input to the output of the circuit. The noise power within the unity-gain frequency is computed by integrating the noise spectral density between zero and the unity-gain

frequency.

The thermal noise generated by a resistor can be modeled as a current noise source in parallel with the resistor. The noise sources spectral density is given by

$$S_R(\omega) = \frac{4kT}{R} \tag{2.8}$$

while for a transistor the noise source can be modeled as a a voltage noise source at the gate of the transistor with the following value

$$S_M(\omega) = \frac{8kT}{3}\frac{1}{g_m} \tag{2.9}$$

The input referred spectral density is given by

$$S_{in}(\omega) = \frac{|H_M|^2 S_M(\omega) + |H_R|^2 S_R(\omega)}{|H_M(\omega)|} = S_M(\omega) + \left|\frac{H_R(\omega)}{H_M(\omega)}\right|^2 S_R(\omega)$$

where

$$H_M(\omega) = -\frac{g_{m1}}{G + g_{ds} + j\omega C_L} \tag{2.10}$$

and

$$H_R(\omega) = \left.\frac{V_{out}}{i_R}\right|_{V_{in}=0} = \frac{1}{G + g_{ds} + j\omega C_L} \tag{2.11}$$

Hence, the input referred noise spectral density is given by

$$S_{in}(\omega) = \frac{8kT}{3}\frac{1}{g_m} + \frac{1}{g_{m1}^2}4kTG = \frac{4kT}{g_m}\left(\frac{2}{3} + \frac{G}{g_m}\right) \tag{2.12}$$

The noise power within the unity-gain frequency is

$$P_{in} = \frac{1}{2\pi}\int_0^{\omega_u} S_{in}(\omega)d\omega = \frac{4kT}{2\pi g_m}\left(\frac{2}{3} + \frac{G}{g_m}\right)\omega_u \approx \frac{4kT}{2\pi C_L}\left(\frac{2}{3} + \frac{1}{|A_0|}\right) \tag{2.13}$$

d) How should the amplifier be designed to have a small input referred noise power within the unity-gain frequency?

In order to have a small input referred noise power within the unity-gain bandwidth the second term in Eq. (2.13) must be small, i.e., increase the DC gain of the amplifier. This can be performed in two ways, either increase the transconductance of the transistor by increasing the supply current or increasing the width of the transistor, or increase the resistance of the resistor.

3. Operational amplifiers

The trend is to decrease the minimum feature sizes in CMOS process. This causes the low-frequency gain of a single transistor to decrease. If high DC gain is required in a modern process, a multi-stage amplifier may be an

appropriate choice. In this exercise, the small-signal equivalent of the differential response of a three-stage amplifier shown in Figure 3.1a is considered. The common-mode gain is zero. Throughout this exercise, assume that $C_L \gg C_1 = C_2 = C$, $R_1 = R_2 = R_L = R$.

a) Derive the transfer function from the input to the output of the circuit shown in Figure 3.1a, i.e., $H(s) = V_{out}(s)/V_{in,\,diff}(s)$.

Since there are not direct connections (compensations) between the individual gain stages in this circuit the transfer function can be divided into a product of partial transfer functions, i.e.,

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_2}\frac{V_2}{V_1}\frac{V_1}{V_{in}} = \frac{g_{m3}R_L}{1+sR_LC_L}\cdot\frac{g_{m2}R_2}{1+sR_2C_2}\cdot\frac{g_{m1}R_1}{1+sR_1C_1} \tag{3.1}$$

b) Compute an approximative expression for the unity-gain frequency given that the higher-order poles are located at much higher frequency than the unity-gain frequency. Motivate your solution.

Due to the simplification mentioned above, the transfer function can be reformulated to

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)^2} \tag{3.2}$$

where $p_1 = 1/(R_LC_L)$, $p_2 = 1/(RC)$, and $A_0 = A_1A_2A_3$.
The unity-gain frequency of the amplifier is computed as $|H(j\omega_u)| \equiv 1$

$$\frac{A_0^2}{\left(1+\frac{\omega_u^2}{p_1^2}\right)\left(1+\frac{\omega_u^2}{p_2^2}\right)^2} = 1 \qquad \Rightarrow \qquad A_0^2 = \left(1+\frac{\omega_u^2}{p_1^2}\right)\left(1+\frac{\omega_u^2}{p_2^2}\right)^2$$

This equation may be hard to solve exactly. However, an approximate solution is obtained by assuming that $|p_2| \gg \omega_u$. This assumption causes the term

$$\left(1+\frac{\omega_u^2}{p_2^2}\right)^2 \approx 1 \tag{3.3}$$

Hence, the approximated equation is now

$$A_0^2 \approx 1+\frac{\omega_u^2}{p_1^2} \tag{3.4}$$

which results in the following approximate expression for the unity-gain frequency

$$\omega_u \approx p_1\sqrt{A_0^2-1} \approx |A_0|p_1 \tag{3.5}$$

This expression holds if higher-order poles do not contribute so much to the decrease in the magnitude response and that the DC gain is much larger than unity (which is the case here).

c) The amplifier is connected in a close-loop configuration as shown in Figure 3.1b. For such a circuit, the transfer function can be given in the form

$$H(s) = \frac{A(s)}{1 + \beta A(s)} \tag{3.6}$$

where β is the feedback factor and $A(s)$ is the gain of the amplifier. Determine the feedback factor for the circuit shown in Figure 3.1b..

This exercise is solved by computing the transfer function from the input of the amplifier in the feedback configuration to its output. In this case the characteristics of the amplifier is

$$(V_{in,\,\mathrm{amp}+} - V_{in,\,\mathrm{amp}-})A = V_{out,\,\mathrm{opamp}}$$

Inserting this into the buffer connected circuit the result is

$$(V_{in} - V_{out})A = V_{out} \qquad \Rightarrow \qquad \frac{V_{out}}{V_{in}} = \frac{A}{1 + A}$$

Hence, the feedback factor β is unity.

d) For the circuit in Figure 3.1b compute an analytic expression for the factor K, which relates the second pole p_2 and the unity-gain frequency ω_u, in the expression $p_2 = K \cdot \omega_u$ in order to obtain a specific phase margin, i.e., compute $K = f(\phi_m)$. Assume that at the unity-gain frequency the first pole has caused a –90 degree phase shift.

The phase margin of the circuit for $\beta = 1$ is computed as follows

$$\phi_m = -\mathrm{atan}\frac{\omega_u}{p_1} - 2\,\mathrm{atan}\frac{\omega_u}{p_2} + 180 = -\mathrm{atan}\frac{\omega_u}{p_1} - 2\,\mathrm{atan}\frac{1}{K} + 180$$

From the exercise the first term in the equation for the phase margin is –90 degrees. Hence, the phase margin is

$$\phi_m = 90 - 2\,\mathrm{atan}\frac{1}{K} \tag{3.7}$$

Solving for the K factor results in

$$K = \frac{1}{\tan\left(\dfrac{90 - \phi_m}{2}\right)} \tag{3.8}$$

e) Compute the value of the K factor to obtain a phase margin of 45 and 75 degrees, respectively.

Using Eq. (3.8) for the phase margins of 45 and 75 degrees respectively results in that the higher-order poles must be located at 2.4 and 7.6 times the unity-gain frequency.

f) Is the approximation in 3b good for the two cases in exercise 3e? Motivate your answer carefully.

Here it is not so easy to give a yes or no answer since this will depend on the application. However, in the computation of the approximate expression for the unity-gain frequency we obtained the following expression

$$A_0^2 = \left(1 + \frac{\omega_u^2}{p_1^2}\right)\left(1 + \frac{\omega_u^2}{p_2^2}\right)^2 \tag{3.9}$$

which should be solved with respect to the unity-gain frequency. In the approximate expression the second term was set to zero since $|p_2| \gg \omega_u$. For a phase margin of 45 degrees $|p_2| \approx 2.4\omega_u$ which results in value of the second term in Eq. (3.9) to be equal to about 1.37. Hence, the unity-gain frequency is a little bit smaller than for the estimation.

For the case of 75 degree phase margin the second term is about 1.035 which typically is small enough for many of the hand computation tasks.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau, t + 4\tau$, etc. is shown in Figure 4.1. Assume that the input signal are constant between clock phase 1 and 2, i.e., $V_1(t) = V_1(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_1(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal.

Starting by assigning positive charge at the left plate of capacitor C_1 and C_2 and to the right of C_3 and C_4.

The next step is to express the charge at the capacitors.

At time t

$q_1(t) = C_1V_1(t)$, $q_2(t) = 0$, $q_3(t) = C_3V_{out}(t)$, $q_4(t) = C_4V_{out}(t)$

time $t + \tau$

$q_1(t + \tau) = C_1V_1(t + \tau)$, $q_2(t + \tau) = C_2V_1(t + \tau)$, $q_3(t + \tau) = C_3V_{out}(t + \tau)$, $q_4(t + \tau) = 0$

and at time $t + 2\tau$

$q_1(t + 2\tau) = C_1V_1(t + 2\tau)$, $q_2(t + 2\tau) = 0$, $q_3(t + 2\tau) = C_3V_{out}(t + 2\tau)$, $q_4(t + 2\tau) = C_4V_{out}(t + 2\tau)$

The charge conservation equations are

$$q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) + q_4(t + \tau) = q_1(t + 2\tau) + q_2(t + 2\tau) + q_3(t + 2\tau) + q_4(t + 2\tau) \tag{4.1}$$

$$q_1(t) + q_3(t) = q_1(t + \tau) + q_3(t + \tau) \tag{4.2}$$

The Eq. (4.2) results in

$$C_1V_1(t) + C_3V_{out}(t) = C_1V_1(t + \tau) + C_3V_{out}(t + \tau) \tag{4.3}$$

Further, by applying the fact that $V_1(t) = V_1(t + \tau)$ results in

$$V_{out}(t) = V_{out}(t + \tau) \tag{4.4}$$

which states that the output voltage at clock phase 2 is equal to the output voltage at the previous clock phase.

Furthermore, Eq. (4.1) results in

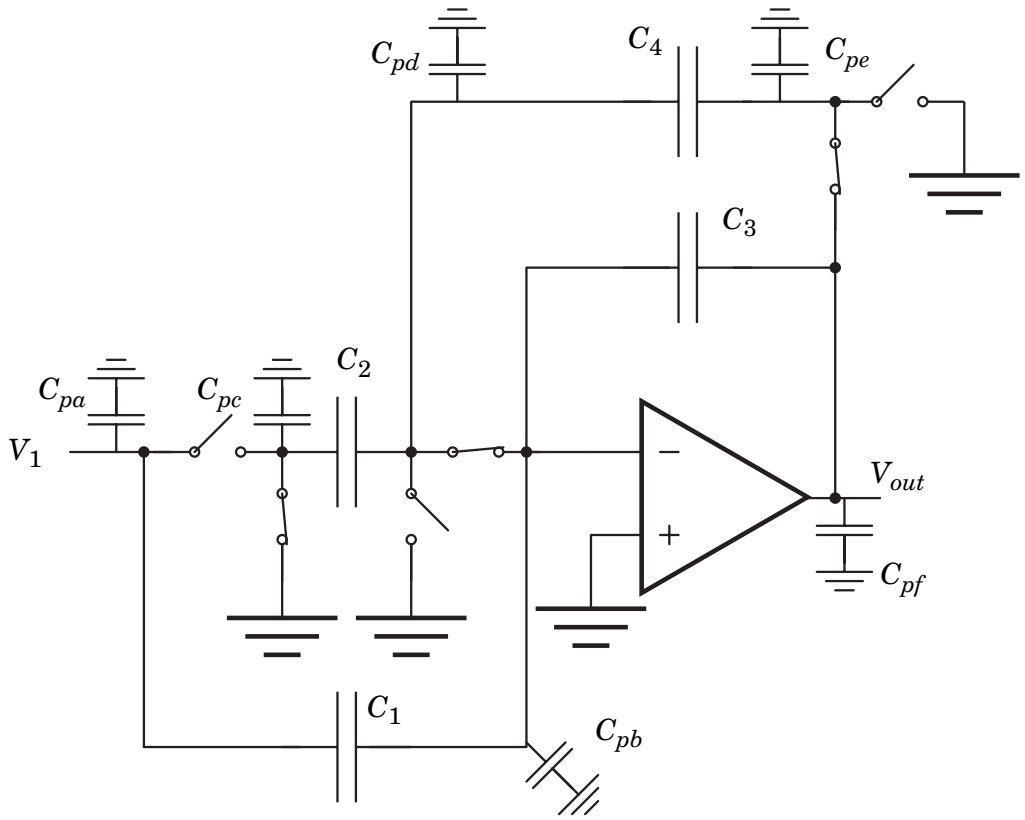

Figure 4.1 The SC circuit with capacitive parasitics due to the capacitor and the switches.

$$C_1V_1(t+\tau) + C_2V_1(t+\tau) + C_3V_{out}(t+\tau) = \\ = C_1V_1(t+2\tau) + C_3V_{out}(t+2\tau) + C_4V_{out}(t+2\tau) \qquad (4.5)$$

This can be simplified to

$$(C_1 + C_2)V_1(t) + C_3V_{out}(t) = C_1V_1(t+2\tau) + (C_3 + C_4)V_{out}(t+2\tau) \qquad (4.6)$$

Performing a Z-transformation on this equation gives the results

$$V_{out}(z)[(C_3 + C_4)z - C_3] = V_{in}(z)[C_1 + C_2 - C_1z] \qquad (4.7)$$

Hence, the transfer function is

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1 + C_2 - C_1z}{(C_3 + C_4)z - C_3} = -\frac{C_1}{C_3}\frac{\left(1 + \frac{C_2}{C_1}\right) - z}{1 - z\left(1 + \frac{C_4}{C_3}\right)} \qquad (4.8)$$

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The parasitics of interest are shown in Figure 4.1.

C_{pa} do not alter the transfer function since they are always connected to the

ideal input source.

C_{pb},C_{pd} are connected between ground and virtual ground and thereby does not change the transfer function.

C_{pc} Charged at clock phase 2 by an ideal voltage source and discharged at clock phase 1 to ground. No changes in the transfer function.

C_{pe} Connected between ground and the output node of the OP amp which can generate and sink as much charge as required. No effect on the transfer function.

Hence, the circuit is insensitive to capacitive parasitics, when the transfer function is of concern.

c) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA suffers from an offset voltage, V_{os}.

The next step is to express the charge at the capacitors.

At time t

$q_1(t) = C_1(V_1(t) - V_{os})$, $q_2(t) = C_2(0 - V_{os})$, $q_3(t) = C_3(V_{out}(t) - V_{os})$, $q_4(t) = C_4(V_{out}(t) - V_{os})$

time $t + \tau$

$q_1(t+\tau) = C_1(V_1(t+\tau) - V_{os})$, $q_2(t+\tau) = C_2V_1(t+\tau)$, $q_3(t+\tau) = C_3(V_{out}(t+\tau) - V_{os})$, $q_4(t+\tau) = 0$

and at time $t + 2\tau$

$q_1(t+2\tau) = C_1(V_1(t+2\tau) - V_{os})$, $q_2(t+2\tau) = C_2(0 - V_{os})$, $q_3(t+2\tau) = C_3(V_{out}(t+2\tau) - V_{os})$, $q_4(t+2\tau) = C_4(V_{out}(t+2\tau) - V_{os})$

The charge conservation equations are

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) + q_4(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) + q_4(t+2\tau) \quad (4.9)$$

$$q_1(t) + q_3(t) = q_1(t+\tau) + q_3(t+\tau) \quad (4.10)$$

The Eq. (4.2) results in

$$C_1V_1(t) + C_3V_{out}(t) = C_1V_1(t+\tau) + C_3V_{out}(t+\tau) \quad (4.11)$$

Further, by applying the fact that $V_1(t) = V_1(t+\tau)$ results in

$$V_{out}(t) = V_{out}(t+\tau) \quad (4.12)$$

which states that the output voltage at clock phase 2 is equal to the output voltage at the previous clock phase.

Furthermore, Eq. (4.1) results in

$$C_1V_1(t+\tau) + C_2V_1(t+\tau) + C_3V_{out}(t+\tau) = C_1V_1(t+2\tau) - C_2V_{os} + C_3V_{out}(t+2\tau) + C_4(V_{out}(t+2\tau) - V_{os}) \quad (4.13)$$

This can be simplified to

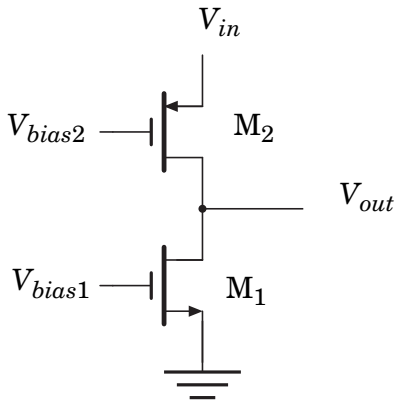

Figure 5.1 A CMOS inverter used as a analog amplifier

$$(C_1 + C_2)V_1(t) + C_3V_{out}(t) + (C_2 + C_4)V_{os} = C_1V_1(t + 2\tau) + (C_3 + C_4)V_{out}(t + 2\tau) \tag{4.14}$$

Performing a Z-transformation on this equation gives the results

$$V_{out}(z)[(C_3 + C_4)z - C_3] = V_{in}(z)[C_1 + C_2 - C_1z] + (C_2 + C_4)V_{os} \tag{4.15}$$

Hence, the output signal is

$$V_{out}(z) = -\frac{C_1}{C_3}\frac{\left(1 + \frac{C_2}{C_1}\right) - z}{1 - z\left(1 + \frac{C_4}{C_3}\right)}V_{in}(z) - \frac{(C_2 + C_4)V_{os}}{C_3\left(1 - z\left(1 + \frac{C_4}{C_3}\right)\right)} \tag{4.16}$$

5. A mixture of questions

a) Draw the small-signal model and compute the DC gain, input and output resistance for this circuit shown in Figure 5.1.

The DC gain can be computed by applying nodal analysis in the output node

$$g_{m2}V_{in} + g_{mbs2}V_{in} + g_{ds2}(V_{in} - V_{out}) - V_{out}(g_{ds1} + sC_L) = 0 \tag{5.1}$$

This results in the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2} + g_{mbs2} + g_{ds2}}{g_{ds1} + g_{ds2} + sC_L} \tag{5.2}$$

The output resistance is computed by adding a voltage source at the output and computing its current when the input voltage is zero.

$$I_{out} = V_{out}(g_{ds1} + g_{ds2}) \tag{5.3}$$

Hence, the output resistance is

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} \tag{5.4}$$

The input resistance is

$$I_{in} = V_{out}g_{ds1} = V_{in}(g_{m2} + g_{mbs2}) + (V_{in} - V_{out})g_{ds2} \tag{5.5}$$

The first equality gives $V_{out} = I_{in}R_{ds1}$ and inserting it into the second equality gives

$$I_{in} = V_{in}(g_{m2} + g_{mbs2} + g_{ds2}) - I_{in}\frac{g_{ds2}}{g_{ds1}} \tag{5.6}$$

Hence, the input resistance is

$$\frac{V_{in}}{I_{in}} = \frac{1 + \frac{g_{ds2}}{g_{ds1}}}{g_{m2} + g_{mbs2} + g_{ds2}} \tag{5.7}$$

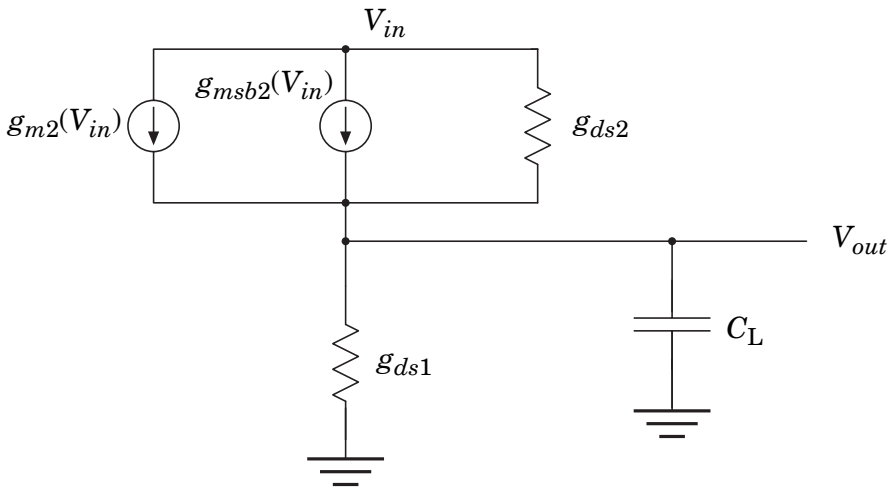

Figure 5.2 A small-signal model for a common-gate amplifier.

b) State advantages and disadvantages of using switched capacitor filters compared with active-RC filters.

The benefits of using a switched capacitor filter over an active-RC filter is that the time constants do not need to be tuned since they are given by a ratio between two or several capacitors compared to a resistance times a capacitance. The drawback is that a clock is required which typically is unwanted on analog integrated circuits due to noise from this clock.

c) State benefits and drawbacks of using a fully differential compare with a single-ended circuit structure in an integrated analog circuit.

Benefits of using fully differential circuits are decreased noise at the outputs, increased CMRR and PSRR. Suppression of even-order distortion terms. The drawbacks are increased power consumption and the need for a common-mode output stabilization circuit.

d) Why is it uncommon to use the minimum channel length and channel widths for a transistor in an analog design.

The minimum channel length is not commonly used since the β matching is poor for this choice of channel length. Instead, larger channel lengths are commonly used.