

**Correct (?) solutions to
Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits**

Date	January 12, 2004
Time:	8 - 12
Place:	Garn
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit shown in the Figure is to be analyzed using large-signal analysis. Throughout this exercise assume that the power supply voltage is much larger than the threshold voltages, i.e., $V_{DD} \gg V_{T1} + V_{T2}$. Further, neglect the channel-length modulation.

a) Assume that the transistors M_1 and M_2 are saturated. Express V_{out} as a function of V_{in} .

The exercise can be solved by setting up the currents in the nodes V_x and V_{out} . The current through transistor M_1 is

$$I_{D1} = \alpha_1(V_{in} - V_{T1})^2 \quad (1.1)$$

and it should equal the current through resistor R_1 , which delivers the current

$$I_{D1} = I_{R1} = (V_{DD} - V_x)G_1 \quad (1.2)$$

Solving for the node voltage V_x results in

$$V_x = V_{DD} - \frac{\alpha_1(V_{in} - V_{T1})^2}{G_1} \quad (1.3)$$

In the output node the following equation must be satisfied

$$I_{D2} = V_{out}G_2 = \alpha_2(V_{DD} - V_x - V_{T2})^2 \quad (1.4)$$

which results in

$$V_{out} = \frac{\alpha_2(V_{DD} - V_x - V_{T2})^2}{G_2} \quad (1.5)$$

The output voltage as a function of the input voltage is computed by inserting (1.3) into (1.5), resulting in

$$\begin{aligned}
V_{out} &= \frac{\alpha_2 \left(V_{DD} - \left(V_{DD} - \frac{\alpha_1 (V_{in} - V_{T1})^2}{G_1} \right) - V_{T2} \right)^2}{G_2} \\
&= \frac{\alpha_2}{G_2} \left(\frac{\alpha_1}{G_1} (V_{in} - V_{T1})^2 - V_{T2} \right)^2 \quad (1.6)
\end{aligned}$$

An input sinusoidal waveform will cause distortion terms at two, three, and four times the input frequency.

- b) Determine the possible range of the voltage V_x in order to ensure that the transistors M_1 and M_2 are saturated. The DC voltages at the input and output should be set to $V_{in,DC} = V_{out,DC} = V_{DD}/2$.

The range is derived by setting up the constraints in which both transistors are operating in the saturation region. Starting with transistor M_2 the following equation must be met

$$V_{SD2} > V_{SG2} - V_{T2} > 0 \quad (1.7)$$

i.e.,

$$V_{DD} - V_{out} > V_{DD} - V_x - V_{T2} > 0 \quad (1.8)$$

The inequality to the left yields

$$V_x > V_{out} - V_{T2} = \frac{V_{DD}}{2} - V_{T2} \quad (1.9)$$

and the inequality to the right is reformulated according to

$$V_{DD} - V_{T2} > V_x \quad (1.10)$$

For transistor M_1 the following inequalities must be met

$$V_x > V_{in} - V_{T1} > 0 \quad (1.11)$$

The inequality to the left constraints the node voltage V_x . In total

$$\max \left\{ \frac{V_{DD}}{2} - V_{T1}, \frac{V_{DD}}{2} - V_{T2} \right\} < V_x < V_{DD} - V_{T2} \quad (1.12)$$

- c) For matching purposes, the resistance values are chosen equal, i.e., $R_1 = R_2 = R$. Further, $V_{in,DC} = V_{out,DC} = V_{DD}/2$. Select a suitable value of the voltage V_x and determine the width over length ratio as a function of the resistance, R , the power consumption, power supply voltage, and transistor parameters.

The power consumption of the circuit is given by $P = V_{DD}(I_{D1} + I_{D2})$ where $I_{D1} = (V_{DD} - V_x)G$ and $I_{D2} = V_{out}G = 0.5V_{DD}G$. Further, the current through the transistors is expressed as

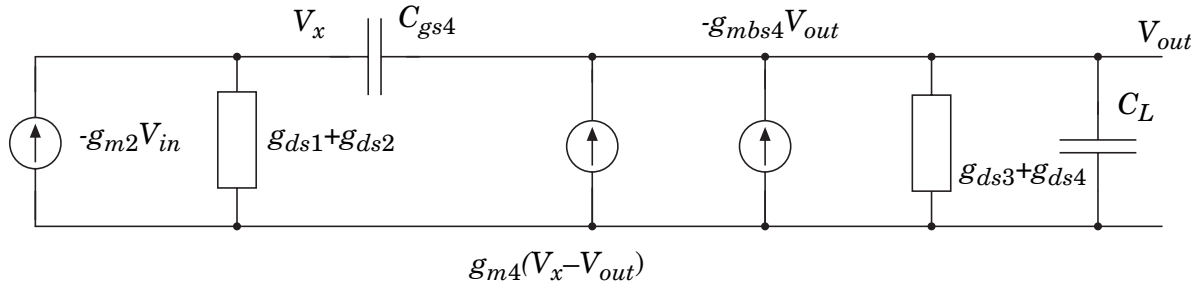


Figure 2.1 Small-signal model of the two amplifier stages.

$$I_{D1} = K_n \frac{W_1}{L_1} (V_{in} - V_{T1})^2 \quad (1.13)$$

Solving for the width-length ratio yields

$$\frac{W_1}{L_1} = \frac{I_{D1}}{K_n \left(\frac{V_{DD}}{2} - V_{T1} \right)^2} = \frac{\frac{P}{V_{DD}} - \frac{V_{DD}}{2} G}{K_n \left(\frac{V_{DD}}{2} - V_{T1} \right)^2} \quad (1.14)$$

In the same manner

$$\frac{W_2}{L_2} = \frac{I_{D2}}{K_p \left(\frac{V_{DD}}{2} - V_{T2} \right)^2} = \frac{\frac{P}{V_{DD}} - (V_{DD} - V_x) G}{K_p \left(\frac{V_{DD}}{2} - V_{T2} \right)^2} \quad (1.15)$$

A suitable value of the V_x node voltage is for example $V_{DD}/2$ since both transistors will then be saturated. This yields a power consumption of $P = V_{DD}^2 G$ and the width-length ratios will be

$$\frac{W_1}{L_1} = \frac{P}{2V_{DD} K_n \left(\frac{V_{DD}}{2} - V_{T1} \right)^2} \quad (1.16)$$

and

$$\frac{W_2}{L_2} = \frac{P}{2V_{DD} K_p \left(\frac{V_{DD}}{2} - V_{T2} \right)^2} \quad (1.17)$$

2. Small-signal analysis

The circuit shown in the Figure is to be used in an amplifier circuit. Assume that the transistors are saturated. Do not neglect the bulk effect.

- a) Compute the transfer function from the input to the output of the circuit. Determine approximative expressions for the DC gain and possible poles and zeros. Assume that $C_L g_{ds} \gg C_{gs4} g_m$.

The small-signal model of the amplifier is shown in Figure 2.1. The transfer

function can be derived by using for example nodal analysis in the nodes V_x and V_{out} .

$$-g_{m2}V_{in} - (g_{ds1} + g_{ds2})V_x - sC_{gs4}(V_x - V_{out}) = 0$$

$$g_{m4}(V_x - V_{out}) - g_{mbs4}V_{out} - (g_{ds3} + g_{ds4} + sC_L)V_{out} - (V_{out} - V_x)sC_{gs4} = 0$$

From the lowermost equation we can solve for V_x

$$V_x = \frac{g_{m4} + g_{mbs4} + g_{ds3} + g_{ds4} + s(C_{gs4} + C_L)}{g_{m4} + sC_{gs4}}V_{out} \quad (2.1)$$

Inserting this into the other equation results in

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m2}(g_{m4} + sC_{gs4})}{a + bs + cs^2} \quad (2.2)$$

where

$$a = (g_{ds1} + g_{ds2})(g_{m4} + g_{mbs4} + g_{ds3} + g_{ds4})$$

$$b = C_L(g_{ds1} + g_{ds2}) + C_{gs4}(g_{ds1} + g_{ds2} + g_{mbs4} + g_{ds4} + g_{ds3})$$

$$c = C_{gs4}C_L$$

The poles can approximately be expressed by using the following assumption that the poles are well separated, i.e., the approximation

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) \approx 1 + \frac{s}{p_1} + \frac{s^2}{p_1p_2} \quad (2.3)$$

is acceptable. The poles are well separated since $C_Lg_{ds} \gg C_{gs4}g_m$. The poles are then expressed as $p_1 \approx a/b$ and $p_2 \approx b/c$.

$$\begin{aligned} p_1 &\approx \frac{(g_{ds1} + g_{ds2})(g_{m4} + g_{mbs4} + g_{ds3} + g_{ds4})}{C_L(g_{ds1} + g_{ds2}) + C_{gs4}(g_{ds1} + g_{ds2} + g_{mbs4} + g_{ds4} + g_{ds3})} \\ &\approx \frac{g_{m4} + g_{mbs4}}{C_L + \frac{C_{gs4}g_{mbs4}}{g_{ds1} + g_{ds2}}} \approx \frac{g_{m4} + g_{mbs4}}{C_L} \end{aligned} \quad (2.4)$$

$$\begin{aligned} p_2 &\approx \frac{C_L(g_{ds1} + g_{ds2}) + C_{gs4}(g_{ds1} + g_{ds2} + g_{mbs4} + g_{ds4} + g_{ds3})}{C_L C_{gs4}} \\ &\approx \frac{g_{ds1} + g_{ds2}}{C_{gs4}} + \frac{g_{mbs4}}{C_L} \approx \frac{g_{ds1} + g_{ds2}}{C_{gs4}} \end{aligned} \quad (2.5)$$

The zero is located at

$$z = g_{m4}/C_{gs4} \quad (2.6)$$

The DC gain of the circuit is given by

$$A_0 = -\frac{g_{m2}g_{m4}}{(g_{ds1} + g_{ds2})(g_{m4} + g_{mbs4} + g_{ds3} + g_{ds4})} \approx \left(-\frac{g_{m2}}{g_{ds1} + g_{ds2}}\right) \frac{g_{m4}}{g_{m4} + g_{mbs4}}$$

The unity-gain frequency is located at

$$\omega_u \approx |A_0|p_1 \approx \frac{g_{m2}}{g_{ds1} + g_{ds2}} \frac{g_{m4}}{C_L} \quad (2.7)$$

b) State two ways to increase the phase margin of this circuit.

Table 1: How to increase the phase margin of the circuit.

Action	ω_u	p_1	p_2	z	ϕ_m
g_{m2} decreased	decreased	-	-	-	increased
g_{m4} decreased	decreased	decreased	-	decreased	increased
C_L increased	decreased	decreased	-	-	increased

c) Compute the output resistance of the circuit.

The small-signal model for low frequencies and for a zeroed input voltage source is shown in Figure 2.2.

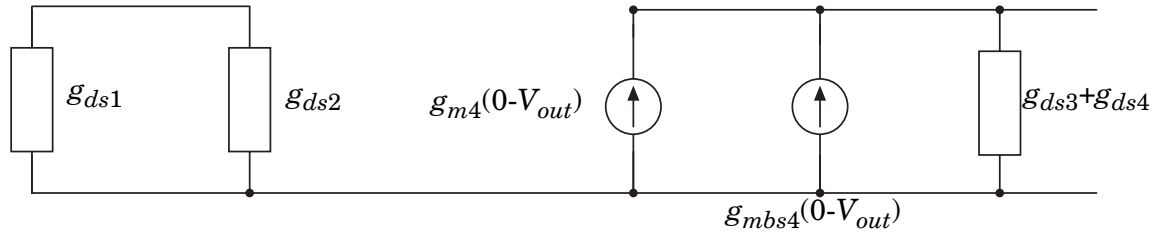


Figure 2.2 A small-signal model of the circuit for computing the output resistance.

The output resistance is computed by adding a voltage source at the output and computing the current that it delivers. Performing nodal analysis in the output node results in

$$-g_{m4}V_{out} - g_{mbs4}V_{out} - (g_{ds3} + g_{ds4})V_{out} = -I_{out} \quad (2.8)$$

and the output resistance is

$$\frac{V_{out}}{I_{out}} = \frac{1}{g_{m4} + g_{mbs4} + g_{ds3} + g_{ds4}} \quad (2.9)$$

3. Analysis of operational amplifiers

The transfer function

$$H(s) = -\left(\frac{a_0 + a_1s + a_2s^2}{b_0 + b_1s + s^2}\right) \quad (3.1)$$

is to be realized in an integrated circuit. A signal-flow graph of a possible implementation is shown in the Figure. The coefficients a_i are positive.

- a) Express a_i and b_i as a function of α_j and β_j . Are there any restrictions of the α and β coefficients in order to have a stable filter?

The output voltage is computed by following the paths in the signal-flow graph.

$$V_{out} = V_{in} \left[\frac{\beta_2}{s^2} + \frac{\beta_1}{s} + \beta_0 \right] + V_{out} \left[\frac{\alpha_2}{s^2} + \frac{\alpha_1}{s} \right] \quad (3.2)$$

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{\beta_0s^2 + \beta_1s + \beta_2}{s^2 - \alpha_1s - \alpha_2} \quad (3.3)$$

Both α_1 and α_2 must be negative in order to realize a circuit which is stable. To realize the transfer function in Eq. (3.1) all β_j must also be negative. The mapping between the a and b to α and β is

$$a_0 = -\beta_2, a_1 = -\beta_1, a_2 = -\beta_0, b_0 = -\alpha_2, \text{ and } b_1 = -\alpha_1.$$

- b) Realize a stable transfer function using the signal-flow graph in the Figure. The implementation should contain only resistors, capacitors, and operational amplifiers. Further, identify the coefficients a_i and b_i in terms of resistance and capacitance values.

There are several possible implementations. The one chosen here is found by propagating -1 so that the integrator to the left is a noninverting integrator while the second one is an inverting integrator. The rightmost summation is actually a difference between the output signal of the integrator and the a_2V_{in} term. The active-RC implementation is shown in Figure 3.1

The constants in the transfer function can should be matched to the ones in the active-RC implementation. Following the same paths in both the signal-flow graphs and the implementation yields

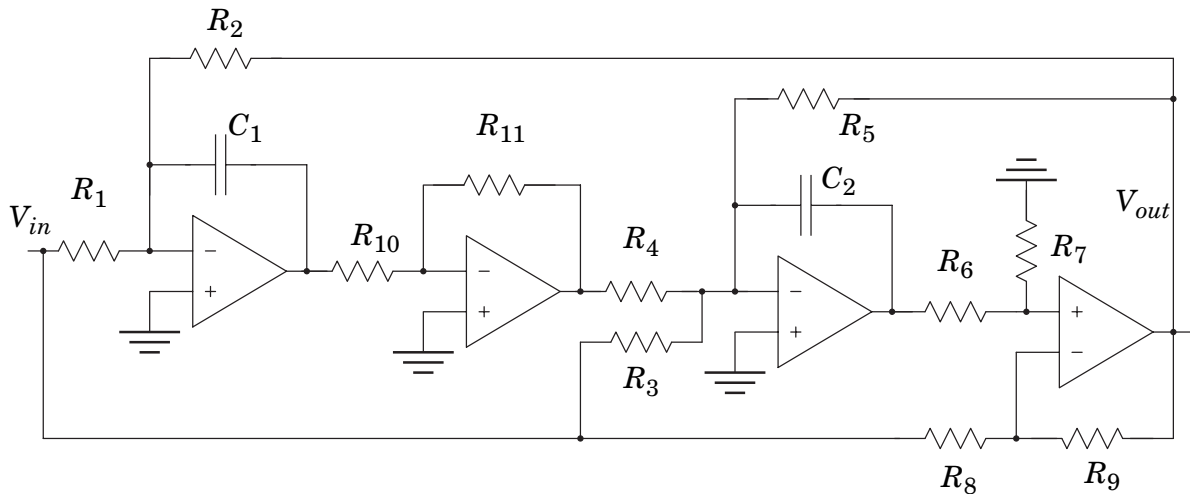


Figure 3.1 An active-RC implementation of the signal-flow graph.

Table 2: Coefficient and RC values

Coefficient	Value
b_0	$\frac{1}{R_2} \frac{R_{11}}{C_1 R_{10}}$
a_0	$\frac{1}{R_1} \frac{R_{11}}{C_1 R_{10}}$
b_1	$\frac{1}{R_5 C_2}$
a_1	$\frac{1}{R_3 C_2}$
1	$R_4 C_2$
a_2	$\frac{R_9}{R_8} = \frac{R_6}{R_7}$

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in the Figure.

- a) Determine the output voltage as a function of the input voltage, $V_{out}(z) = f(V_{in}(z))$ for clock phase 1 of the circuit shown in the Figure. Assume that the operational amplifier is ideal except that it suffers from an offset voltage.

This exercise is solved using charge redistribution analysis. The reference directions are shown in Figure 4.1.

First we express the charges over all capacitors at times instances t , $t + \tau$, and $t + 2\tau$.

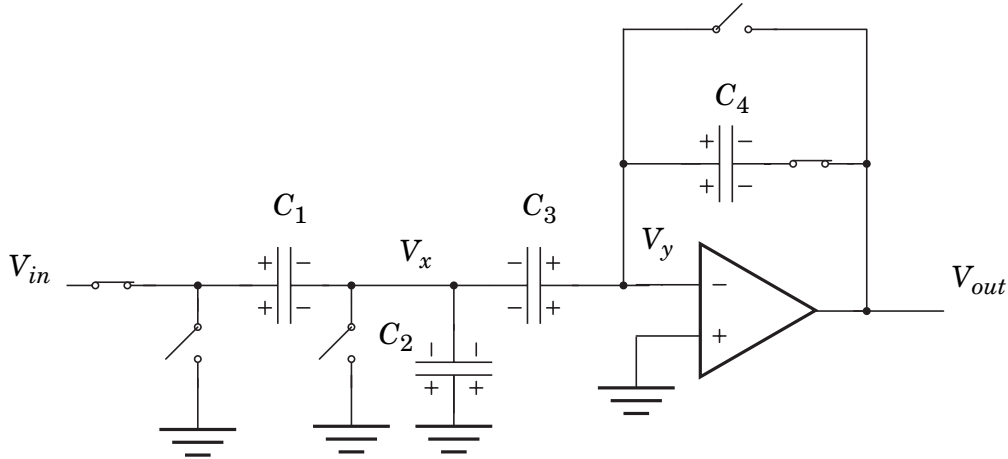


Figure 4.1 The switched-capacitor circuit with reference directions.

$$q_1(t) = C_1(V_{in}(t) - V_x(t)),$$

$$q_2(t) = C_2(-V_x(t)),$$

$$q_3(t) = C_3(V_{os} - V_x(t)),$$

$$q_4(t) = C_4(V_{os} - V_{out}(t)).$$

At time $t + \tau$

$$q_1(t + \tau) = C_1(0 - 0),$$

$$q_2(t + \tau) = C_2(0 - 0),$$

$$q_3(t + \tau) = C_3(V_{os} - 0),$$

$$q_4(t + \tau) = q_4(t).$$

At time $t + 2\tau$

$$q_1(t + 2\tau) = C_1(V_{in}(t + 2\tau) - V_x(t + 2\tau)),$$

$$q_2(t + 2\tau) = C_2(-V_x(t + 2\tau)),$$

$$q_3(t + 2\tau) = C_3(V_{os} - V_x(t + 2\tau)),$$

$$q_4(t + 2\tau) = C_4(V_{os} - V_{out}(t + 2\tau)).$$

Charge conservation yields

$$-q_1(t + 2\tau) - q_2(t + 2\tau) - q_3(t + 2\tau) = -q_1(t + \tau) - q_2(t + \tau) - q_3(t + \tau) \quad (4.1)$$

and

$$-q_3(t + 2\tau) - q_4(t + 2\tau) = -q_3(t + \tau) - q_4(t + \tau) \quad (4.2)$$

The transfer function is found using the above equations. V_x is solved from Eq. (4.1)

$$C_1(V_{in}(t + 2\tau) - V_x(t + 2\tau)) + C_2(-V_x(t + 2\tau)) + C_3(V_{os} - V_x(t + 2\tau)) = C_3V_{os}$$

which yields

$$V_x(t + 2\tau) = \frac{C_1}{C_1 + C_2 + C_3} V_{in}(t + 2\tau) \quad (4.3)$$

Eq. (4.2) yields

$$C_3V_{os} + C_4(V_{os} - V_{out}(t)) = C_3(V_{os} - V_x(t + 2\tau)) + C_4(V_{os} - V_{out}(t + 2\tau))$$

and

$$C_4(V_{out}(t + 2\tau) - V_{out}(t)) = -C_3\left(\frac{C_1}{C_1 + C_2 + C_3} V_{in}(t + 2\tau)\right)$$

Performing Z-transformation yields

$$C_4(z - 1)V_{out}(z) = -\left(\frac{C_1 C_3 z}{C_1 + C_2 + C_3}\right)V_{in}(z).$$

This results in the following transfer function

$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1 C_3}{C_4(C_1 + C_2 + C_3)} \frac{z}{z - 1} \quad (4.4)$$

which is an accumulator.

b) Is the circuit insensitive of capacitive parasitics. Motivate for all parasitic capacitors in the circuit.

The circuit with all parasitic capacitors are shown in Figure 4.2.

C_{pa} does not change the transfer function since it is driven by an ideal voltage source as an input.

C_{pb} is charged from an ideal voltage source and then discharged to ground and thereby not changing the transfer function.

C_{pc} , C_{pd} , and C_{pf} is short-circuited to ground and do not alter the transfer function.

C_{pe} is charged during clock cycle 1 and discharged in clock cycle 2 and thereby it will be take part in the charge conservation step and the transfer function of the circuit is changed.

C_{pg} is connected between ground and virtual ground and thereby not changing the transfer function.

C_{ph} is charged from the ideal output of the amplifier in clock phase 1 and will keep its charge in clock phase 2. Hence, the transfer function is not changed for this parasitic.

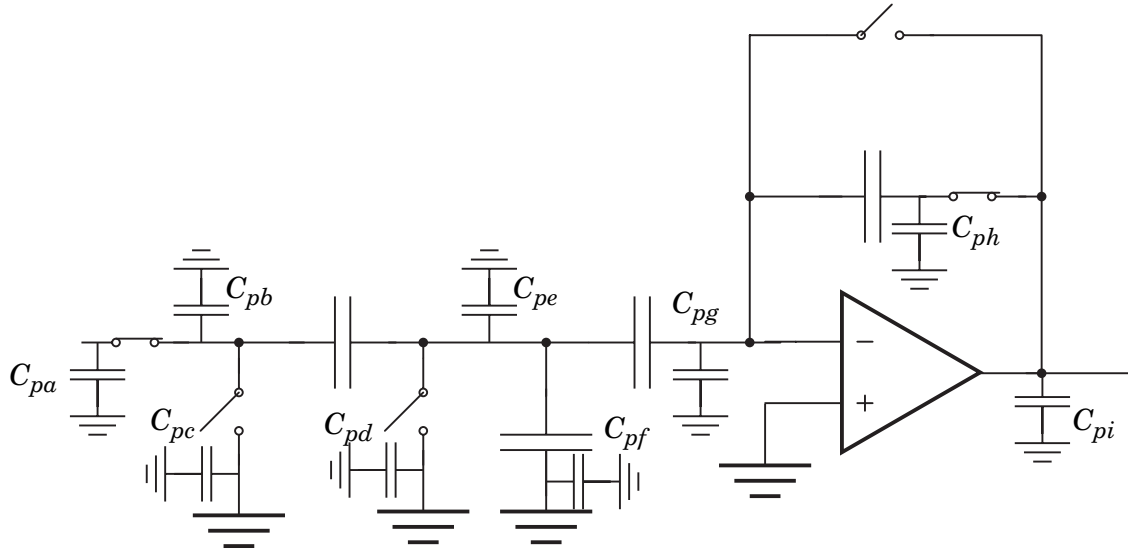


Figure 4.2 The SC circuit with parasitics capacitors.

C_{pi} is charged and discharged by an ideal amplifier and thereby does not alter the transfer function.

Hence, the circuit is sensitive to capacitive parasitics and it is not recommended to be used in a SC filter.

5. A mixture of questions

- a) Compute the input-referred noise spectral density of the circuit shown in the Figure. Assume that the resistor and the saturated transistor generate thermal noise.

The thermal noise in a MOS transistor can be modelled as a voltage noise source in series with the gate of the transistor. For the resistor a good noise model is a noise current source in parallel with the resistor. Computing the input-referred noise spectral density can be obtained by computing the output-referred noise spectral density and dividing it by the squared magnitude response from the input to the output of the circuit. The output referred spectral density is computed according to

$$S_{out}(\omega) = \sum |H_i|^2 S_i(\omega) \tag{5.1}$$

The transfer function from the input to the output is given by

$$H_1 = \frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{ds} + G + sC_L} \tag{5.2}$$

while the transfer function from the resistor's noise source to the output is

$$H_2 = \frac{V_{out}}{I_{nR}} = \frac{1}{g_{ds} + G + sC_L} \tag{5.3}$$

Hence, the output noise spectral density is given by

$$S_{out}(\omega) = |H_1|^2 S_{transistor} + |H_2|^2 S_{resistor} \tag{5.4}$$

The input referred noise spectral density is then

$$\begin{aligned}
 S_{in}(\omega) &= S_{transistor} + \left| \frac{H_2}{H_1} \right|^2 S_{resistor} \\
 &= \frac{8kT}{3} \frac{1}{g_m} + \frac{1}{g_m^2} \frac{4kT}{R} = \frac{4kT}{g_m} \left(\frac{2}{3} + \frac{1}{g_m R} \right)
 \end{aligned} \tag{5.5}$$

- b) Which of the accumulator circuits in the Figure is preferred to be used in an integrated filter? Assume that the input voltage is sampled according to $V_{in}(t + \tau) = V_{in}(t + 2\tau)$. Motivate your answer carefully.

Both the circuits are SC accumulators, but the one to the right(b) is sensitive to capacitive parasitics. This means that the time-constant of the circuit is partly determined by the unpredictable parasitic component. Hence, the circuit is not recommended to be used in a real implementation.

- c) State two advantages of using oversampled digital-to-analog converters instead of Nyquist-rate converters.

First of all, using oversampling results in higher signal-to-noise ratio and thereby higher resolution.

Second, anti-sinc filter requirements are decreased, which eases the implementation of the analog filter.

- d) What are the benefits and drawbacks of using a fully-differential compared to a single-ended operational amplifier?

Examples of advantages are higher PSRR and CMRR and lower distortion (since even-order distortion terms are ideally cancelled.) and less noise.

A drawback is the required CMFB (Common-mode feedback) or CMFF (Common-mode feedforward) circuit which typically is hard to design.

Further, the possible swing at the output of the amplifier is decreased due to this circuit.