Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	January 11, 2002
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

a) Determine the operation regions of the transistors.

To be able to have a current much larger than zero, the transistor M_1 must be on. When this transistor is on it will start to operate in saturation region. Hence, the transistor M_1 is operating in the saturation region.
For the current I_{out} to be much larger than zero, non of the transistors, M_2 and M_3 can be operating in cut-off since no (or very small) current is flowing through the transistors. Hence, the transistors are either operating in the saturation region or in the linear region. For a transistor that is biased in the saturation region the following inequalities must be met

$$V_{DS} > V_{GS} - V_{TH} > 0\,. \tag{1.1}$$

In the case of transistor M_3 this means that

$$V_{out} - V_x > V_1 - V_x - V_{TH} > 0 \tag{1.2}$$

where the left inequality is simplified to $V_{out} > V_1 - V_{TH}$. Hence, since the circuit is designed to have $V_1 = V_{out}$ this inequality holds and the transistor operates in the saturation region. This is also due to the fact the transistor is on. The right inequality is expressed as

$$V_x < V_1 - V_{TH} \tag{1.3}$$

for the transistor to be on.

For the transistor M_2 Eq. (1.1) is simplified to

$$V_x > V_1 - V_{TH} \tag{1.4}$$

Comparing Eq. (1.3) and Eq. (1.4) yields a contradiction and since M_3 is on Eq. (1.3) must hold and then Eq. (1.4) is not correct. Hence, transistor M_2 must operate in the linear (triode) region.

b) Derive the voltage at node V_x.

The current through transistor M_3 is expressed as

$$I_3 = \alpha \cdot (V_{GS} - V_{TH})^2 = \alpha \cdot (V_1 - V_x - V_{TH})^2 \quad (1.5)$$

when the channel-length modulation is ignored. The current through transistor M_2 is

$$I_2 = 2\alpha\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] =$$

$$2\alpha\left[(V_1 - V_{TH})V_x - \frac{V_x^2}{2}\right] \quad (1.6)$$

Using KCL yields $I_2 = I_3$. Hence,

$$2\alpha\left[(V_1 - V_{TH})V_x - \frac{V_x^2}{2}\right] = \alpha \cdot (V_1 - V_x - V_{TH})^2 \quad (1.7)$$

$V_1 = 2V_{TH}$ is given in the exercise which yields

$$\alpha[2V_{TH}V_x - V_x^2] = \alpha \cdot (V_{TH} - V_x)^2 \quad (1.8)$$

Hence,

$$2V_{TH}V_x - V_x^2 = V_{TH}^2 + V_x^2 - 2V_xV_{TH} \quad (1.9)$$

Solving for V_x yields,

$$2V_x^2 - 4V_xV_{TH} + V_{TH} = 0 \quad (1.10)$$

and

$$V_x = V_{TH} \pm V_{TH}(1/\sqrt{2}). \quad (1.11)$$

The solution with a plus sign is a false solution since this leads to transistor M_3 is cut off ($V_{GS} < V_{TH}$). Hence,

$$V_x = \left(1 - \frac{1}{\sqrt{2}}\right)V_{TH} \quad (1.12)$$

2. Small-signal analysis

a) Sketch the small signal model of the circuit.

The circuit is a common source amplifier with a degeneration resistance at the source. This extra resistance can either be used in the circuit or it occurs due to the parasitic resistances in the ground. The equivalent small signal model of the amplifier is shown in Figure 2.1.

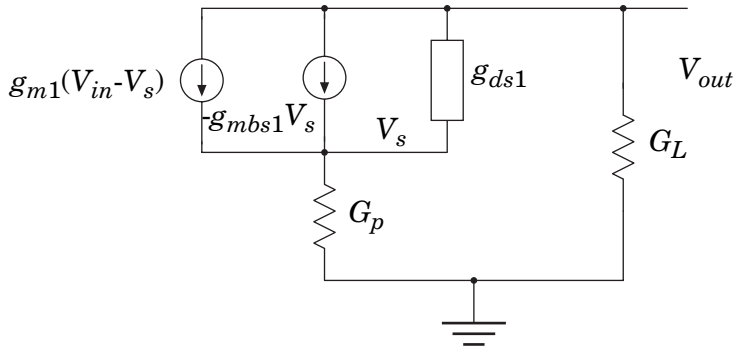

Figure 2.1 A small signal equivalent of the source degenerated amplifier.

b) Derive the DC gain of the circuit.

The DC gain is derived using nodal analysis in the nodes V_s and V_{out} which yields the following system of equations

$$g_{m1}(V_{in}-V_s)-g_{mbs1}V_s+g_{ds1}(V_{out}-V_s)-G_pV_s = 0 \quad (2.1)$$

$$g_{m1}(V_{in}-V_s)-g_{mbs1}V_s+g_{ds1}(V_{out}-V_s)+V_{out}G_L = 0 \quad (2.2)$$

Solving for V_s in (2.1) yields

$$V_s = \frac{g_{m1}V_{in}+g_{ds1}V_{out}}{g_{m1}+g_{mbs1}+g_{ds1}+G_p} \quad (2.3)$$

Inserting (2.3) into (2.2) yields

$$V_{in}\left(g_{m1}-\frac{g_{m1}(g_{m1}+g_{mbs1}+g_{ds1})}{g_{m1}+g_{mbs1}+g_{ds1}+G_p}\right)+V_{out}\left(g_{ds1}+G_L-\frac{g_{ds1}(g_{m1}+g_{mbs1}+g_{ds1})}{g_{m1}+g_{mbs1}+g_{ds1}+G_p}\right) = 0$$

which is simplified to

$$V_{in}\frac{g_{m1}G_p}{g_{m1}+g_{mbs1}+g_{ds1}+G_p}+V_{out}\frac{g_{ds1}G_p+G_L(g_{m1}+g_{mbs1}+g_{ds1}+G_p)}{g_{m1}+g_{mbs1}+g_{ds1}+G_p} = 0$$

and the transfer functions is then

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}G_p}{g_{ds1}G_p+G_L(g_{m1}+g_{mbs1}+g_{ds1}+G_p)} \quad (2.4)$$

which also is the DC gain of the circuit. If the R_p is very small it means that G_p is large. Hence, the transfer function can then be approximated to

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1}+G_L} \quad (2.5)$$

which is the expression for the DC gain of a common-source amplifier without the resistance R_p.

c) Derive the output resistance.

The output resistance is derived by adding a voltage source at the output of

the circuit with the value V_{out}. Then compute the current delivered by the voltage source under the assumption that the input sources are zeroed, Using nodal analysis in the nodes V_s and V_{out} yields

$$-(g_{m1}+g_{mbs1})V_s + g_{ds1}(V_{out}-V_s) - V_s G_p = 0 \quad (2.6)$$

$$-(g_{m1}+g_{mbs1})V_s + g_{ds1}(V_{out}-V_s) + V_{out}G_L - I_{out} = 0 \quad (2.7)$$

From (2.6) the voltage at node V_s can be solved

$$V_s = \frac{g_{ds1}}{g_{m1}+g_{mbs1}+g_{ds1}+G_p}V_{out} \quad (2.8)$$

Inserting (2.8) into (2.7) yields

$$\left(g_{ds1}+G_L - \frac{g_{ds1}(g_{m1}+g_{mbs1}+g_{ds1})}{g_{m1}+g_{mbs1}+g_{ds1}+G_p}\right)V_{out} = I_{out} \quad (2.9)$$

which can be expressed as

$$\frac{V_{out}}{I_{out}} = \frac{g_{m1}+g_{mbs1}+g_{ds1}+G_p}{g_{ds1}G_p + G_L(g_{m1}+g_{mbs1}+g_{ds1}+G_p)} \quad (2.10)$$

3. Noise analysis

a) Compute the equivalent input referred thermal noise spectral density generated by the amplifier.

The noise spectrum at the output is given by the squared transfer function from the noise source to the output times the noise source spectral density

$$S_{out}(f) = |H_1|^2 S_1(f) + |H_2|^2 S_2(f) \quad (3.1)$$

where H_1 in this case is the transfer function from the gate of transistor M_1 to the output and H_2 is the transfer function from the gate of transistor M_2 to the output. To compute the input referred spectral density the output referred spectral density is divided by the squared transfer function from the input to the output. Hence,

$$S_{in}(f) = \frac{S_{out}(f)}{|H_1|^2} = S_1(f) + \frac{|H_2|^2}{|H_1|^2}S_2(f) \quad (3.2)$$

The transfer functions equal

$$H_1 = \frac{g_{m1}}{g_{ds1}}\frac{g_{m2}}{g_{ds2}+sC_L} \quad (3.3)$$

and

$$H_2 = \frac{g_{m2}}{g_{ds2}+sC_L}. \quad (3.4)$$

The equivalent input referred spectral density for the thermal noise

generated by the amplifier is

$$S_{in}(f) = \frac{8kT}{3}\frac{1}{g_{m1}} + \frac{8kT}{3}\frac{1}{g_{m2}}\left(\frac{g_{ds1}}{g_{m1}}\right)^2 = \frac{8kT}{3g_{m1}}\left(1 + \frac{g_{ds1}^2}{g_{m1}g_{m2}}\right) \quad (3.5)$$

b) The effect of the noise spectral density

The small-signal parameters can be expressed as a function of the design parameters in the following way

$$g_m \propto \sqrt{2K\frac{W}{L}I_D} \quad (3.6)$$

and

$$g_{ds} = \lambda I_D \quad (3.7)$$

Hence, the spectral density can be expressed as

$$S_{in}(f) = \frac{8kT}{3\sqrt{2K\frac{W_1}{L_1}I_{bias1}}}\left(1 + \frac{\lambda_1^2 I_{bias1}^{3/2}}{\sqrt{2K\frac{W_1}{L_1}2K\frac{W_2}{L_2}I_{bias2}}}\right) \quad (3.8)$$

The DC gain is expressed as

$$A_0 = \frac{\sqrt{2K\frac{W_1}{L_1}}\sqrt{2K\frac{W_2}{L_2}}}{\lambda_1\lambda_2\sqrt{I_{bias1}I_{bias2}}} \quad (3.9)$$

and the first pole

$$p_1 = \frac{g_{ds2}}{C_L} = \frac{\lambda_2 I_{bias2}}{C_L} \quad (3.10)$$

Making the widths of the transistors twice as wide yield
decreased spectral density by a factor of about $\sqrt{2}$, increased DC gain by a factor of 2 and the first pole will not be changed.

Decreasing the currents to half their original value yield
increased spectral density by a factor of about $\sqrt{2}$ since the first term in (3.8) is the dominating term since $g_{ds} \ll g_m$. The DC gain is increased by a factor 2. and the first pole is decreased by a factor of 2.

4. Switched-capacitor circuit analysis

a) Compute the output voltage in the Z-domain.

The negative plate of the capacitors are assumed to be connected to the input of the active device (OTA). In the first clock cycle we have that
$q_1(t) = V_{in}(t)C_1$, $q_2(t) = 0$, $q_3(t) = C_3(V_{out}(t) - V_{os})$.
In the clock cycle $t + \tau$
$q_1(t+\tau) = -V_{os}C_1$, $q_2(t+\tau) = C_2(V_{out}(t+\tau) - V_{os})$,

$q_3(t+\tau) = C_3(V_{out}(t+\tau) - V_{os})$.
and in clock cycle $t+2\tau$
$q_1(t+2\tau) = V_{in}(t+2\tau)C_1$, $q_2(t+2\tau) = 0$,
$q_3(t+2\tau) = C_3(V_{out}(t+2\tau) - V_{os})$
The charge conservation equations are

$$-q_1(t) - q_2(t) - q_3(t) = -q_1(t+\tau) - q_2(t+\tau) - q_3(t+\tau) \quad (4.1)$$

$$q_3(t+\tau) = q_3(t+2\tau) \quad (4.2)$$

Equation (4.2) yields that $V_{out}(t+2\tau) = V_{out}(t+\tau)$. Further, (4.1) together with the former result yield
$-V_{in}(t)C_1 - C_3(V_{out}(t) - V_{os}) = V_{os}C_1 - C_2(V_{out}(t+2\tau) - V_{os}) - C_3(V_{out}(t+2\tau) - V_{os})$
Some simplifications give
$V_{in}(t)C_1 + C_3V_{out}(t) = -V_{os}(C_1 + C_2) + (C_2 + C_3)V_{out}(t+2\tau)$
Performing a Z transformation yields
$V_{out}(z)((C_2 + C_3)z - C_3) = V_{in}(z)C_1 + V_{os}(C_1 + C_2)$
and the output voltage is expressed as

$$V_{out}(z) = \frac{C_1}{C_2 + C_3} \frac{1}{z - \frac{C_3}{C_2 + C_3}} \left(V_{in} + V_{os}\left(1 + \frac{C_2}{C_1}\right)\right) \quad (4.3)$$

b) Is the circuit insensitive to parasitics?
The circuit together with the parasitics introduced by the switches and the top and bottom plate is shown in

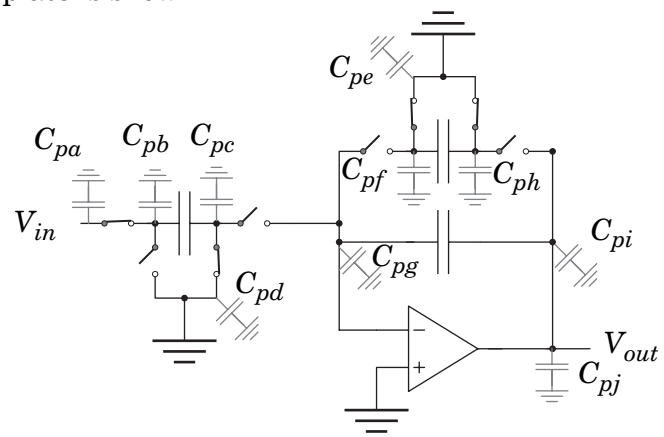

Figure 4.1 SC circuit with capacitive parasitics.

C_{pa} does not change the transfer function since it is connected to the input source.

C_{pb} is connected to the input source in ϕ_1 and discharged in ϕ_2. Hence, not changing the transfer function.

C_{pc}, C_{pf} Connected between ground and ground or ground and virtual ground. Not changing the transfer function.

C_{pd}, C_{pe} Connected between ground and ground and not changing the transfer function.

C_{pg} Connected between virtual ground and ground and thereby not changing the transfer function.

C_{ph} Ground- ground or ground- OTA output. Not changing the transfer function.

C_{pi}, C_{pj} connected between ground and to the output of the amplifier. Hence not changing the transfer function.

The circuit is insensitive to capacitive parasitics.

5. A mixture of questions

a) Compare fully differential vs. single-ended circuit.

Fully differential circuits are less sensitive to noise introduced in the power supplies. In an amplifier circuit the gain in a fully differential circuit is twice as large as in the single-ended counterpart.

Single-ended circuit have the benefit of not requiring a common-mode feedback circuit, which can be one of the thoughest circuits to be designed, depending on the requirements of the circuit.

b) Compute the transfer function of the opamp circuit.

Introducing two new voltages. V_{neg} is the voltage at the opamps negative input and V_x is the voltage at the output of opamp 1.

The voltage at the output is given by

$$V_{out} = (V_x - V_{neg})A_2 \tag{5.1}$$

and the voltage at V_x is given by

$$V_x = -V_{neg}A_1 \tag{5.2}$$

Furthermore, the current through the resistor R should be equal to the current through the capacitor C. Hence,

$$\frac{V_{in} - V_{neg}}{R} = (V_{neg} - V_{out})sC \tag{5.3}$$

Using (5.1) in combination with (5.2) yields

$$V_{neg} = -\frac{V_{out}}{(A_1 + 1)A_2} \tag{5.4}$$

inserting this equation into (5.3) yields

$$\frac{V_{in}}{R} = -V_{out}\left(\frac{1}{A_2(A_1 + 1)}\left(\frac{1}{R} + sC\right) + sC\right) \tag{5.5}$$

Hence,

$$\frac{V_{out}}{V_{in}} = \frac{1}{R}\frac{1}{sC + \frac{1}{A_2(A_1 + 1)}\left(\frac{1}{R} + sC\right)} = \frac{1}{sRC + \frac{1 + sRC}{A_2(A_1 + 1)}} \tag{5.6}$$

Which is an integrator when the gain of the amplifiers are large.

c) Compute CMR and OR of the circuit.

The common-mode range is given by

$$V_{inmin} = V_{dssat,5} + V_{gs,1} \propto \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{TH1} \tag{5.7}$$

$$V_{inmax} = V_{DD} - V_{dssat,3} - V_{dssat,1} + V_{gs,1} =$$

$$V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} + V_{TH1} \tag{5.8}$$

The output range is given by

$$V_{outmin} = V_{gs11} + V_{gs9} - V_{gs8} + V_{ds8} =$$

$$\sqrt{\frac{I_{D11}}{\alpha_{11}}} + V_{TH11} + \sqrt{\frac{I_{D9}}{\alpha_9}} + V_{TH9} - V_{TH8} \tag{5.9}$$

$$V_{outmax} = V_{DD} - V_{dssat,4} - V_{dssat,6} =$$

$$V_{DD} - \sqrt{\frac{I_{D4}}{\alpha_4}} - \sqrt{\frac{I_{D6}}{\alpha_6}} \tag{5.10}$$

d) Derive the minim DC current required fro the amplifier.

An RC circuit have to following charging time for linear settling

$$V_{out} = V_{step}A_0\left(1 - e^{-\frac{t}{R_{out}C_L}}\right) \tag{5.11}$$

The maximum slope of the circuit is the time derivative of the output voltage.

$$max\left\{\frac{dV_{out}}{dt}\right\} = \frac{V_{step}A_0}{R_{out}C_L} \tag{5.12}$$

If linear settling is required no slew rate limitation is to occur. The slew rate of the amplifier is given by

$$SR = \frac{I_{outmax}}{C_L} = \frac{2I_{D4}}{C_L} \tag{5.13}$$

where I_{D4} is the DC current of the amplifier. Hence, I_{D4} must be larger than

$$I_{D4} > \frac{V_{step}A_0}{2R_{out}} \tag{5.14}$$

for no slew rate limiting.

6. Extra exercise for students that have taken the course before 2002

a) Determine the gain and the poles of the circuit.

The gain and poles can be determined from the equivalent small signal scheme, ESSS, shown in Figure 6.1

The conductances g_{ds1} and g_{ds3} are parallel to g_{ds2} and g_{ds4} respectively.

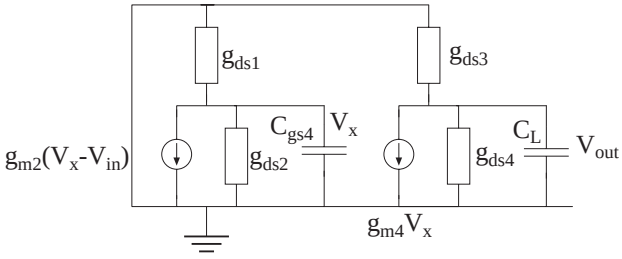

Figure 6.1 ESSS for the circuit.

Using nodal analysis in nodes V_x and V_{out} give the following equations.

$$g_{m2}(V_x - V_{in}) + V_x(g_{ds1} + g_{ds2} + sC_{gs4}) = 0 \tag{6.1}$$

$$g_{m4}V_x + V_{out}(g_{ds3} + g_{ds4} + sC_L) = 0 \tag{6.2}$$

Solving for V_x in Eq. (6.2) and inserting it in Eq. (6.1) gives the transfer function of the circuit according to

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m4}}{g_{ds3} + g_{ds4} + sC_L} \cdot \frac{g_{m2}}{g_{m2} + g_{ds1} + g_{ds2} + sC_{gs4}} \tag{6.3}$$

From the Eq. (6.3) we can identify the gain and the poles since $C_L \gg C_{gs4}$.

$$A_0 = \frac{-g_{m4}}{g_{ds3} + g_{ds4}} \cdot \frac{g_{m2}}{g_{m2} + g_{ds1} + g_{ds2}} \approx \frac{-g_{m4}}{g_{ds3} + g_{ds4}} \propto \frac{L_3}{L_3 + L_4}\sqrt{\frac{W_4 L_4}{I_{D4}}}$$

$$p_1 = \frac{g_{ds3} + g_{ds4}}{C_L}$$

$$p_2 = \frac{g_{m2} + g_{ds1} + g_{ds2}}{C_{gs4}}$$

b) Explain the use of each building block.

Transistors M1 and M2 are a Common-Drain gain stage that has the gain of approximately unity. This stage is used as a level shifter so that voltages

lower than V_T can be used as input (compare with just one common source stage).

Transistors M3 and M4 are a Common-Source stage that amplifies its input signal.

c) How do we increase the unity-gain frequency without increasing the total power dissipation? What will then happen with the gain of the circuit?

The unity-gain frequency for a system with well separated poles is determined by $\omega_u \approx A_0 p_1$. Using this relation together with Eq. and Eq. give

$$\omega_u \approx \frac{g_{m4}}{C_L} \propto \sqrt{\frac{W_4}{L_4} I_{D4}} \tag{6.4}$$

The unity-gain frequency can be increased without increasing the power consumption by increasing either W_4 or decreasing L_4.

An increased W_4 will increase the DC-gain, A_0.

A decreased L_4 will either increase or decrease the gain depending of the size of L_3. If length of the transistors M3 and M4 are equal then will a decreasing length equal a lower DC-gain.

d) How do we increase the output swing without changing the unity-gain frequency? What will happen with the gain of the circuit? (2p)

The output swing is

$$V_{out,\,min} = V_{ds4} = V_{eff4} = \sqrt{\frac{I_{D4} L_4}{K'_4 W_4}} \tag{6.5}$$

$$V_{out,\,max} = V_{dd} - V_{sd3} = V_{dd} - V_{eff3} = V_{dd} - \sqrt{\frac{I_{D3} L_3}{K'_3 W_3}} \tag{6.6}$$

The output swing can be increased by either increasing the size of W_3 or decreasing L_3, we must also adjust the bias voltage of M3 so the current through M3 is not changed.

An increased W_3 increases g_{m3} which will increase the gain of the common-drain building block and thereby the gain of the circuit. This increased gain will be a weak function of the transistor width.

A decreased L_3 will by the same argument decrease the gain. Do not forget that the output conductance of the transistors is proportional to the inverse of the transistor length.