Correct(?) Solutions to Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	August 16, 2001
Time:	14 - 18
Place:	Garnisonen
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. Written material and downloaded web-material except old exams. No textbooks are allowed.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

This exam covers nearly the whole course except the filter chapters. Our advise to you is to start by reading through the exam and then begin to solve the exercises that you are familiar with.

Exercise

1. Basic CMOS building blocks

a) Assume that V_{b3} is connected to ground. Determine the gain, the poles, and the zeros of the circuit. The only parasitic capacitance to consider is of M3. The load capacitance is much larger than all the other parasitics.

The gain, poles, and zeros can be determined from the equivalent small signal scheme, ESSS, shown in Figure 1.1.

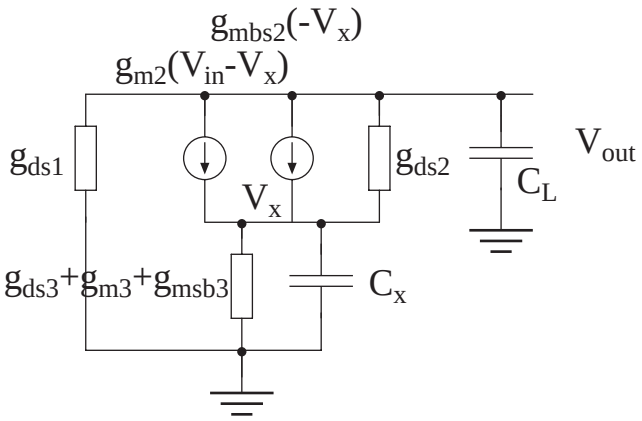

Figure 1.1 ESSS for the amplifier

Using nodal analysis in nodes V_x and V_{out} results in the following equations.

$$g_{m2}(V_{in}-V_x)+g_{mbs2}(-V_x)+(V_{out}-V_x)g_{ds2}+V_{out}(g_{ds1}+sC_L)\ =\ 0 \qquad (1.1)$$

$$g_{m2}(V_{in}-V_x)-g_{mbs2}V_x+(V_{out}-V_x)g_{ds2}-V_x(g_{ds3}+g_{m3}+g_{msb3}+sC_x)\ =\ 0 \qquad (1.2)$$

where $C_x = C_{sg3}+C_{sd3}$. Solving for V_x in Eq. (1.2) gives the transfer function of the circuit according to

$$V_x = \frac{g_{m2}V_{in} + g_{ds2}V_{out}}{g_{m2} + g_{mbs2} + g_{ds2} + g_{m3} + g_{msb3} + g_{ds3} + sC_x} \tag{1.3}$$

Insert Eq. (1.3) into Eq. (1.1) gives the transfer function.

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m2}(g_{m3} + g_{ds3} + g_{msb3} + sC_x)}{(g_{ds1} + g_{ds2} + sC_L)(g_{m3} + g_{ds3} + g_{msb3} + sC_x) + (g_{ds1} + sC_L)(g_{m2} + g_{mbs2} + g_{ds2})}$$

We can identify the gain, poles, and zero since $C_L \gg C_{gs4}$.

$$A_0 = -\frac{g_{m2}(g_{m3} + g_{ds3} + g_{msb3})}{(g_{ds1} + g_{ds2})(g_{m3} + g_{ds3} + g_{msb3}) + g_{ds1}(g_{m2} + g_{mbs2} + g_{ds2})} \approx$$

$$\approx -\frac{1}{\frac{(g_{ds1} + g_{ds2})}{g_{m2}} + \frac{g_{ds1}}{g_{m3} + g_{msb3} + g_{ds3}}\left(1 + \frac{g_{mbs2}}{g_{m2}}\right)}$$

$$p_1 \approx \frac{(g_{ds1} + g_{ds2})(g_{m3} + g_{ds3} + g_{msb3}) + g_{ds1}(g_{m2} + g_{mbs2} + g_{ds2})}{C_L(g_{m3} + g_{msb3} + g_{ds3} + g_{m2} + g_{mbs2} + g_{ds2}) + C_x(g_{ds1} + g_{ds2})} \approx$$

$$\frac{g_{ds1}}{C_L} + \frac{g_{ds2}(g_{m3} + g_{msb3})}{C_L(g_{m3} + g_{m2} + g_{msb3} + g_{mbs2})}$$

$$p_2 \approx \frac{(g_{m3} + g_{msb3} + g_{ds3} + g_{m2} + g_{mbs2} + g_{ds2})C_L + (g_{ds1} + g_{ds2})C_x}{C_L C_x} \approx$$

$$\frac{g_{m3} + g_{m2} + g_{mbs2} + g_{msb3}}{C_x}$$

$$z_1 = \frac{g_{m3} + g_{ds3} + g_{msb3}}{C_x} \approx \frac{g_{m3}}{C_x}$$

b) Derive an expression for the possible input swing of the circuit. Use relevant design parameters such as W, L, ...

The minimum and maximum input signal to ensure that all transistors work in saturation region is

$$V_{in,\,min} = V_{gs3} + V_{gs2}$$

$$V_{in,\,max} = V_{DD} - V_{sd1} - V_{ds2} + V_{gs2}$$

The minimum voltage drop between drain and source is defined as

$$V_{dsmin} = V_{gs} - V_T = V_{eff}$$

Solving for V_{eff} in the square-law relationship between the input voltage and the drain current of a CMOS transistor gives

$$V_{gs} - V_T = \sqrt{\frac{I_D}{\alpha}} = V_{eff}$$

and

$$V_{gs} = \sqrt{\frac{I_D}{\alpha}} + V_T$$

Insertion of the expressions for V_{gs} and V_{ds} gives

$$V_{in,\,min} = \sqrt{\frac{I_D}{K'_p \frac{W_3}{2L_3}}} + V_{T3} + \sqrt{\frac{I_D}{K'_n \frac{W_2}{2L_2}}} + V_{T2}$$

$$V_{in,\,max} = V_{DD} - \sqrt{\frac{I_D}{K'_p \frac{W_1}{2L_1}}} + V_{T2}$$

The common-mode range is then

$$CMR = \{V_{in,\,min}, V_{in,\,max}\}$$

c) Now assume that M3 is biased in the triode region. What will happen to the gain of the circuit when V_{b3} is varied? Why do we do build this type of circuit?

The small signal circuit will be the same except that the conductance $g_{m3} + g_{ds3}$ is replaced by a conductance of with the value of g_{ds3}, where

$$g_{ds3} = K'_p \frac{W_3}{L_3}(V_{sg3} - V_T - V_{sd3})$$

When V_{b3} is varied the conductance value will also vary linearly with the bias voltage.

$$A_0 = -\frac{1}{\frac{g_{ds1} + g_{ds2}}{g_{m2}} + \frac{g_{ds1}}{g_{ds3}}\left(1 + \frac{g_{mbs2}}{g_{m2}}\right)} \approx -\frac{1}{\frac{g_{ds1} + g_{ds2}}{g_{m2}} + \frac{g_{ds1}}{g_{ds3}}}$$

We can set g_{ds3} to be larger than g_{m2} and thereby is it possible to change the gain of the circuit by just adjusting V_{b3}.

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2. Operational transconductor amplifiers

a)Draw the small signal scheme for the amplifier. Do not forget the most important parasitics.

The small signal scheme will look like the one shown in Figure 2.1. $C_{p1} \approx C_{gs3} + C_{gs4}$ and $C_1 \approx C_{gs6}$.

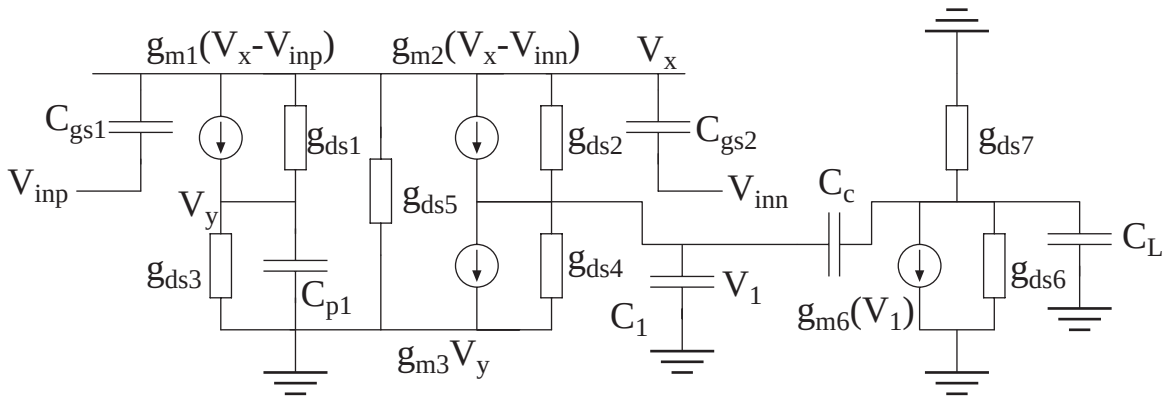

Figure 2.1 Small signal schematic with parasitics.

b) Derive the gain, poles, and zeros of the amplifier. Motivate all the approximations you are doing.

The first approximation come from the fact that C_{p1} is much smaller than C_c and C_L since the output node is often connected to many other stages and thereby is it large. The C_c is often even larger than C_L and $W_6 \gg W_3 = W_4$. Furthermore, the output resistance of transistor M5 is assumed to be very large which means that the g_{ds5} disappears at the same time as V_x can be considered small signal ground. The ESSS of the differential gain stage is simplified to the one shown in Figure 2.2.

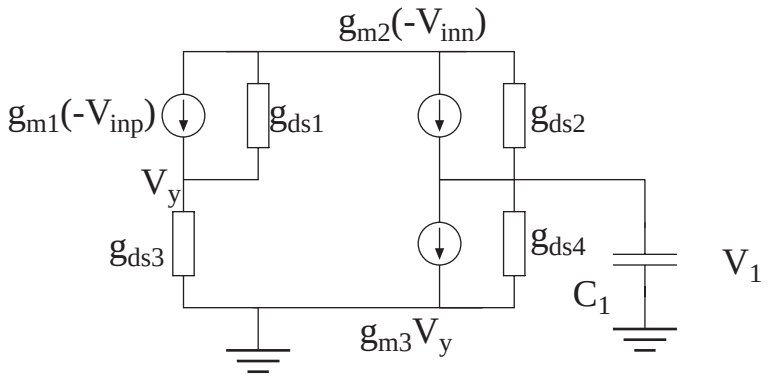

Figure 2.2 Simplified ESSS for the differential gain stage.

Nodal analysis in node V_y and V_1 gives

$$g_{m1}V_{inp} + V_y(g_{ds1} + g_{ds3}) = 0 \tag{2.1}$$

$$g_{m2}V_{inn} + V_1(g_{ds2} + g_{ds4} + sC_L) + g_{m3}V_y = 0 \tag{2.2}$$

Solving for V_y in Eq. (2.1) and inserting it in Eq. (2.2) give the transfer function from the input to the output.

$$V_1 = \frac{1}{g_{ds2}+g_{ds4}}\left(g_{m1}\frac{g_{m4}}{g_{m3}+g_{ds3}+g_{ds1}}V_{inp} - g_{m2}V_{inn}\right) \approx$$

$$\frac{g_{m2}}{g_{ds2}+g_{ds4}}(V_{inp}-V_{inn})$$

The approximation step comes from the fact the $g_{m3} \gg g_{ds1}+g_{ds3}$ together with the matching between the transistors M1-M2 and M3-M4.
The differential gain stage can be simplified to the first part of Figure 2.3

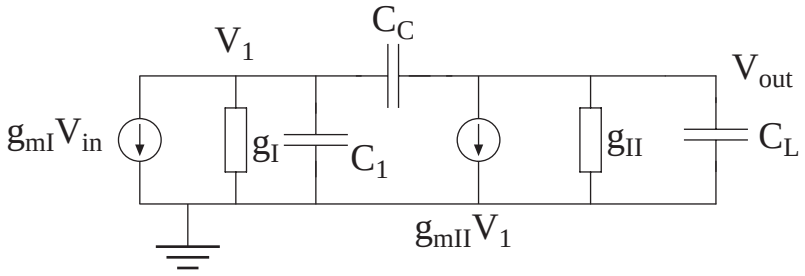

Figure 2.3 Simplified ESSS for the two stage amplifier

where

$$g_{mI} = g_{m2}$$

$$g_I = g_{ds2}+g_{ds4}$$

$$g_{mII} = g_{m6}$$

$$g_{II} = g_{ds6}+g_{ds7}$$

The second part of the ESSS comes from the common source gain stage at the output of the OTA.

Use nodal analysis to the left and right of the compensation capacitor gives the following equations.

$$g_{mI}(V_{inp}-V_{inn}) + V_1(g_I + sC_I) + sC_c(V_1 - V_{out}) = 0 \quad (2.3)$$

$$g_{mII}V_1 + V_{out}(g_{II}+sC_L) + (V_{out}-V_1)sC_c = 0 \quad (2.4)$$

The transfer function can be found by combining Eq. (2.3) and Eq. (2.4).

$$\frac{V_{out}}{V_{inp}-V_{inn}} = \frac{g_{mI}(g_{mII}-sC_c)}{g_I g_{II} + s(g_I(C_L+C_c)+g_{II}(C_I+C_c)+C_c g_{mII}) + s^2 C_L C_c} \quad (2.5)$$

We can now determine the DC-gain, poles, and zeros directly from the transfer function.

$$A_0 = \frac{g_{mI}g_{mII}}{g_I g_{II}}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c}$$

$$p_2 \approx \frac{g_I}{C_c} + \frac{g_I + g_{II} + g_{mII}}{C_L} + \frac{C_I g_{II}}{C_c C_L} \approx \frac{g_{mII}}{C_L} \approx \frac{\sqrt{2\mu C_{ox}\frac{W_6}{L_6} I_{D6}}}{C_L}$$

$$z_1 = -\left(\frac{g_{mII}}{C_c} \approx \frac{\sqrt{2\mu C_{ox}\frac{W_6}{L_6} I_{D6}}}{C_C} \right)$$

c) Determine two ways to increase the unity-gain frequency of the amplifier. What will happen to the phase margin, common-mode range, and the DC voltage at node x?

The unity-gain frequency of the amplifier with separated poles is

$$w_u = A_o p_1 = \frac{g_{mI}}{C_c} \approx \frac{\sqrt{2\mu_n C_{ox}\frac{W_2}{L_2} I_{D2}}}{C_c}$$

There are three different ways to increase the unity-gain frequency.

1) Increase W_2/L_2.

This will only increase the unity-gain not the second pole or the zero and thereby the phase margin will decrease, since the unity-gain frequency will be closer to the second pole.

The common-mode range is

$$\sqrt{\frac{I_{D2}}{\alpha_3}} + V_{T3} - V_{T1},\ V_{DD} - \sqrt{\frac{I_{D2}}{2\alpha_5}} - \sqrt{\frac{I_{D2}}{\alpha_1}} - V_{T1} \qquad (2.6)$$

Increasing W_2/L_2 will increase α_1 and thereby the common-mode range will increase.

If we start by looking at the drain current expression for a saturated transistor:

$$I_D = K\frac{W_2}{L_2}(V_{sg2} - V_{T2})^2(1 + \lambda V_{sd2}) \qquad (2.7)$$

Furthermore, we know that I_D will constant while W_2/L_2 will increase at the same time as V_{g2} and V_{d2} will be constant. This results in a decreased V_x voltage.

2) Increase the current through transistor M2, I_{D2}.

This increment will not change the phase margin of the amplifier, since the unity-gain frequency will increase as fast as both the second pole as the zero.

The common-mode range will decrease and the voltage at node x will increase since V_{g2} will be constant and V_{d2} will increase.

3) Decrease C_c

The phase margin will decrease since p2 will lay still while z_1 will increase.

The common-mode range and V_x will be constant.

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3. Noise

a) Derive the total thermal output noise power of the circuit. All parasitics are much smaller than C_L. The spectral density function of for the resistor is given by

$$V_R^2(f) = 4kTR$$

The ESSS is shown in Figure 3.1.

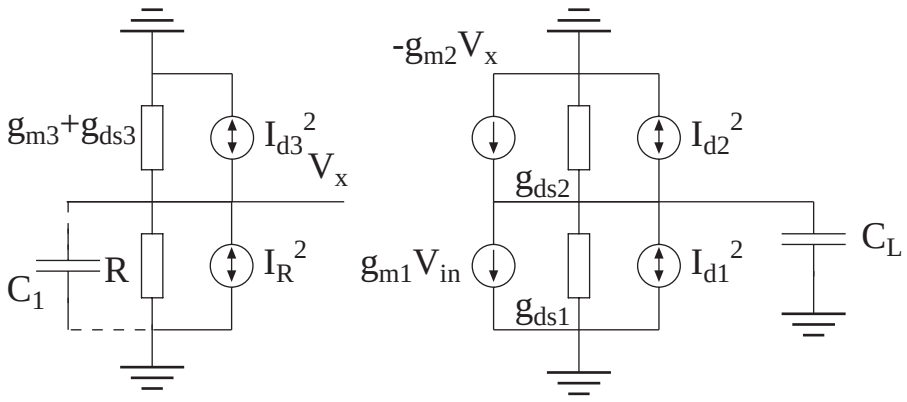

Figure 3.1 The ESSS of the noisy circuit.

We have to calculate the transfer function from the drain of transistor M1 to the output, H1, from transistor M2 to the output, H2, from transistor M3 to the output, H3, and from the resistor to the output, H4.

Consider a current source at in parallel with transistor M1 this will give a transfer function from that current source to the output according to

$$H1 = -\frac{1}{g_{ds1} + g_{ds2} + sC_L} \tag{3.1}$$

the pole is located in

$$p_1 = \frac{g_{ds1} + g_{ds2}}{C_L} \tag{3.2}$$

(3.3)

Continuing with the transfer function from the noise current source in transistor M2 to the output.

$$H2 = H1 \tag{3.4}$$

The transfer function from M3 to the output is given by

$$H_3 = \frac{V_{out}}{V_x}\frac{V_x}{I_{nM3}} = -\frac{g_{m2}}{g_{ds1}+g_{ds2}+sC_L}\frac{1}{g_{ds3}+g_{m3}+\frac{1}{R}} \tag{3.5}$$

The transfer function from the resistor to the output is given by

$$H_4 = \frac{V_{out}}{V_x}\frac{V_x}{I_R} = -\frac{g_{m2}}{g_{ds1}+g_{ds2}+sC_L}\frac{1}{g_{ds3}+g_{m3}+\frac{1}{R}} \tag{3.6}$$

The spectral density function of the output can be calculated as

$$S_{out}(f) = \left|H_1(f)\right|^2 I^2_{n1} + \left|H_2(f)\right|^2 I^2_{n2} + \left|H_3(f)\right|^2 I^2_{n3} + \left|H_4(f)\right|^2 I^2_R \tag{3.7}$$

where

$$I_{ni} = \frac{8kT}{3}g_{mi} \tag{3.8}$$

The noise power at the output can now be calculated according to

$$V^2_{out} = \int_0^\infty S_{out}(f)df \tag{3.9}$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see chapter 4 in Johns&Martin). The integral of a one pole system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V^2_{out} = \frac{2kT}{g_{ds2}+g_{ds1}}\frac{1}{C_L}\left(\frac{g_{m1}}{3}+\frac{g_{m2}}{3}+\frac{g^2_{m2}}{\left(\frac{1}{R}+g_{m3}+g_{ds3}\right)^2}\left(\frac{g_{m3}}{3}+\frac{1}{2R}\right)\right) \tag{3.10}$$

b) Describe two ways to decrease the thermal output noise power of the circuit by changing relevant design parameter. What will happen to the gain and the unity-gain frequency?

1) Increase the load capacitor. This will decrease the unity-gain frequency of the amplifier but the gain will not change.

2) Decrease the resistance R. This will increase the current through transistor M3 and thereby through all transistors.

The output noise voltage is approximately proportional to the inverse of the square root of the current through transistor M1. $g_{m3} \gg 1/R$ is assumed. Increasing the current will decrease the gain of the circuit but increase the unity-gain frequency.

3) Decrease the size of M1. Decreases the gain and the unity-gain.

4) Decrease the size of both M2 and M3 => approximately constant current. No change will happen to neither the gain nor the unity-gain frequency.

c) Add a large capacitor $C_1 \gg C_L$ in parallel with the resistor. Furthermore assume that $1/R \gg g_{out}$. What will happen to the output noise power?

The ESSS is the same as in Figure 3.1.
The transfer function H1 and H2 will not be affected but H3 and H4 will be changed.

$$H_3 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \tag{3.11}$$

$$H_4 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \tag{3.12}$$

The dominating pole of both H3 and H4 are approximately

$$p = \frac{\frac{1}{R} + g_{m3} + g_{ds3}}{C_1} \tag{3.13}$$

Using the same way to calculate the output noise as in 3a) gives

$$V_{out}^2 = \frac{2kT}{g_{ds2} + g_{ds1}} \left(\frac{1}{3C_L}(g_{m1} + g_{m2}) + \frac{g_{m2}^2}{g_{ds2} + g_{ds1}} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3}} \left(\frac{g_{m3}}{3C_1} + \frac{1}{2R} \right) \right)$$

4. Switched capacitor circuits

a) Derive the transfer function from V_1 to V_2.

The circuit is shown in Figure 4.1.

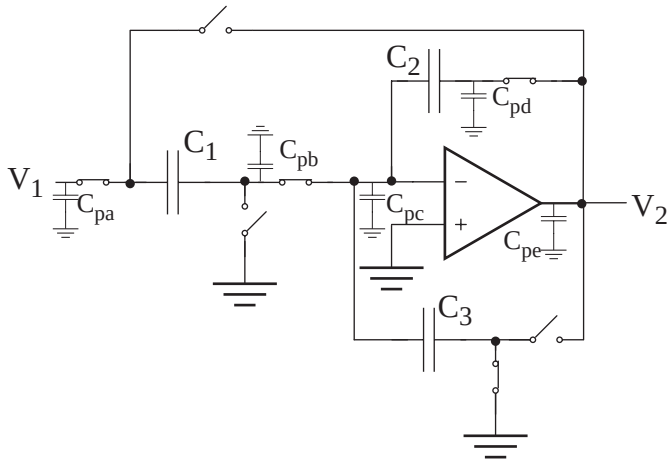

Figure 4.1 The SC circuit with parasitic capacitances

V_n is the input voltage of the amplifier. The transfer function can be derived by using charge analysis.

t:

$$q_1(t) = C_1(V_1(t) - V_n(t)) \tag{4.1}$$

$$q_2(t) = C_2(V_2(t) - V_n(t)) \tag{4.2}$$

$$q_3(t) = C_3(-V_n(t)) \tag{4.3}$$

t+τ:

$$q_1(t+\tau) = C_1 V_2(t+\tau) \tag{4.4}$$

$$q_2(t+\tau) = q_2(t) \tag{4.5}$$

$$q_3(t+\tau) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{4.6}$$

t+2τ:

$$q_1(t+2\tau) = C_1(V_1(t+2\tau) - V_n(t+2\tau)) \tag{4.7}$$

$$q_2(t+2\tau) = C_2(V_2(t+2\tau) - V_n(t+2\tau)) \tag{4.8}$$

$$q_3(t+2\tau) = -C_3 V_n(t+2\tau) \tag{4.9}$$

Charge redistribution

$$q_2(t) + q_3(t) = q_2(t+\tau) + q_3(t+\tau) \tag{4.10}$$

$$q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{4.11}$$

We also know that $V_2 = A(V_p - V_n)$ where V_p and V_n is the positive and negative input node of the OTA respectively. An offset voltage of the OTA is modelled by a voltage source in at the positive input. Solve for V_n.

$$V_n = -\frac{V_2}{A} + V_{os} \tag{4.12}$$

Eq. (4.10) gives that

$$-C_3 V_n(t) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{4.13}$$

Solving this equation gives

$$V_2(t+\tau) = \frac{V_2(t)}{(A+1)} \tag{4.14}$$

Inserting all necessary equations in Eq. (4.11) gives the following transfer function:

$$V_2(z) = -\frac{C_1}{C_2 + \frac{1}{A}(C_1 + C_2 + C_3)} \frac{(zV_1(z) - V_{os})}{z - 1 + \frac{\frac{C_1}{A+1}}{C_2(A+1) + C_1 + C_3}} \tag{4.15}$$

b) Is the circuit insensitive to parasitics?

Yes it is insensitive to parasitics.

Parasitics:

C_{pa} is connected to an ideal voltage source is will not affect the transfer function.

C_{pb} is connected between ground and virtual ground or ground and ground so it will not affect the transfer function.

C_{pc} is connected between ground and virtual ground so it will not affect the transfer function

C_{pd} is either connected to the output of the OTA or it will not be connected so it will not affect the transfer function.

C_{pe} is connected to the output of the OTA and thereby not change the transfer function.

c) Find the settling time constants, i.e. the speed of the circuit, for both clock phases. Neglect the influence of the switches.

The settling time constant is the same as the inverse of the w_{-3dB} frequency. From the feedback theory we know that

$$w_{-3dB} = \beta w_u \tag{4.16}$$

where β is the feedback factor.

For clock phase 1 (t, $t + 2\tau$, ...)

$$\beta_1 = \frac{\dfrac{1}{C_1 + C_3 + C_{pb} + C_{pc}}}{\dfrac{1}{C_2} + \dfrac{1}{C_1 + C_3 + C_{pb} + C_{pc}}} = \frac{C_2}{C_2 + C_1 + C_3 + C_{pb} + C_{pc}} \tag{4.17}$$

For clock phase 2 ($t + \tau$, $t + 3\tau$, ...)

$$\beta_2 = \frac{\dfrac{1}{C_{pc}}}{\dfrac{1}{C_3} + \dfrac{1}{C_{pc}}} = \frac{C_3}{C_3 + C_{pc}} \tag{4.18}$$

β_1 is probably much smaller than β_2 and thereby is the circuit slower in clock phase 1 than in clock phase 2.

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5. A mixture of questions

a) Determine the common-mode range and the maximum swing of the control signal, V_{cnrtl}, of the common-mode feedback circuit

The Common-mode range of the Common-mode feedback circuit is

$$V_{in,\,min} = V_{gs6} + V_{sd_1} - V_{sg1} = \sqrt{\frac{I_{D6}}{\alpha_6}} + V_{T6} - V_{T1} \tag{5.1}$$

$$V_{in,\,max} = V_{DD} - V_{sd7} - V_{sd8} - V_{sg1} = V_{DD} - \sqrt{\frac{I_{D7}}{\alpha_7}} - \sqrt{\frac{I_{D7}}{\alpha_8}} - \sqrt{\frac{I_{D1}}{\alpha_1}} - V_{T1} \tag{5.2}$$

$$CMR = \{V_{in,\,min}, V_{in,\,max}\} \tag{5.3}$$

The maximum swing of the V_{cnrtl} is

$$V_{cnrtl,\,min} = V_{gs5} = \sqrt{\frac{I_{D5}}{\alpha_5}} + V_{T5} \tag{5.4}$$

$$V_{cnrtl,\,max} = V_{DD} - V_{sd7} - V_{sd8} - V_{sd2} = V_{DD} - \sqrt{\frac{I_{D7}}{\alpha_7}} - \sqrt{\frac{I_{D7}}{\alpha_8}} - \sqrt{\frac{I_{D2}}{\alpha_2}} \tag{5.5}$$

b) Determine the output resistance of the circuit.

The output impedance is determined by

$$\left.\frac{V_{out}}{I_{out}}\right|_{I_{in} = 0} \tag{5.6}$$

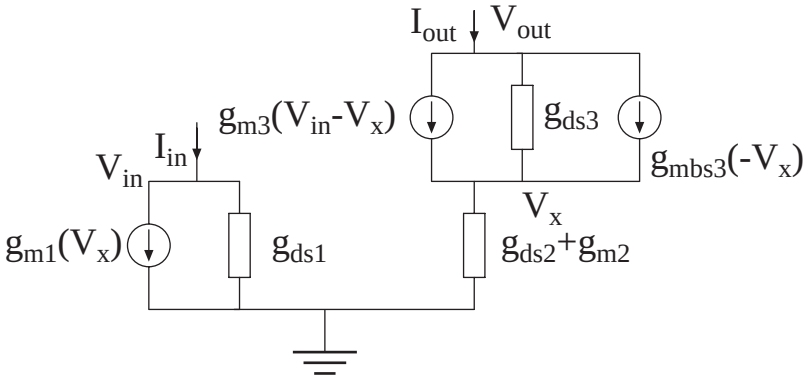

Figure 5.1 ESSS for the current mirror

Using nodal analysis in the ESSS shown in Figure 5.1 we get the following equations

$$I_{out} = g_{m3}(V_{in} - V_x) + (V_{out} - V_x)g_{ds3} \tag{5.7}$$

$$I_{out} = V_x(g_{m2} + g_{ds2}) \tag{5.8}$$

$$g_{m1}V_x + V_{in}g_{ds1} = 0 \tag{5.9}$$

Solve for V_{out} as a function of I_{out}.

$$R_{out} = \frac{(g_{m2} + g_{ds2})g_{ds1} + g_{m3}(g_{m1} + g_{ds1}) + g_{ds1}g_{ds3}}{g_{ds3}(g_{m2} + g_{ds2})g_{ds1}} \approx \frac{1}{g_{ds3}} + \frac{1}{g_{m2}} + \frac{g_{m3}g_{m1}}{g_{m2}g_{ds1}g_{ds3}}$$

c) Sketch the output signal of the circuit as a function of the input signal, when the input signal ramps from ground to V_{DD}. Determine the operation region of the transistor in the diagram.

For large input voltages, $V_{in} \approx V_{DD}$, the transistor is in the cut-off region and no current will flow through the circuit. The output voltage of the circuit will be very close to zero volt.

For small input voltages, $V_{in} \approx 0$, the transistor will work in the linear region. The maximum output voltage of the circuit is when V_{in} approximately equal to zero, then the output voltage is equal to

$$V_{DD}\frac{R_L}{R_L + R_S}$$

For some signal in between $V_{DD} - V_T$ and ground the transistor will be in the saturation region. When does the transistor change from operating in the linear region to the saturation region? It is exactly when $V_{sd} = V_{sg} - V_T$. The input voltage that fulfills the equation $V_{sd} = V_{sg} - V_T$ is called V_x

We know that

$$I_D = \alpha(V_{sg}-V_T)^2 \tag{5.10}$$

$$V_{sd} = V_{DD}-(R_L+R_S)I_D \tag{5.11}$$

$$V_{out} = R_L I_D \tag{5.12}$$

Insert Eq. (5.11) and Eq. (5.12) into Eq. (5.10)

$$I_D = \alpha(V_{DD}-(R_L+R_S)I_D)^2 \tag{5.13}$$

Solving the above equations gives I_D = ... and the V_x = ...

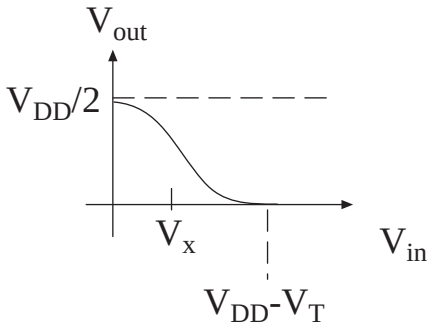

Figure 5.2 Output voltage as a function of input voltage

d) Clock feedthrough, CFT, appears both from clock leakage of the switches and from the channel discharge of a transistor that is going to be in the cut-off region.

The CFT adds extra unwanted charge to the capacitors in the SC circuit and thereby causing gain-errors, distortion, dc-offset, and nonlinearity.