# Correct(?) Solutions to Written Test
# TSTE80,
# Analog and Discrete-time Integrated Circuits

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|---|---|
| Date | May 31, 2001 |
| Time: | 8 - 12 |
| Place: | Garnisonen |
| Max. no of points: | 70;<br>50 from written test,<br>15 for project, and 5 the assignment. |
| Grades: | 30 for 3, 42 for 4, and 56 for 5. |
| Allowed material: | No LapTops. No text book in analog design such as Johns & Martin *"Analog Integrated Circuit Design"*. No dedicated compedia such as Eriksson *"Aktiva RC-filter och SC-filter"* or *"Exempelsamling"*. Pocket calculators are allowed. Written material, downloaded web-material, except old exams are allowed. |
| Examiner: | Lars Wanhammar. |
| Responsible teacher: | Robert Hägglund.<br>Tel.: 013 - 28 16 76 (3). |
| Correct (?) solutions: | Solutions and results will be displayed June in House B, entrance 25 - 27, 1st floor. |

## Good Luck!

# Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

This exam covers nearly the whole course except the filter chapters. Our advise to you is to start by reading through the exam and then begin to solve the exercises that you are familiar with.

# Exercise

## 1. Basic CMOS building blocks

a) Determine the gain and the poles of the circuit.

The gain and poles can be determined from the equivalent small signal scheme, ESSS, shown in Figure 1.1

The conductances $g_{ds1}$ and $g_{ds3}$ are parallel to $g_{ds2}$ and $g_{ds4}$ respectively.

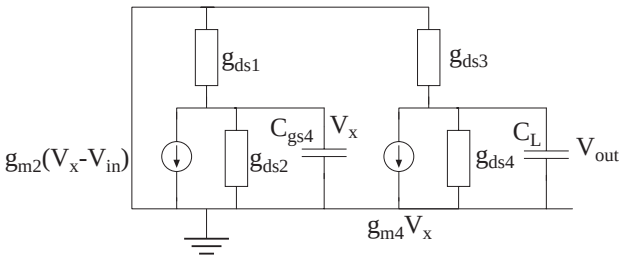



***Figure 1.1*** ESSS for the circuit.

Using nodal analysis in nodes $V_x$ and $V_{out}$ give the following equations.

$$g_{m2}(V_x - V_{in}) + V_x(g_{ds1} + g_{ds2} + sC_{gs4}) = 0 \qquad (1.1)$$

$$g_{m4}V_x + V_{out}(g_{ds3} + g_{ds4} + sC_L) = 0 \qquad (1.2)$$

Solving for $V_x$ in Eq. (1.2) and inserting it in Eq. (1.1) gives the transfer function of the circuit according to

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m4}}{g_{ds3} + g_{ds4} + sC_L} \cdot \frac{g_{m2}}{g_{m2} + g_{ds1} + g_{ds2} + sC_{gs4}} \qquad (1.3)$$

From the Eq. (1.3) we can identify the gain and the poles since $C_L \gg C_{gs4}$.

$$A_0 = \frac{-g_{m4}}{g_{ds3} + g_{ds4}} \cdot \frac{g_{m2}}{g_{m2} + g_{ds1} + g_{ds2}} \approx \frac{-g_{m4}}{g_{ds3} + g_{ds4}} \propto \frac{L_3}{L_3 + L_4}\sqrt{\frac{W_4 L_4}{I_{D4}}}$$

$$p_1 = \frac{g_{ds3} + g_{ds4}}{C_L}$$

$$p_2 = \frac{g_{m2} + g_{ds1} + g_{ds2}}{C_{gs4}}$$

b) Explain the use of each building block.

Transistors M1 and M2 are a Common-Drain gain stage that has the gain of approximately unity. This stage is used as a level shifter so that voltages

lower than $V_T$ can be used as input (compare with just one common source stage).

Transistors M3 and M4 are a Common-Source stage that amplifies its input signal.

c) How do we increase the unity-gain frequency without increasing the total power dissipation? What will then happen with the gain of the circuit?

The unity-gain frequency for a system with well separated poles is determined by $\omega_u \approx A_0 p_1$. Using this relation together with Eq. and Eq. give

$$\omega_u \approx \frac{g_{m4}}{C_L} \propto \sqrt{\frac{W_4}{L_4} I_{D4}} \tag{1.4}$$

The unity-gain frequency can be increased without increasing the power consumption by increasing either $W_4$ or decreasing $L_4$.

An increased $W_4$ will increase the DC-gain, $A_0$.

A decreased $L_4$ will either increase or decrease the gain depending of the size of $L_3$. If length of the transistors M3 and M4 are equal then will a decreasing length equal a lower DC-gain.

d) How do we increase the output swing without changing the unity-gain frequency? What will happen with the gain of the circuit? (2p)

The output swing is

$$V_{out,\,min} = V_{ds4} = V_{eff4} = \sqrt{\frac{I_{D4} L_4}{K'_4 W_4}} \tag{1.5}$$

$$V_{out,\,max} = V_{dd} - V_{sd3} = V_{dd} - V_{eff3} = V_{dd} - \sqrt{\frac{I_{D3} L_3}{K'_3 W_3}} \tag{1.6}$$

The output swing can be increased by either increasing the size of $W_3$ or decreaseing $L_3$, we must also adjust the bias voltage of M3 so the current through M3 is not changed.

An increased $W_3$ increases $g_{m3}$ which will increase the gain of the common-drain building block and thereby the gain of the circuit. This increased gain will be a weak function of the transistor width.

A decreased $L_3$ will by the same argument decrease the gain. Do not forget that the output conductance of the transistors is proportional to the inverse of the transistor length.

e) Assume that the we like to use building blocks to increase the output resistance of a common-source gain stage with cascodes. How are they connected to the common-source stage? Explain with a schematic of the

gain-boosted circuit where only transistors are shown together with a short text.

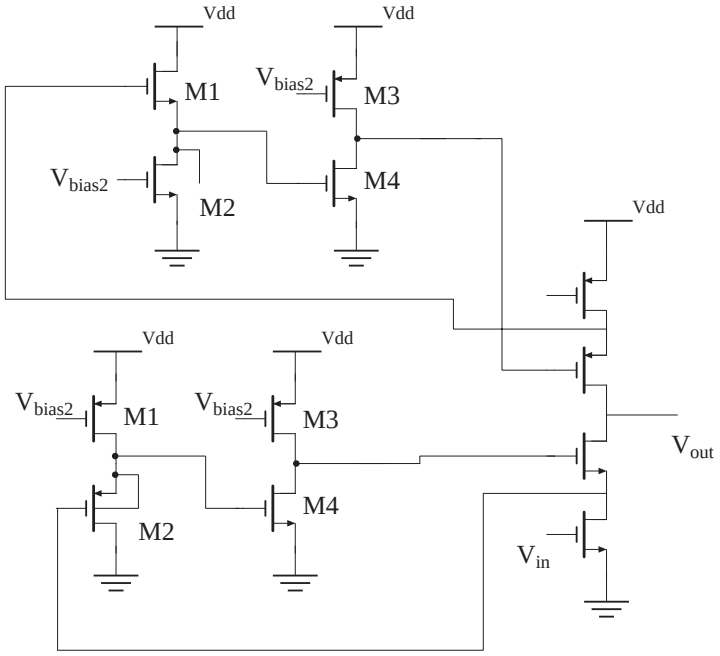



***Figure 1.2*** Gain-boosting circuit.

The full schematic is shown in Figure 1.2. The upper gain stage has nmos transistors as input transistors in the Common-Drain circuit whereas the lower gain stage uses pmos transistors as input transistors. These are chosen to increase the possible swing in the circuit.

## 2. Operational transconductor amplifiers

The power supply of the circuit are 3.3V and 0V respectively. Assume that all internal parasitics are small.

a) Explain the function of every transistor in the two-stage amplifier.

M1 and M2 are the input transistors.

M3 and M4 are connected in a current mirror configuration. M3 is reflecting the current from the left branch to the right through M4.

M5 are used as a current source to approximately hold a constant drain current.

M6 and M9 are a common-source gain stage.

M7 and M8 are cascodes to increase the output resistance.

b) Derive the common-mode range, CMR, and the output range, OR, of the circuit. Propose **two** ways to increase the output range.

$$I_D = \alpha(V_{gs} - V_T)^2 = \alpha V_{eff}^2 \tag{2.1}$$

Solving for $V_{eff}$ gives

$$V_{eff} = \sqrt{\frac{I_D}{\alpha}} \tag{2.2}$$
$$V_{gs} = V_{eff} + V_T$$

The minimum value of $V_{ds}$ are $V_{gs} - V_T = V_{eff}$ for all transistors if it should work in the saturation region.

The common-mode range are

$$V_{in,min} = V_{ds5} + V_{gs1} = V_{eff5} + V_{eff1} + V_{T1} = \tag{2.3}$$
$$\sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D1}}{\alpha_1}} + V_{T1}$$

$$V_{in,max} = V_{dd} - V_{sg3} - V_{ds1} + V_{gs1} \tag{2.4}$$
$$= V_{dd} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} + V_{T1}$$

The output range are

$$V_{out,min} = V_{ds9} + V_{ds8} = \sqrt{\frac{I_{D9}}{\alpha_9}} + \sqrt{\frac{I_{D8}}{\alpha_8}} \tag{2.5}$$

$$V_{out,max} = V_{dd} - V_{sd6} - V_{sd7} = V_{dd} - \sqrt{\frac{I_{D6}}{\alpha_6}} - \sqrt{\frac{I_{D7}}{\alpha_7}} \tag{2.6}$$

Assume that all transistor length are the same. The output range can be increase by decreasing the current through the last gain stage or by

increasing the width of the transistors M6 to M9.

c) Propose one way to increase the DC-gain. What will then happen with the unity-gain frequency and the phase margin?

Here it is appropriate to make some assumptions.

1) The output conductance of M5 are very small. Approximate it by zero.

2) Assume that transistor M3 does not affect the transfer function.

3) The parasitics of the transistors are very small compared to $C_C$ and $C_L$.

These assumptions give that the small signal scheme looks like Figure 2.1

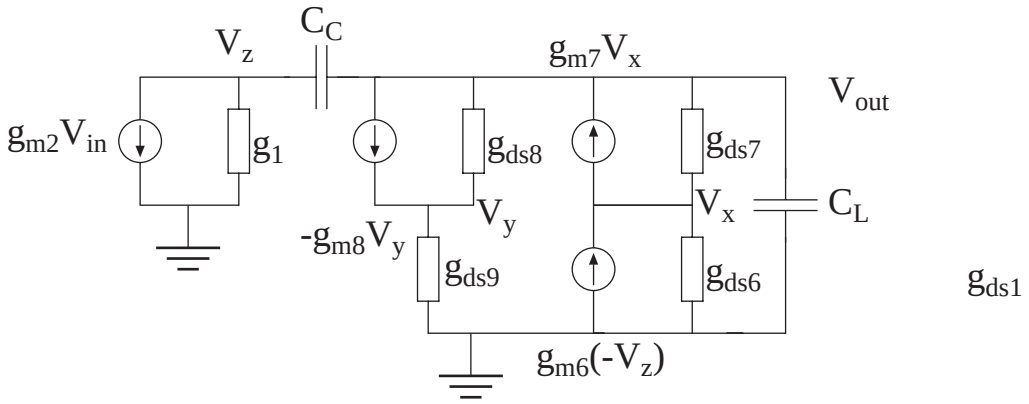



***Figure 2.1*** The small signal schematic of the two-stage OTA.

where $g_1 = g_{ds2} + g_{ds4}$. We can simplify this circuit by computing the thevenin equivalent of the output stage. The simplified circuit is shown in

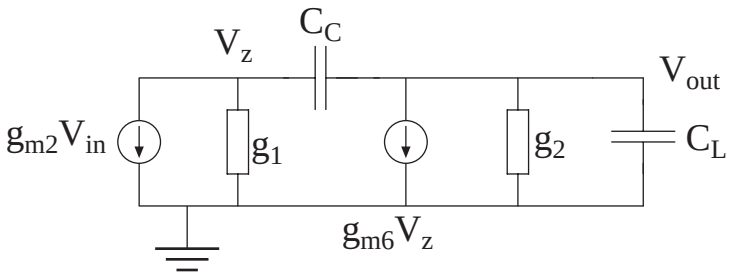



***Figure 2.2*** The simplified circuit.

where

$$g_2 \approx \frac{g_{ds6}g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds9}}{g_{m8}} \tag{2.7}$$

Use nodal analysis to the left and right of $C_C$ gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}(g_{m6} - sC_C)}{g_1g_2 + s(C_L(g_1) + C_C(g_1 + g_2 + g_{m6})) + s^2C_LC_C} \tag{2.8}$$

Assume that $C_C \approx C_L$. This assumption gives that the first and second pole are well separated.

$$A_0 = \frac{g_{m2}g_{m6}}{g_1 g_2} \tag{2.9}$$

$$p_1 \approx \frac{g_1 g_2}{g_{m6} C_C} \tag{2.10}$$

$$p_2 \approx \frac{g_{m6}}{C_L} \tag{2.11}$$

$$z_1 \approx \frac{g_{m6}}{C_C} \tag{2.12}$$

The unity-gain frequency are approximately $A_0 p_1$ for an amplifier with well separated poles. This gives

$$\omega_u \approx \frac{g_{m2}}{C_C} \tag{2.13}$$

The gain of the circuit can be increased for example by

**Table 1: Some ways to increasing the gain**

| Change | gain | unity-gain | phase margin |
|---|---|---|---|
| Increase $W_2$ | Increases | Increased | decreases since p2 not affected |
| Increase $W_6$ | Increases | not affected | increases since p2 increase. |

There are quite many other ways to increase the gain.

d) The amplifier is connected. What will the output voltage from the amplifier look like when the input voltage is $V_{in} = V_{DC} + 0.1\sin(2\pi 100 \cdot 10^3 t)$? Assume that $V_{CMR,\,min} < V_{DC} < V_{CMR,\,max}$

The negative input voltage of the amplifier is floating since there is no dc-path its input. To solve this we have to assign a charge to the capacitor at the negative input of the OTA. If for example the charge at the negative input is zero the input voltage of the negative input will be zero and thereby will the OTA not be properly biased and the gain will be very small so the output voltage from the amplifier will not be the expected by small signal analysis.

## 3. Noise

Assume that transistors M1 and M2 generate thermal noise only. Furthermore, $I_{bias1}$ and $I_{bias2}$ can be seen as DC current sources. Assume that $C_{gs} \ll C_L$.

a) Derive the total output noise power.

The ESSS is shown in Figure 3.1.

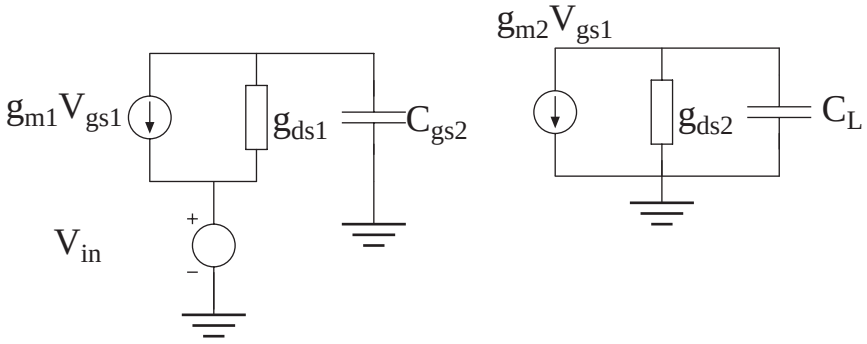



***Figure 3.1*** The ESSS of the noisy circuit

We have to calculate the transfer function from the gate of transistor M1 to the output, H1, from transistor M2 to the output, H2, and from the $V_{in}$ to the output, H.

$$H1 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2C_LC_{gs2}} \tag{3.1}$$

According to exercise 2 the poles of the transfer function can be extracted directly.

$$p_{11} \approx \frac{g_{ds2}}{C_L} \tag{3.2}$$

and

$$p_{12} \approx \frac{g_{ds1}}{C_{gs2}} \tag{3.3}$$

Continuing with the transfer function from the gate of M2 to the output.

$$H2 = -\frac{g_{m2}}{g_{ds2} + sC_L} \tag{3.4}$$

The transfer function from $V_{in}$ to the output is

$$H = \frac{(g_{m1} + g_{ds1})g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2C_LC_{gs2}} \tag{3.5}$$

The spectral density of the output can be calculated as

$$S_{out}(f) = |H_1(f)|^2 V_{n1} + |H_2(f)|^2 V_{n2} \tag{3.6}$$

where

$$V_{ni} = \frac{8kT}{3}\frac{1}{g_{mi}} \tag{3.7}$$

The noise power at the output can now be calculated according to the equation below

$$V_{out}^2 = \int_0^\infty S_{out}(f)df \tag{3.8}$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see chapter 4 in Johns&Martin). The integral of a one pole

system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V_{out}^2 = \frac{2kT}{3}\frac{g_{m2}}{g_{ds2}}\frac{1}{C_L}\left(\frac{g_{m1}g_{m2}}{g_{ds1}^2}+1\right) \tag{3.9}$$

b) Derive the noise voltage that can be referred to the input.

The input referred noise voltage can be obtain by dividing the output referred noise voltage by $|H_1|^2$.

$$S_{in}(f) = S_{out}(f)/|H_1|^2 \tag{3.10}$$

This gives the answer

$$S_{in}(f) = \frac{8kT}{3}\frac{g_{ds2}}{g_{m1}}\left(1+\frac{g_{ds1}}{g_{m1}g_{m2}}^2\right) \tag{3.11}$$

c) Propose one way to increase the maximum signal to noise ratio, SNR in the circuit. What will happen to the DC-gain, unity-gain frequency, bandwidth and the phase margin of the circuit?

The gain, p1, p2, wu of the circuit are already derived. Assume that the input voltage source is white.

$$V_{in}^2 = S_{in}(f) = \frac{2kT}{3}\frac{1}{g_{m1}}\left(1+\frac{g_{ds1}^2}{g_{m1}g_{m2}}\right)\frac{g_{ds2}}{C_L}$$

$$\propto \frac{2kT}{3}\frac{g_{ds2}}{g_{m1}}\frac{1}{C_L}\left(1+\frac{g_{ds1}^2}{g_{m1}g_{m2}}\right)$$

$$\propto \frac{I_2}{L_2}\sqrt{\frac{L_1}{W_1 I_1}}\left(1+\frac{I_1^2}{L_1^2}\sqrt{\frac{L_1 L_2 I_1 I_2}{W_1 W_2}}\right)$$

$$A_0 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}} \propto \sqrt{\frac{W_1 L_1 W_2 L_2}{I_{bias1} I_{bias2}}}$$

$$p1 = \frac{g_{ds2}}{C_L} \propto \frac{I_2}{L_2 C_L}$$

$$p_2 \approx \frac{g_{ds1}}{C_{gs2}} \propto \frac{I_1}{W_2 L_1 L_2}$$

$$\omega_u \approx A_0 p_1 = \frac{g_{m1} g_{m2}}{g_{ds1} C_L} \propto \sqrt{\frac{W_1 L_1 W_2 I_{bias2}}{L_2 I_{bias1} C_L}}$$

The above five equations shows that will happen if a parameter is changed. Remember that

$$1 \gg \frac{g_{ds1}}{g_{m1} g_{m2}}^2$$

**Table 2: A change in the parameters**

| Change | noise | A0 | p1 | unity-gain | phase margin |
|---|---|---|---|---|---|
| Increase W1 | decreases | Increases | - | increases | decreases |
| increase I1 | decreases | decreases | - | decreases | increases |
| Increase W2 | decreases | increases | - | increases | decreases |
| decrease I2 | decreases | increases | decreases | decreases | increases |

## 4. Switched capacitor circuits

Assume that the operational amplifier is ideal except that it has an input offset voltage.

a) Find the transfer function form $V_1$ to $V_2$ in Figure 4.1.

See exercise 4e)

b) Is the circuit insensitive to parasitics?

Yes it is insensitive to parasitics.

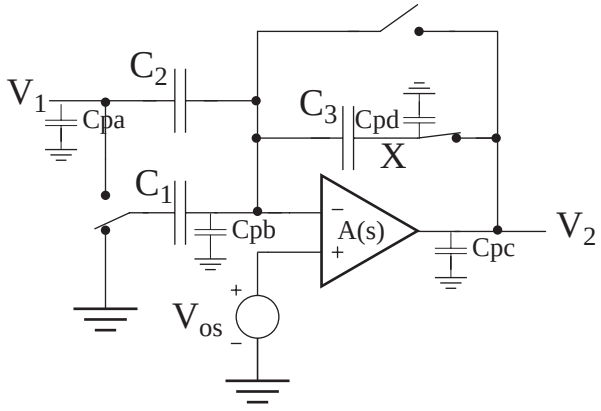
Parasitics:

$C_{pa}$ are connected to an ideal voltage source is will not be affected.

$C_{pb}$ are connected between ground and virtual ground so it will not be affected.

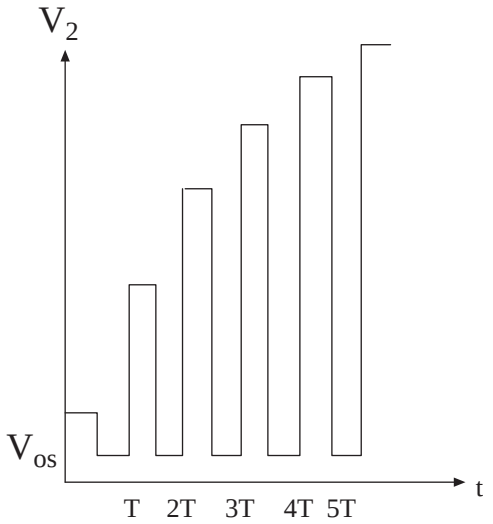
$C_{pc}$ are connected to the output of the ideal OTA, so it will not be affected.

$C_{pd}$ are either connected to the output of the OTA or it will not affect the transfer function.




c) Sketch (sw. skissera) a typical output voltage, $V_2$, over 5 clock periods. Assume a DC-input voltage.

The output from the SC-circuit. Every other output (T/2) will be $V_{os}$.




d) What will be the impact of the circuit if a capacitor is connected between

node X and ground?

The circuit is insensitive to parasitics so the transfer function will not change. The speed of the circuit will decrease since a larger load are applied to the output of the amplifier.

Assume that the operational amplifier ideal except for a finite-gain, A, and an input offset voltage.

e) What is the transfer function? (3p)

Assume that at time t the circuit is in the state as shown in Figure 4.1.

During time t, t+2$\tau$, t+4$\tau$ and so on, vi see that

$$V_2(t + 2n\tau) = (V_{off} - V_x)A \tag{4.1}$$

$$V_2(t + (2n + 1)\tau) = (V_{off} - V_2(t + (2n + 1)\tau))A \tag{4.2}$$

Eq. (4.1) give

$$V_x = V_{off} - \frac{V_2(t + 2n\tau)}{A} \tag{4.3}$$

Eq. (4.2) give

$$V_x = \frac{V_{off}}{1 + \frac{1}{A}} \tag{4.4}$$

Use charge analysis

During time t:

$$q_1(t) = C_1\left(0 - V_{off} + \frac{V_2(t)}{A}\right)$$

$$q_2(t) = C_2\left(V_1(t) - V_{off} + \frac{V_2(t)}{A}\right)$$

$$q_3(t) = C_3\left(V_2(t) - V_{off} + \frac{V_2(t)}{A}\right)$$

During time t+$\tau$:

$$q_1(t+\tau) = C_1\left(V_1(t+\tau) - \frac{V_{off}}{1+\frac{1}{A}}\right)$$

$$q_2(t+\tau) = C_2\left(V_1(t+\tau) - \frac{V_{off}}{1+\frac{1}{A}}\right)$$

$$q_3(t+\tau) = q_3(t)$$

The charge across capacitor 3 is constant from time t to t+$\tau$ since it is not connected anywhere.
During time t+2$\tau$:

$$q_1(t) = C_1\left(0 - V_{off} + \frac{V_2(t+2\tau)}{A}\right)$$

$$q_2(t) = C_2\left(V_1(t) - V_{off} + \frac{V_2(t+2\tau)}{A}\right)$$

$$q_3(t) = C_3\left(V_2(t) - V_{off} + \frac{V_2(t+2\tau)}{A}\right)$$

Charge conservation:

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau)$$

Inserting the above equations in the charge conservation equation and then a Z-transformation gives the transfer function

$$V_2(z) = \frac{1}{C_3\left(1+\frac{1}{A}\right) + \frac{C_1+C_2}{A}} \frac{(C_1+C_2)z^{\frac{1}{2}} - C_2 z + V_{off}\frac{C_1+C_2}{1+A}}{z - \frac{C_3\left(1+\frac{1}{A}\right)}{C_3\left(1+\frac{1}{A}\right) + \frac{C_1+C_2}{A}}}$$

The solution for exercise 4a) is achieved by setting $A \to \infty$

$$V_2(z) = \frac{1}{C_3}\frac{(C_1+C_2)z^{\frac{1}{2}} - C_2 z}{z-1}$$

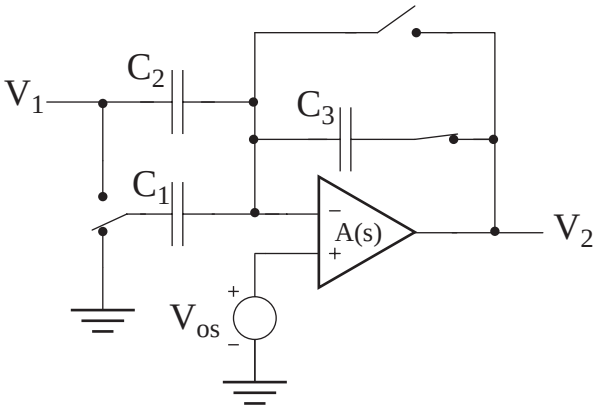



***Figure 4.1*** The switched capacitor circuit.

**5. A mixture of questions**

a) In the course we have discussed matching of transistors. What do we mean by matching? Describe **three** different ways to increase the matching between two transistors.

When we try to make two transistors as equal as possible we call it matching. We can also talk about matching when we try to make two transistors of the same type (i.e. nmos or pmos) to have an exact area ratio.

1) Larger $V_{gs}$ will increase the $V_T$-matching (see lecture 1)

2) Make the transistors larger since the variance of the width and length of the transistor are proportional to the inverse of its area (WL)

3) Use unit size elements and layout them in a symmetric pattern (common centroid or interdigitized)

b) Explain the concept of oversampled analog-to-digital or digital-to-analog converters. What are the advantages and the disadvantages of an oversampled converter compared to a Nyquist-Rate converter?

By using oversampling of the signal $f_s$ » Signal bandwidth the high frequency noise can be attenuated by a low pass filter. Doubling the OSR by 1 increases the accuracy of the converter by 0.5 bits. The accuracy can be further increased by using a delta-sigma modulator that “moves” the noise form the signal band to higher frequencies, where it later on can be attenuated.

+ High accuracy can be achieved

+ A low order, i.e. few bits, converter can be used

- It requires very high sampel rate for a telecommunication application.

c) Describe the function of a common-mode feedback circuit. Explain the function of the circuit in Figure 5.3. How can it be connected to the

operational transconductor amplifier in exercise 2, if it was a fully differential gain stages?

A common-mode feedback circuit will take the mean value of two output voltages and feed the mean back to an amplifier that adjust the DC-level.

$V_{cntrl} = f(V_1 + V_2)$ but not $V_{cntrl} \neq g(V_1 - V_2)$.

If both the input voltage to the circuit below increases then more current will flow in the middle transistors M2 & M3 and thereby the control voltage will increase. A negative feedback amplifier will decrease the input voltage. The opposite action will happen if the input voltage is decreased.

If we increase $V_{inp}$ and decrease $V_{inn}$ there will flow more current through M2 and less through M3 and thereby will the sun be constant. It is working as a common-mode circuit.

The circuit could be connected to the gain stage in the following way.

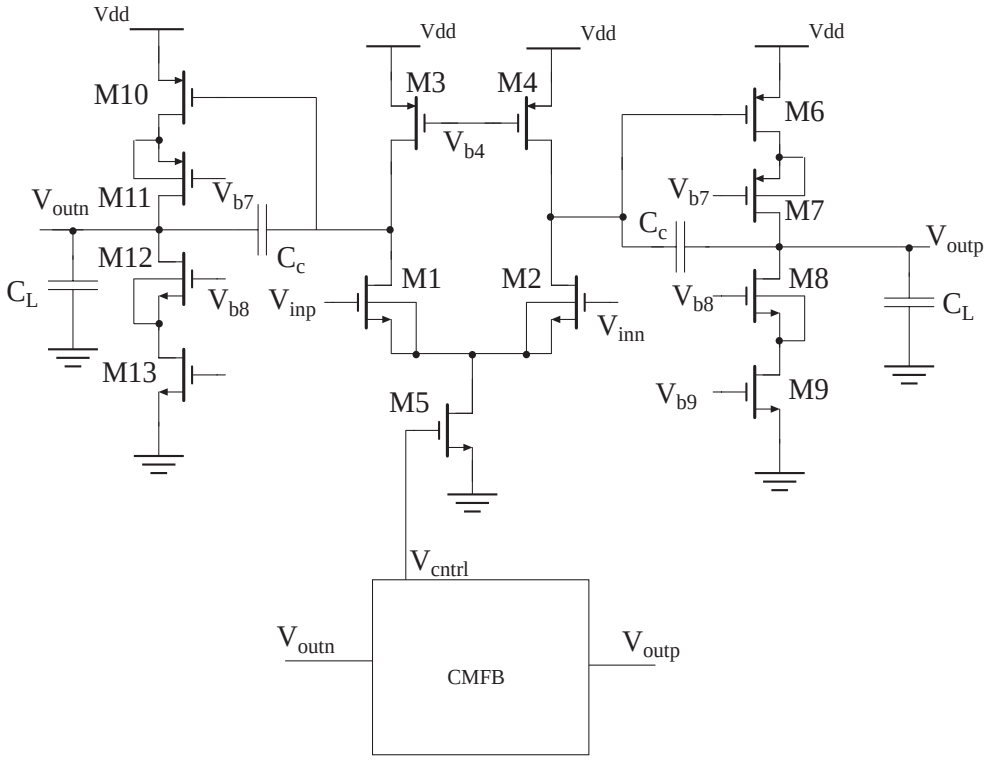



***Figure 5.1*** How to connect a CMFB to a fully differential gain stage.

d) Derive the possible input and output voltages of the circuit in Figure 5.4a. What type of circuit is it?

A too low input and output voltage will set some transistors out of saturation region.

$$V_{out,\,min} = V_{gs2} + V_{ds2} = \sqrt{\frac{I_{out}}{\alpha_2}} + V_{T2} + \sqrt{\frac{I_{out}}{\alpha_4}}$$

$$V_{in,\,min} = max(V_{gs2} + V_{gs4}, V_{ds1} + V_{gs3}) =$$

$$max\left(\sqrt{\frac{I_{out}}{\alpha_2}} + V_{T2} + \sqrt{\frac{I_{out}}{\alpha_4}} + V_{T4}, \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}}\right)$$

It is a current mirror circuit called Wilson current mirror.

e) Derive the power supply rejection ratio, PSRR, from the positive supply of a common source amplifier loaded by an active load, see Figure 5.4b. Propose a way to increase the PSRR.

The PSRR is defined as the gain of the circuit from the input to the output divided by the gain from the supply to the output. We start by finding the ESSS. It is shown in Figure 5.2

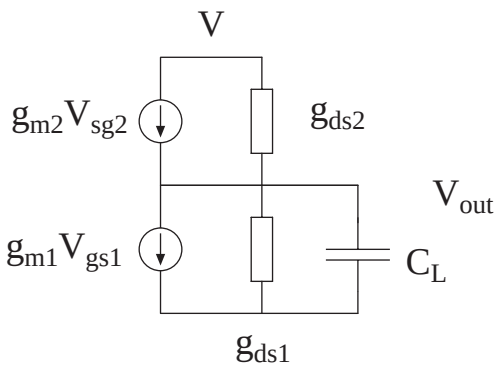



***Figure 5.2*** The ESSS.

The potential V is zero then we like to calculate the gain from the input to the output. It is the supply variations when we like to calculate the gain from the supply to the output.

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L} \tag{5.1}$$

$$\frac{V_{out}}{V} = \frac{g_{m2} + gds2}{g_{ds1} + g_{ds2} + sC_L} \tag{5.2}$$

The PSRR are now calculated to

$$\frac{V}{V_{in}} = PSRR = \frac{g_{m1}}{g_{m2} + g_{ds2}} \approx \frac{g_{m1}}{g_{m2}} \approx \sqrt{\frac{K_1}{K_2}\frac{W_1}{L_1}\frac{L_2}{W_2}} \qquad (5.3)$$

The PSRR are increased by increasing the ratio of the sizes between transistor M1 and M2.

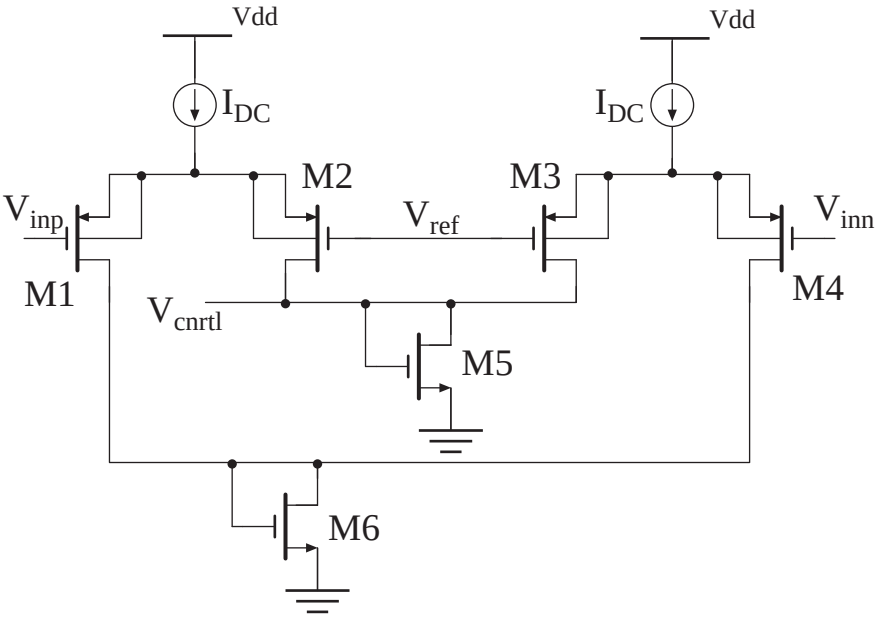



***Figure 5.3*** A common-mode feedback circuit.

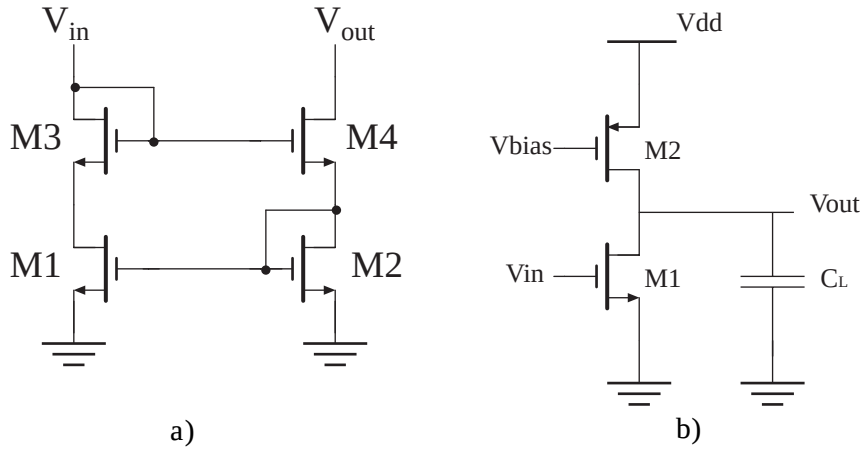



***Figure 5.4*** a) CMOS circuit and b) a common source gain stage.