

Written Test

TSTE80, Analog and Discrete-time Integrated Circuits

Date	January 18, 2000
Time:	9 - 13
Place:	T2
Max. no of points:	100; 80 from written test, 15 for project, and 5 for oral test.
Grades:	36 for 3, 52 for 4, and 68 for 5.
Allowed material:	Tables as "Physics Handbook", "Beta", "TeFyMa", "Digitala Kretsar - Formula", etc., are allowed but no text books as for example Johns & Martin " <i>Analog Integrated Circuit Design</i> ". Pocket calculators are (of course) allowed but no laptops or similar.
Examiner:	Lars Wanhammar.
Responsible teacher:	J. Jacob Wikner. Tel.: 070-591 59 38.
Correct (?) solutions:	Solutions and results will be displayed January 28 in House B, entrance 29, 2nd floor and on the Internet.

Good Luck!

Solutions

a) — The filter specification

Compare with exercise 2.7.

LDI-transformation gives

$$s = s_0 \cdot \frac{z-1}{z^{1/2}}$$

where s_0 is a normalizing constant.
Choose in the reference filter specification that

$$\omega_0 = 2\pi \cdot 1.104 \times 10^6 \text{ rad/s}$$

Derive the normalizing constant as

$$\begin{aligned} s_0 &= \frac{\omega_0}{2 \sin \frac{\Omega_c}{2}} = \\ &= \frac{2\pi \cdot 1.104 \times 10^6}{2 \sin \frac{2\pi \cdot \frac{1.104}{32 \cdot 1.104}}{2}} \approx 35.4 \text{ Mrad/s} \end{aligned}$$

From this we can calculate ω_s as

$$\begin{aligned} \omega_s &= 2s_0 \cdot \sin \frac{\Omega_s}{2} \approx \\ &\approx 2 \cdot 35.4 \cdot \sin \frac{2\pi \cdot \frac{3.093}{32 \cdot 1.104}}{2} \approx \\ &\approx 19.22 \text{ Mrad/s} \end{aligned}$$

which is approximately

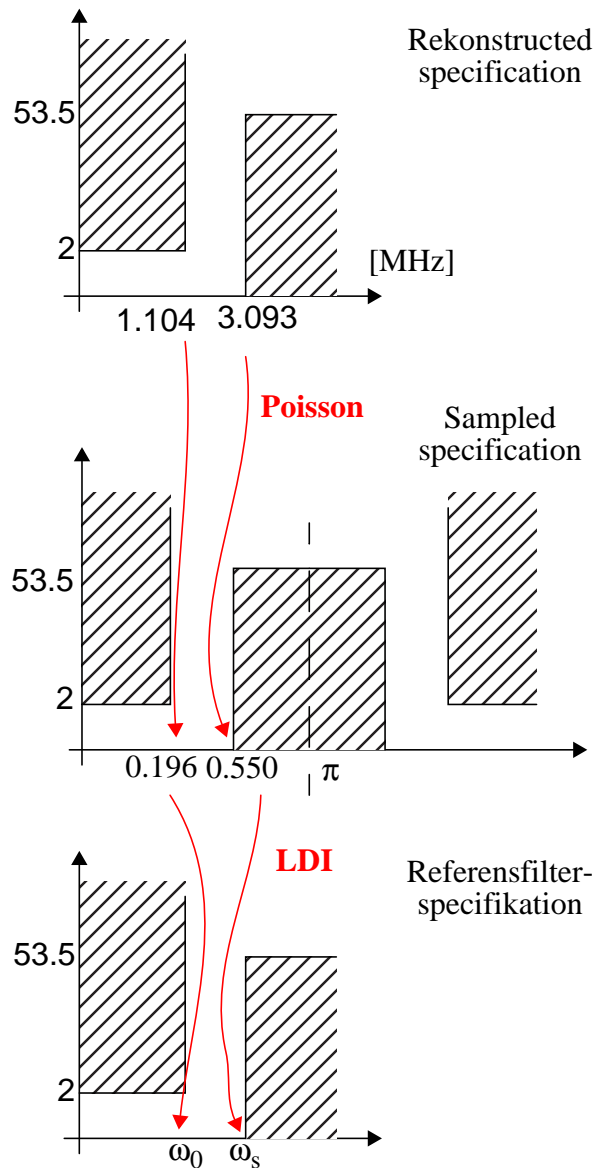
$$3.059 \text{ MHz}$$

(Note the deviation from the specification ...)

Now, we can use the filter tables and we find for equal load and source resistance we get $N = 4$ for the Cauer filter and $N = 7$ for the Butterworth filter. The structure of the ladder networks can be found in the tables and the compendia.

8 points

b) — The transformations

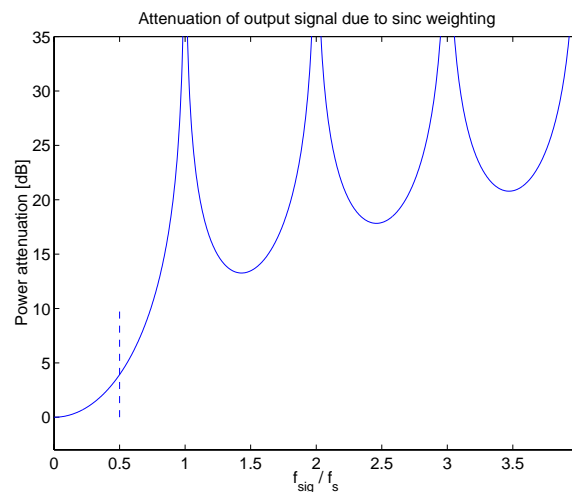


The LDI transform is useful for narrow band filters and the bilinear filter for wide band filters. Using the bilinear transform in an SC filter may have a higher design complexity and overhead than using the LDI transform. The LDI transform is approximate and the bilinear transform is “exact”.

The output signal from the SC filter is piecewise linear due to the sample&hold. This will introduce a so called sinc weighting of the output spectrum. In the frequency domain the output will be attenuated by

$$A(f) = \frac{\pi f / f_s}{\sin(\pi f / f_s)}$$

where f_s is the sampling frequency. For the exercise in a) we have that the attenuation of the output signal at the passband edge is as low as 1.002 or 0.01 dB. However, if the sampling frequency would be lower the sinc attenuation may very well affect the specification and choice of filter.



8 points

c) — The capacitor

I) Use a number of metal plates as a so called sandwich structure. Advantages: simplicity, linearity.

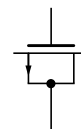
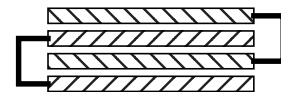
Disadvantages: large chip area, fringing capacitance

II) Use special poly layers or similar for capacitors.

Advantage: linearity. Disadvantages: special process.

III) Use a transistor and the gate-channel capacitance.

Advantage: small chip area. Disadvantage: Nonlinearity



Parasitic capacitance arise for example between ground and the capacitor, particularly from the substrate. Fringing capacitance arises along the edges of the capacitor.

With parasitics we also understand the “unwanted” capacitances associated with the transistor itself, C_{gs} , C_{gd} , etc.

6 points

d) — The filter

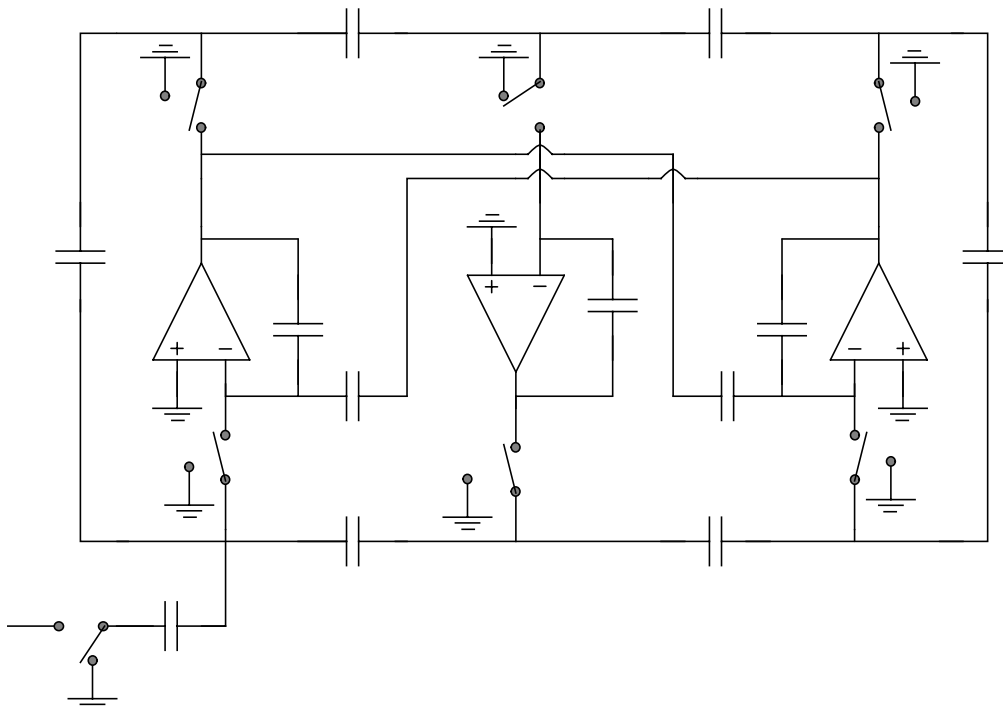
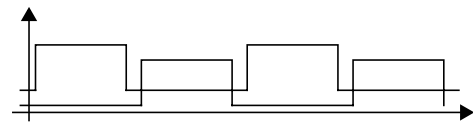
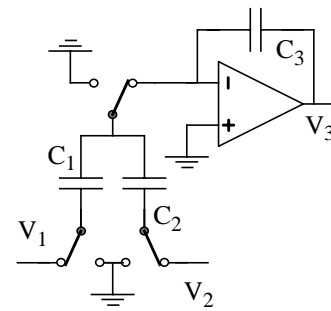
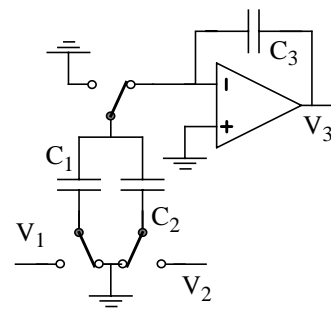
To the right two examples on integrators are shown. The upper is a summing accumulator and the lower is an inverting summing accumulator. Parasitic sensitivity implies that the transfer function of the circuit is dependent on parasitic capacitances in switches, transistors, etc.

The integrators shown in the figure are parasitic insensitive.

The clock phases of an SC circuit should be non-overlapping to prevent unwanted charge sharing.

The component values, hence the capacitors, in the SC filter, should be chosen according to the principle; as many as equally large as possible. For example, choose the integration capacitors for each opamp to be equally large, etc. After that the capacitor sizes are determined by analyzing each signal path through the filter and compare the SC filter with the signal flow graph of the leapfrog filter.

Due to the LDI transform the resistors in the outer branches have to be approximated by a resistance in parallel with a capacitor. This capacitor will eventually end up in parallel with capacitors C_1 and C_3 and they can be taken into account. The resistors are



approximated to be frequency independent, which is a reasonable approximation since a narrow band filter is assumed (see b).

10 points

e) — The switch

Compare with exercise 3.5. Actually, there are different answers to the first parts of this question. CFT is given by the gate-drain (or gate-source) capacitance

$C_{gs} \approx C_{ox} \cdot L \cdot W$ and the load (or sampling capacitance). In the linear region (it is a switch) we have that $C_{gs} = C_{gd}$. The induced voltage on the output node is given by

$$\Delta V_{out} = V_{switch} \cdot \frac{C_{gd}}{C_{gd} + C_1}$$

This induced voltage will however be most characteristic when the transistor is turning from off to on. When the transistor is on we have $V_{in} = V_{out}$. Therefore, the worst case is at the limit, $V_{switch} = V_{in} + V_T$, and we have that

$$\max \Delta V_{out} = (V_{in} + V_T) \cdot \frac{C_{gd}}{C_{gd} + C_1}$$

We find that for large input signal levels we have a high CFT. To minimize the CFT we can reduce the input swing, reduce L and W of the switch transistor or decrease the load capacitance C_L (which may be impossible).

The channel charge is the charge stored under the switch, which actually is what we have discussed above, hence the charge stored by the C_{gs} and C_{gd} . When turning off the transistor, this charge has to go somewhere. Half of the charge is going to the load capacitance and half of the charge is going to the input voltage source.

To reduce the channel charge injection we can use a dummy switch transistor which works in counterphase and with half the size. Then the dummy will absorb half of the channel charge and prevent it from leaking to the load capacitor.

We also have a small induced voltage by the overlap capacitance from C_{ov} .

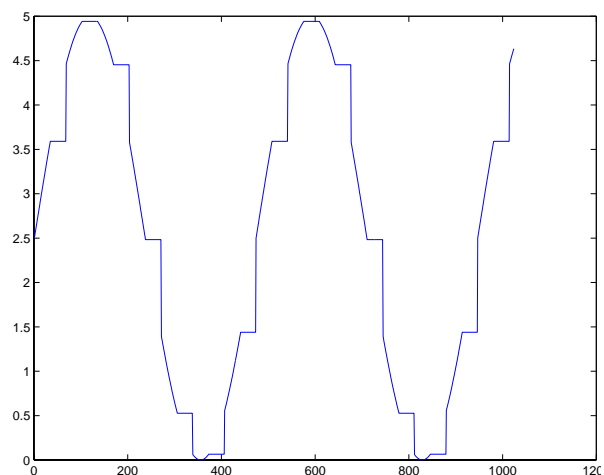
The on-resistance of the switch is found by differentiating the current formula with respect to the drain-source voltage, and we have

$$R_{on} = \frac{1}{\alpha \cdot (V_{switch} - V_T - V_{in})} \propto \frac{1}{V_{switch} - V_T - V_{in}} \cdot \frac{L}{W}$$

Now, we find that we reduce R_{on} by increasing the switch voltage, reducing the input signal level, increasing W , and reducing L .

The CFT (and charge injection) will stay unaffected if we change the switch voltage, it will reduce if we reduce the input signal level, increase if we increase the W , and reduce if we reduce the L . Hence, to achieve low CFT and low on-resistance we try to use low signal levels and a small channel length of the transistor.

The output signal is sketched to the right. The CFT is given by the formulas above at the regions where the switch is turning on. from off.



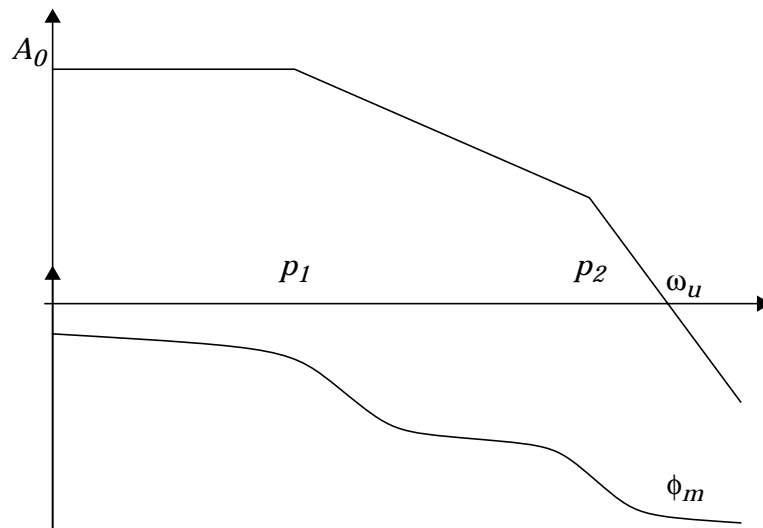
12 points

f) — Active components

The operational amplifier has a zero output impedance and the operational transconductance has an infinite output impedance.

The OTA can be used instead of the OP when there are capacitive loads and no resistive loads.

The transconductor is designed to be linear over a large input voltage range, the OTA does not need to be linear (it must be held in a feedback configuration to become linear).



The SC filter is discrete-time and an image rejection filter is needed at its output. However, the SC filter tend to be very linear. The active-RC is appropriate for intermediate frequency filters of higher filter order and the Gm-C filter for high frequencies. Find out more about this in the filter compendium.

12 points

g) — The operational transconductance amplifier (OTA)

Output impedance is high, the output conductance is given by $g_{out} = g_m/g_{ds}^2$. The bandwidth is given by $p_1 = g_{out}/C_L$ and hence very low, the gain is also high, it is given by $A_0 = g_m^2/g_{ds}^2$.

- M12, M3, M4, M13, M5 are used for biasing of the OTA.
- M8-M11 are the active load for the OTA forming a wideswing mirror.
- M1 and M2 are the input driving transistors
- M6 and M7 are the transistors increasing the output impedance.
- (Assume that the mirror rates are 1 for all mirrors in the OTA).

The currents through the branches should be carefully sized.

Johns&Martin suggest

$$I_{bias2} \approx \frac{8}{5} \cdot I_{bias1}$$

as a design goal. However, it is obvious that $I_{bias2}/2$ has to be less than I_{bias1} due to the current subtractions at the drain of M3 and M4. The currents floating into the sources of M6 and M7 can/must be low for high gain.

The slew rate is given by

$$SR = \frac{I_{bias1}}{C_L}$$

which implies that the bias currents have to be large and relatively equally large to form the “small” current through the cascode transistors.

The dominant pole is determined by the load capacitance and the output conductance. The output conductance is given by the transistors M4 M7 M9 M11, we have that the output conductance is given by

$$g_{out} \approx \frac{g_{ds4} \cdot g_{ds7}}{g_{m7}} + \frac{g_{ds9} \cdot g_{ds11}}{g_{m9}}$$

It is the g_{m7} and the capacitors associated with M4 and M7 that determine the non-dominant pole.

When increasing the output impedance we also increase the gain and we should use this knowledge. to solve the question. We know that

$$A_0 = \frac{g_{m1}}{g_{out}} = \frac{g_{m1}}{\frac{g_{ds4} \cdot g_{ds7}}{g_{m7}} + \frac{g_{ds9} \cdot g_{ds11}}{g_{m9}}}$$

Very roughly, this is approximately

$$\frac{\sqrt{\frac{W_1}{L_1}} \cdot \sqrt{I_{bias2}}}{\left(\frac{I_{bias1}}{L_4 \cdot \sqrt{W_7} \cdot L_7} + \frac{\Delta I_{bias}}{L_{11} \cdot \sqrt{W_9} \cdot L_9} \right) \cdot \sqrt{\Delta I_{bias}}}$$

where

$$\Delta I_{bias} = I_{bias1} - \frac{I_{bias2}}{2} \text{ and } \lambda_i \propto \frac{1}{L_i} \cdot I_i \text{ and } g_m \propto \sqrt{\frac{W}{L}} \cdot \sqrt{I}$$

Three approaches to increase the output impedance:

- Reduce the ΔI_{bias} . To small current may be hazardous since the voltage swing will be reduced.
- Increase the gains in M9 and M7 by making them larger. This will increase the parasitic capacitances and chip area.
- Add further cascodes or gain-boosting to increase output impedance. It will however reduce the voltage swing.

To increase the gain, we can increase the output impedance with the three methods above. Otherwise

- Increase the size of the input transistors. Larger capacitance and chip area.
- Increase the bias current through the transistors. This will increase the power dissipation.

14 points

h) — Noise

We have three noisy components, the two transistors and the resistor.

Reasonable approximations? Assume that only thermal noise dominates and that the resistor noise can be neglected. We also know that it is a common-gate stage, therefore the gain from the input transistor to the output is unity (source-follower). Also assume that the bulk effects can be neglected.

Since it is a source follower it is very simple to find the equivalent noise at the input for M1. The transfer function when also using the effect of C_L is

$$V_{out} = \frac{V_{in}}{1 + \frac{s}{g_{m1}/C_L}} = \frac{V_{in}}{1 + s/p_1} \text{ where } p_1 \text{ is the dominant pole.}$$

For M2 we have to be careful. We have to find the transfer function from the gate of M2 to the output. Use superposition and we have the formulas

$$\begin{aligned} (g_{m1} + g_{ds1} + sC_L) \cdot (0 - V_{out}) + g_{ds2} \cdot (V_x - V_{out}) - g_{m2} \cdot (V_{g2} - V_x) &= 0 \\ g_{m2} \cdot (V_{g2} - V_x) + g_{ds2} \cdot (V_{out} - V_x) + G_L \cdot (0 - V_x) &= 0 \end{aligned}$$

We have that

$$V_x = \frac{g_{m2} \cdot V_{g2}}{g_{m2} + g_{ds2} + G_L} + \frac{g_{ds2} \cdot V_{out}}{g_{m2} + g_{ds2} + G_L} \approx \frac{g_{m2} \cdot V_{g2}}{g_{m2} + G_L} + \frac{g_{ds2} \cdot V_{out}}{g_{m2} + G_L}$$

and

$$V_{out} = \frac{(g_{m2} + g_{ds2}) \cdot V_x}{g_{m1} + g_{ds1} + g_{ds2} + sC_L} - \frac{g_{m2} \cdot V_{g2}}{g_{m1} + g_{ds1} + g_{ds2} + sC_L} \approx \frac{g_{m2} \cdot V_x}{g_{m1} + sC_L} - \frac{g_{m2} \cdot V_{g2}}{g_{m1} + sC_L}$$

This gives approximately

$$V_{out} \approx \frac{g_{m2} \cdot G_L}{(g_{m2} + G_L) \cdot g_{m1}} \cdot \frac{1}{1 + s/p_1} \cdot V_{g2}$$

Now, we can use the super formula and add the noise sources to the output:

$$S_{out}(f) = |H_1(f)|^2 \cdot S_1(f) + |H_2(f)|^2 \cdot S_2(f)$$

We want to find which amount of noise at the input transistor that would yield this noise at the output when transistor 2 is noiseless. Hence

$$S_{out}(f) = \left(S_1(f) + \frac{|H_2(f)|^2}{|H_1(f)|^2} \cdot S_2(f) \right) \cdot |H_1(f)|^2$$

This yields that the spectral density of the equivalent noise source at the input should be

$$S_{eq}(f) = \frac{8kT}{3} \cdot \frac{1}{g_{m1}} + \frac{8kT}{3} \cdot \frac{1}{g_{m2}} \cdot \left(\frac{g_{m2} \cdot G_L}{(g_{m2} + G_L) \cdot g_{m1}} \right)^2$$

This is

$$S_{eq}(f) = \frac{8kT}{3} \cdot \left(1 + \frac{g_{m2} \cdot G_L^2}{(g_{m2} + G_L)^2 \cdot g_{m1}} \right) \cdot \frac{1}{g_{m1}}$$

or

$$S_{eq}(f) = \frac{8kT}{3} \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m2}/g_{m1}}{(1 + g_{m2} \cdot R_L)^2} \right)$$

Assume that R_L and C_L are fixed and the parameters to change are g_{m2} and g_{m1} . Roughly (and inaccurate), we have that we can reduce the equivalent noise at the input by increasing g_{m1} to its double. This is done by increasing its aspect ratio 4 times or the current floating through it 4 times. If we increase the current we will also affect the g_{m2} .

The total noise power at the output is easily found by using the fact that the transfer function at DC is unity and we can use the noise bandwidth factor $p_1/4$ to simplify the integral. Hence

$$P_{tot} = \frac{8kT}{3} \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m2}/g_{m1}}{(1 + g_{m2} \cdot R_L)^2} \right) \cdot \frac{g_{m1}/C_L}{4} = \frac{2}{3} \cdot \frac{kT}{C_L} \cdot \left(1 + \frac{g_{m2}/g_{m1}}{(1 + g_{m2} \cdot R_L)^2} \right)$$

The same considerations to decrease the noise power at the output as for the equivalent noise at the input can be made.

10 points