Written Test

Solutions

TSTE80, Analog and Discrete-time Integrated Circuits

Date	August 20, 1999
Max. no of points:	100; 80 from written test, 15 for project, and 5 for oral test.
Grades:	36 for 3, 52 for 4, and 68 for 5.
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Good Luck!

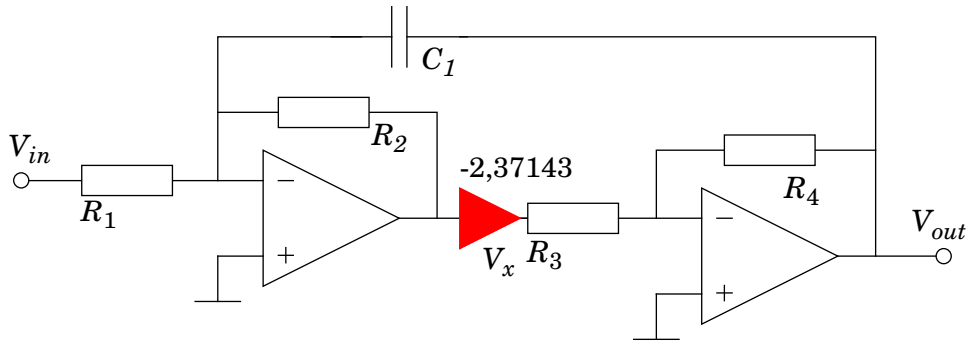
Solutions

1. Continuous-Time Filters.

The filter is scaled for two reasons; 1) we want to avoid to large amplitude levels at the inputs/outputs of the amplifiers, otherwise distortion is introduced; and 2) we also want to avoid to low amplitude levels since then the signal-to-noise ratio (SNR) becomes to low. Usually we adjust the parameters so that

$$\max|H_i(s)| = 1 \text{ for all } i$$

where $H_i(s)$ is the transfer function from the input to an output node, V_i, of an operational amplier. To find the scaling factors of the filter below, we first derive the



transfer functions:

$$V_x = -A\cdot\left(-\frac{R_2}{R_1}\cdot V_{in} - R_2 sC_1\cdot V_{out}\right) \text{ where } A = 2.37143\text{, and } V_{out} = -\frac{R_4}{R_3}\cdot V_x$$

We have that

$$V_x = A\cdot\left(\frac{R_2}{R_1}\cdot V_{in} - R_2 sC_1\frac{R_4}{R_3}\cdot V_x\right) \text{ and } V_x\cdot\left(1 + AR_2 sC_1\frac{R_4}{R_3}\right) = A\frac{R_2}{R_1}\cdot V_{in} \text{ yields}$$

$$V_x = \frac{AR_2/R_1}{1 + AR_2 sC_1R_4/R_3}\cdot V_{in}.\ H_x(s) = \frac{AR_2/R_1}{1 + AR_2 sC_1R_4/R_3}$$

Further we have

$$V_{out} = \frac{-AR_2R_4/R_1R_3}{1 + AR_2 sC_1R_4/R_3}\cdot V_{in}.\ H_{out}(s) = \frac{-AR_2R_4/R_1R_3}{1 + AR_2 sC_1R_4/R_3}$$

The maximum values of both cases, $\max|H_x|$ and $\max|H_{out}|$, are found at $s = 0$ (Low pass filter). The scaling should (could) be done so that the maximum value is equal to one, $\max|H_i| = 1$. Then we should have that

$$AR_2/R_1 = 1 \text{ and } AR_2R_4/R_1R_3 = 1$$

In the unscaled case, we have that

$\max|H_x| = AR_2/R_1 = 4.74286$ and $\max|H_{out}| = AR_2R_4/R_1R_3 \approx 6.323813$

First, observe that by scaling we must absolutely not change the locations of the poles. Therefore, we see that in the simplest case we change the value of R_1 to become larger, and we have $R_1' = R_1 \cdot 4.74286 = 4.74286$. This gives the second expression to become

$$AR_2R_4/R_1'R_3 = R_4/R_3 \approx 1.3333$$

Now we see that if we would change one of the R_3 or R_4 the pole's location would also change. We can however use the capacitance to adjust this change. Let $R_4' = R_3 = 3$ and adjust $C_1' = 1.33333 \cdot C_1 = 1.33333$.

5 points

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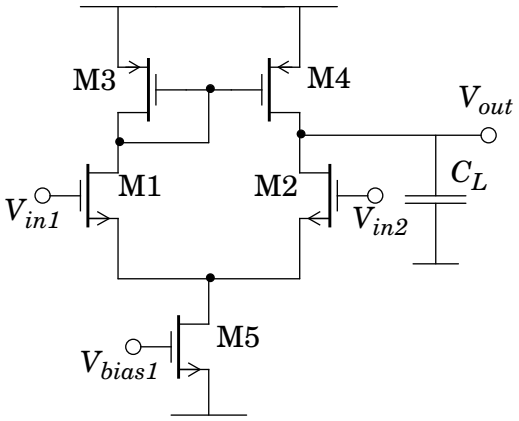
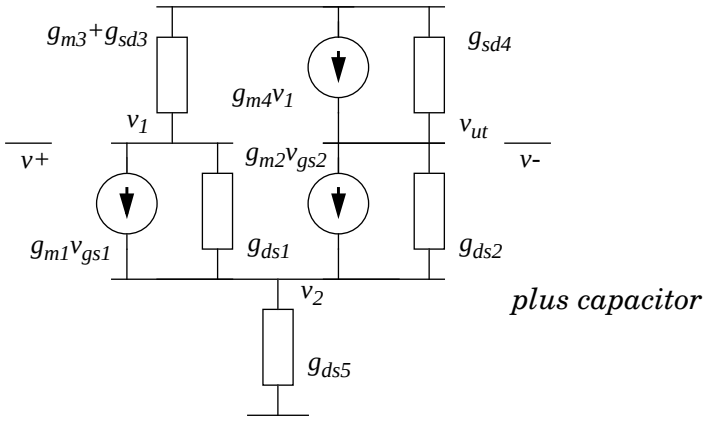
2. CMOS Circuit and Noise.

a) The transistors M1-M5 in the figure below have the different operations; M1 and



M2 are amplifying input transistors, M3 and M4 are the current mirror and function as load to M1-M2 (basically a common-source stage), and M5 is the biasing transistor feeding the circuit with a bias current.

b) The small signal schematic is given in the figure below, where no approximation



have been done. The appropriate approximations would be $g_{m3} + g_{ds3} \approx g_{m3}$ and $g_{ds5} \approx 0$. This should also be motivated. Note! Don't forget the bulk-source connections. Now, we assume that they can be neglected.

c) It can be seen that the gain from input to output is given by (using the approximations and including the capacitance from above):

$$A(s) \approx \frac{g_{m1}/(g_{ds2}+g_{ds4})}{1+\dfrac{s}{(g_{ds2}+g_{ds4})/C_L}}$$

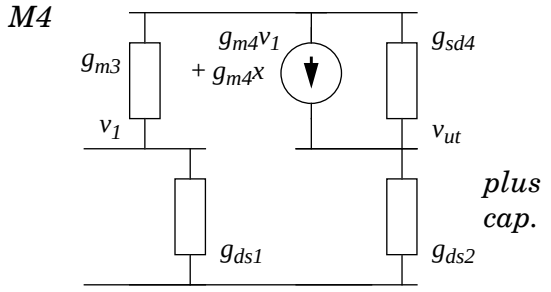
Hence the output conductance is $g_{out} = g_{ds2} + g_{ds4}$, the dominating pole (bandwidth) is $p_1 = (g_{ds2} + g_{ds4})/C_L$ and the unity-gain frequency is $\omega_u = g_{m2}/C_L$.
So to increase the dc gain by a factor of two, we have two choices:

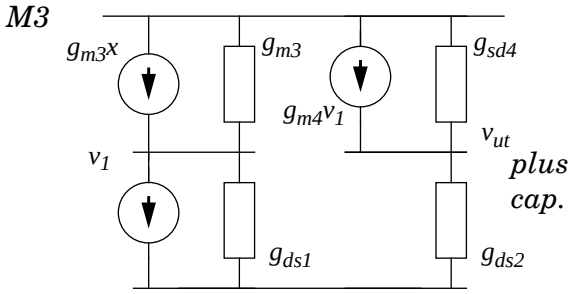
1) **Increase** $g_{m1} \approx \sqrt{2\mu_0 C_{ox} \cdot (W/L)_1 \cdot I_D}$ by a factor of two by increasing $(W/L)_1$ by a factor of 4. In this case, the dominant pole is not moved, but the unity-gain frequency is doubled.

2) **Decrease** the drain current by a factor of 4. This *decreases* g_{m1} two times but it also *decreases* g_{dsi} by a factor of 4 and hence the gain is doubled. Now, however, the dominant pole is moved, it becomes four times lower and the unity-gain frequency is reduced by a factor of two.

d) First, telecommunication applications imply high-speed and hence high frequency. Therefore we are actually only interested in the thermal noise. The 1/f noise is not influencing the result to much. The formulas are given in the tables at the end of the exam.

e) First, realize that the noise source on M1 and M2 give the same result at the output, since they have the same transfer function from gate to output (which was derived in c). The contribution from transistors M3 and M4 is easy to calculate. First, we should use the concept of superposition. For the ccase of noise on M4 we have the situation as below. Assume that $g_{ds5} \approx 0$. In the left branch it is obvious that $v_1 = 0$, and the





current source on M4 is given by $g_{m4} \cdot x$ where x is the noise voltage. We have the transfer function,

$$H_4 = \frac{g_{m4}/(g_{ds2}+g_{ds4})}{1+s/p_1}$$

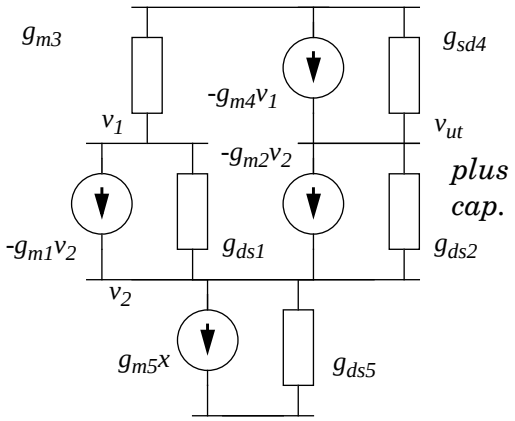
For M3 we have the case as in the figure above. Now we see that the transfer function from x to the output is

$$H_3 = \frac{g_{m4}/(g_{ds2}+g_{ds4})}{1+s/p_1} \cdot \frac{g_{m3}}{g_{m3}+g_{ds1}} \approx \frac{g_{m4}/(g_{ds2}+g_{ds4})}{1+s/p_1} \approx H_4$$

Finally, the noise from the M5 source becomes somewhat trickier.We have the small signal circuit as in the figure below. Using KCL in node v_2 we have that

$$v_1 \cdot g_{m3} \approx v_2 \cdot g_{m1}$$

Considering node v_{out} we have that



$g_{m4} \cdot v_1 - (g_{ds2} + g_{ds4}) \cdot v_{out} + g_{m2} \cdot v_2 \approx 0$ and

$$g_{m4} \cdot v_2 \cdot \frac{g_{m1}}{g_{m3}} - (g_{ds2} + g_{ds4}) \cdot v_{out} + g_{m2} \cdot v_2 \approx 2g_{m2} \cdot v_2 - (g_{ds2} + g_{ds4}) \cdot v_{out} \approx 0$$

Finally, we have

$$-2g_{m2} \cdot v_2 + g_{ds1} \cdot v_1 + g_{ds2} \cdot v_{out} - g_{m5} \cdot x \approx -2g_{m2} \cdot v_2 + g_{ds2} \cdot v_{out} - g_{m5} \cdot x \approx 0$$

and the corresponding transfer function is given by

$$H_5 = \frac{g_{ds4} \cdot g_{m5}}{2 \cdot (sC_L + g_{ds4}) \cdot g_{m4}}$$

Now, using the superfunction, we can find the total noise at the output. We realize that all transfer functions have approximately the same dominant pole. Therefore, the noise bandwidth will be given by $p_1/4$.

$$P_n = \frac{2kT}{3} \cdot p_1 \cdot \left(A_{01}^2 \cdot \frac{1}{g_{m1}} + A_{02}^2 \cdot \frac{1}{g_{m2}} + A_{03}^2 \cdot \frac{1}{g_{m3}} + A_{04}^2 \cdot \frac{1}{g_{m4}} + A_{05}^2 \cdot \frac{1}{g_{m5}} \right)$$

Where A_{0i} is the dc gain of the different transfer functions. From the properties above (thermal noise), we have that

$$P_n \approx \frac{4kT}{3} \cdot p_1 \cdot \left(A_{01}^2 \cdot \frac{1}{g_{m1}} + A_{03}^2 \cdot \frac{1}{g_{m3}} + A_{05}^2 \cdot \frac{1}{2g_{m5}} \right)$$

$$P_n \approx \frac{4kT}{3} \cdot \frac{g_{ds2} + g_{ds4}}{C_L} \cdot \left(\frac{g_{m1}}{(g_{ds2} + g_{ds4})^2} + \frac{g_{m3}}{(g_{ds2} + g_{ds4})^2} + A_{05}^2 \cdot \frac{1}{2g_{m5}} \right)$$

$$P_n \approx \frac{4kT}{3C_L} \cdot \left(\frac{g_{m1} + g_{m3}}{g_{ds2} + g_{ds4}} + A_{05}^2 \cdot \frac{g_{ds2} + g_{ds4}}{2g_{m5}} \right)$$

Note that the pole for

f) When changing the bias voltage the current through the circuit is changed. This influences the g_m and g_{ds} values. According to the formula above we have roughly that

$$P_n \sim \frac{g_{m1} + g_{m3}}{g_{ds2} + g_{ds4}} \sim \frac{1}{\sqrt{I_D}} \sim \frac{1}{V_{bias}}$$

Hence with a larger bias voltage, the noise is reduced. The signal power is however still the same and therefore the SNR is increasing.

g) Mismatch between M1 and M2 influences the common-mode rejection ratio. To guarantee a good matching we have to use special layout techniques as for example interdigitized, common-centroid, etc.

h) The slew rate is found when a step is applied at the input of the amplifier. The slew rate is defined as the maximum possible derivative of the output signal during rise or fall.

35 points

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3. Operational Amplifiers and Transconductances.

a) The ideal operational amplifier is characterized by an infinite input impedance and zero output impedance. The unity-gain frequency should be infinity and the voltage gain as well.

For the common CMOS amplifier the input impedance is infinite, the output impedance is finite, in the order of possibly MΩ.

b) The ideal transconductor has infinite input and output impedance.

c) The Miller effect is characterized by a capacitor between the input and output of the circuit. So basically, the miller integrator uses the miller capacitance to integrate the signal, hence no capacitance between output and ground is needed.

d) The dc gain is A_0. Use the approximation to find the other parameters. It is since previously known that $\omega_u \approx A_0 \cdot p_1$ and the phase margin ϕ_m is approximately $90°$. More advanced case, rewrite the transfer function as

$$\frac{V_{out}(s)}{V_{in}(s)} = H(s) = \frac{A_0}{(1 + s/p_1) \cdot (1 + s/p_2)} = \frac{A_0}{1 + s/p_1 + s/p_2 + s^2/p_1 p_2}$$

Investigate the power spectral density.

$$|H(j\omega)|^2 = \frac{A_0^2}{\left(1 - \frac{\omega^2}{p_1 p_2}\right)^2 + \left(\frac{1}{p_1} + \frac{1}{p_2}\right)^2 \omega^2} = \frac{A_0^2}{1 + \left(\frac{1}{p_1^2} + \frac{1}{p_2^2}\right) \cdot \omega^2 + \frac{\omega^4}{(p_1 p_2)^2}}$$

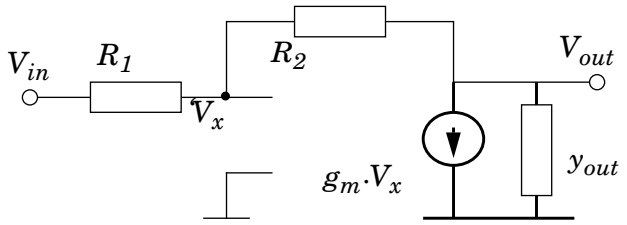
To find the bandwidth and unity-gain frequency, we should solve the equations

$$1 + \left(\frac{1}{p_1^2} + \frac{1}{p_2^2}\right) \cdot \omega^2 + \frac{\omega^4}{(p_1 p_2)^2} = 2 \text{ and } 1 + \left(\frac{1}{p_1^2} + \frac{1}{p_2^2}\right) \cdot \omega^2 + \frac{\omega^4}{(p_1 p_2)^2} = A_0^2$$

or

$$\omega^4 + (p_1^2 + p_2^2) \cdot \omega^2 - (p_1 p_2)^2 = 0 \text{ and } \omega^4 + (p_1^2 + p_2^2) \cdot \omega^2 - A_0^2 \cdot (p_1 p_2)^2 = 0$$

e) One dominant pole in the amplifier implies that we have one dominant capacitor. The output admittance of the amplifier is given by $y_{out} = g_{out} + sC_{out}$ where $p_1 = g_{out}/C_{out}$. Consider the figure below. Use KCL in both nodes:



$$(V_{in} - V_x)\frac{1}{R_1} + (V_{out} - V_x)\frac{1}{R_2} = 0 \text{ and } (V_x - V_{out})\frac{1}{R_2} - g_m V_x + (0 - V_{out})y_{out} = 0$$

$$V_{in}\frac{1}{R_1} = \left[\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \cdot \frac{1/R_2 + y_{out}}{1/R_2 - g_m} - \frac{1}{R_2}\right] V_{out}$$

u.s.w.

15 points

4. Switched-Capacitor Circuits.

a) During clockphase φ_1 we have

$$q_1(t) = C_1 \cdot [V_{in}(t) - V_{out}(t)] \text{ and}$$
$$q_2(t) = C_2 \cdot [V_{in}(t) - V_{out}(t)]$$

NOTE! During this clock phase the opamp is zeroed. Hence the output voltage is grounded (ac ground must not be 0V). Therefore we have that $V_{out}(t) = 0$ and

$$q_1(t) = C_1 \cdot V_{in}(t) \text{ and}$$
$$q_2(t) = C_2 \cdot V_{in}(t)$$

During clockphase φ_2 we have

$$q_1(t + \tau) = C_1 \cdot 0 \text{ and}$$
$$q_2(t + \tau) = C_2 \cdot [V_{out}(t + \tau) - 0]$$

However, during this transition, the charge from C_1 is moved to C_2. Therefore, we have the charge conservation

$$q_2(t + \tau) = q_1(t) + q_2(t)$$

This gives that

$$C_2 \cdot V_{out}(t + \tau) = (C_1 + C_2) \cdot V_{in}(t)$$

The transfer function is given by

$$\frac{V_{out}(z)}{V_{in}(z)} = H(z) = \frac{C_1 + C_2}{C_2} \cdot z^{-1/2}$$

We have that the output signal follows the input signal but with a delay of half a cycle. It is a **gain function**, hence an amplifying **sample&hold** function.

b) Use the same equations from b) but introducing an error. At the first clock phase we have that

$$q_1(t) = C_1 \cdot [V_{in}(t) - V_{out}(t)] \text{ and}$$
$$q_2(t) = C_2 \cdot [V_{in}(t) - V_{out}(t)]$$

NOTE! During this clock phase the opamp is not perfectly zeroed. We have that

$$V_{out}(t) = \frac{A}{1+A} \cdot V_{dc} = B \cdot V_{dc}$$

where V_{dc} is the dc level of the positive input. This gives

$$q_1(t) = C_1 \cdot [V_{in}(t) - B \cdot V_{dc}] \text{ and}$$
$$q_2(t) = C_2 \cdot [V_{in}(t) - B \cdot V_{dc}]$$

During clockphase φ_2 we have

$$q_1(t+\tau) = C_1 \cdot \left[0 - \left(V_{dc} - \frac{1}{A}V_{out}(t+\tau)\right)\right] = C_1 \cdot \left[\frac{1}{A}V_{out}(t+\tau) - V_{dc}\right] \text{ and}$$

$$q_2(t+\tau) = C_2 \cdot \left[\frac{1+A}{A}V_{out}(t+\tau) - V_{dc}\right]$$

However, during this transition, the charge from C_1 is moved to C_2. Therefore, we have the charge conservation

$$q_2(t+\tau) + q_1(t+\tau) = q_1(t) + q_2(t)$$

This gives that

$$C_2 \cdot \left[\frac{1+A}{A} \cdot V_{out}(t+\tau) - V_{dc}\right] + C_1 \cdot \left[\frac{1}{A}V_{out}(t+\tau) - V_{dc}\right] = \ldots$$

$$\ldots = \left(\frac{1+A}{A} \cdot C_2 + \frac{1}{A} \cdot C_1\right) \cdot V_{out}(t+\tau) - V_{dc} \cdot \frac{(1+A) \cdot C_2 + C_1}{A} = \ldots$$

$$\ldots = (C_1 + C_2) \cdot V_{in}(t) - \frac{A}{1+A} \cdot (C_1 + C_2) \cdot V_{dc}$$

$$V_{out}(t+\tau) = \frac{C_1 + C_2}{\frac{1+A}{A} \cdot C_2 + \frac{1}{A} \cdot C_1} \cdot V_{in}(t) - \frac{\frac{A}{1+A} \cdot (C_1 + C_2) - \frac{1 + A \cdot C_2 + C_1}{A}}{\frac{1+A}{A} \cdot C_2 + \frac{1}{A} \cdot C_1} \cdot V_{dc}$$

$$V_{out}(t+\tau) = \frac{C_1 + C_2}{C_2 + \frac{C_1 + C_2}{A}} \cdot V_{in}(t) - \frac{\frac{A}{1+A} \cdot C_1}{C_2 + \frac{C_1 + C_2}{A}} \cdot V_{dc}$$

We now see that the gain error affects the overall gain of the converter. We also see that it affects the true dc voltage at the output. We also see that the magnitude of the error is also dependent on the capacitors C_1 and C_2.

c) Yes the circuit is insensitive to parasitics since all parasitics are connected to a voltage source or/and ac ground.

d) The feedback factor in φ_1 is given by 1 since the output is connected to the input of the operational amplifier. During φ_2 the feedback factor is given by

$$\beta_2 = \frac{C_2}{C_1 + C_2 + C_p}$$

where C_p is the parasitic capacitance at the op amps negative input. During the zeroing phase, φ_1, the feedback factor is $\beta_1 = 1$. Since the bandwidth of the closed system is given by

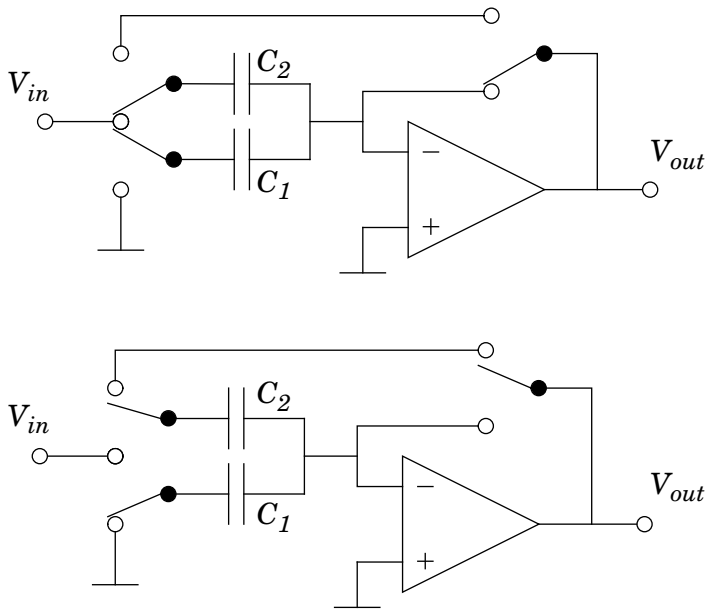
$$\omega_i = \beta_i \cdot \omega_u$$

we see that φ_2 limits the speed, since $\frac{C_2}{C_1 + C_2 + C_p} < 1$.

e) Clock feedthrough is the change of voltage dependent on the capacitive coupling, C_{gs}, C_{gd}, … , between the switching signal and the “analog” signal. Especially, when fast and abrupt changes occur (which is usual) in the switching signal, the CFT is severe.

f) From a we see that a capacitor matching is used to create a gain function (see a). We know from the course that capacitor matching is generally very good.

g) See the answers from the previous exam. LDI - narrow banded filter. Bilinear - wideband filters, but more complex.



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