1. Basic CMOS.

a) The parasitic capacitances that dominate are the C_{gs} and the C_{gd}. Both capacitors are dependent on the size of the transistor, as

$$C_{gs} \sim W \cdot L \text{ and } C_{gd} \sim W \cdot L_{ov}$$

2 points.

b) The transistor will furst be cut-off until the input voltage is larger than the treshold voltage of the transistor: $V_{in} > V_T$. During the cut-off phase the output voltage is high, since no current is going through the resistances. Therefore, when the input voltage is higher than the threshold voltage, the transistor will enter its saturation region. When the input voltage is larger than a certain trip voltage, $V_{in} > V_{trip}$, the transistor enters its linear region. The trip voltage is found when $V_{ds} = V_{gs} - V_T$ of the transistor, hence

$$V_{trip} - V_x - V_T = V_{out} - V_x \Rightarrow V_{trip} = V_{out} + V_T$$

$$V_{out} = V_{dd} - R \cdot I_D \text{ and } V_x = R \cdot I_D$$

$$I_D = \alpha \cdot (V_{trip} - V_x - V_T)^2 = \alpha \cdot (V_{out} - V_x)^2 = \alpha \cdot (V_{dd} - 2RI_D)^2$$

$$I_D = \ldots \text{ which gives } V_{trip} = \ldots$$

3 points.

c) The transconductance goes from low to high to low. Formulas are given at the end of the test.

1 points.

d) The output conductance is basically dependent on the input voltage and not the output voltage. This implies that we get a lower distortion. The transconductance is generally higher as well.

2 points.

2. Basic CMOS Circuits I

a) M1 is a current source. M2 is a cascode transistor, increasing the output impedance and reducing the effect of the Miller capacitance from input to output. It also reduces the voltage swing at the drain of transistor M3 and further reducing the channel length modulation effects (hence increases the linearity). M3 is the amplifying transistor.

3 points.

b) The gain is not influenced by the choise of V_{bias2} (unless it does affect the operation region).

2 points.

c) The gain is dependent on the size of transistor M3 and the bias current. It holds that

$$A_0 \sim \sqrt{W/L} \text{ and } A_0 \sim 1/\sqrt{I_{bias}}$$

We also know that

$$\omega_{-3\text{dB}} = p_1 = g_{ds}/C_L \text{ and } \omega_u = A_0 \cdot p_1 = g_m/C_L$$

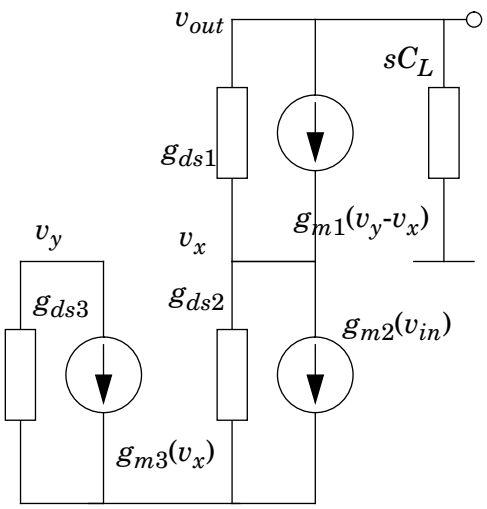
Therefore, to double the gain, we have to either increase the size of M3 by a factor 4, or we can reduce the current by a factor 4. The first case influences the g_m only and therefore the bandwidth is not changed, the unity-gain is doubled. In the second case, the g_m and the output impedance, g_{ds}, are both reduced . Therefore both the band-

width and unity-gain frequency are reduced.

3 points.

3. Basic CMOS Circuits II

Consider the small signal schematics of the circuit. Use nodal voltage approach



$$v_y = -\frac{g_{m3}}{g_{ds3}} \cdot v_x$$

$$(v_{out} - v_x) \cdot g_{ds1} + (0 - v_x) \cdot g_{ds2} + \ldots$$
$$\ldots + g_{m1} \cdot (v_y - v_x) - g_{m2} \cdot v_{in} = 0$$

$$(v_x - v_{out}) \cdot g_{ds1} - g_{m1} \cdot (v_y - v_x) + \ldots$$
$$\ldots + (0 - v_{out}) \cdot sC_L = 0$$

Using these equations, we have that

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m2}(g_{ds1}g_{ds3} + g_{ds3}g_{m1} + g_{m1}g_{m3})}{sC_L(g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m1} + g_{m1}g_{m3}) + g_{ds1}g_{ds2}g_{ds3}} \approx$$

$$\ldots \approx \frac{(g_{m1}/g_{ds1}) \cdot (g_{m2}/g_{ds2}) \cdot (g_{m3}/g_{ds3})}{1 + \dfrac{s}{(g_{ds1} \cdot g_{ds2} \cdot g_{ds3})/(c_L \cdot g_{m1} \cdot g_{m3})}}$$

Hence, we have the dc gain and the dominate pole are

$$A_0 = \frac{g_{m1}}{g_{ds1}} \cdot \frac{g_{m2}}{g_{ds2}} \cdot \frac{g_{m3}}{g_{ds3}} \text{ and } p_1 = \frac{g_{ds1} \cdot g_{ds2} \cdot g_{ds3}}{c_L \cdot g_{m1} \cdot g_{m3}}$$

a) If I_{bias1} is doubled, we have that the gain of M1 and M2 is effected, and they are changed inversly with the square-root of the current, hence the dc gain from input to output is reduced by a factor two.

2 points.

b) Now only the gain of M3 is effected, and the total dc gain is therefore changed by a factor $1/\sqrt{2}$.

2 points.

c) There is no upper bound on the input and output voltages (just the supply). The input voltage has to be higher than the threshold voltage, hence $V_{in} > V_{T2}$. For the output voltage we have to consider the voltage drops over all transistors. First we see that the drain voltage at M2 is equal to the gate voltage at M3. Therefore, we have

$$V_{ds2} = V_{gs3} = V_{eff,2}$$

But to have M3 in proper operation region, we see that $V_{eff,2} > V_{T3}$. The same holds for the gate voltage for M1. This implies that the minimum output voltage has to be

$$V_{out} = V_{T3} + V_{T1} + V_{eff,1}$$

3 points.

d) Regulated cascode or enhanced ouput-impedance circuit configuration.

1 points.

4. Noise.

a) The two most dominating noise sources are the flicker noise and the thermal noise. The flicker noise is inversly proportional to the transistor area, and its power spectral density is inversly dependent on the frequency. Therefore it is dominating at lower frequencies. The thermal noise is dominating at higher frequencies.

3 points.

b) The circuit is a voltage follower with amplification 1. The transconductance is given by g_m and the output resistance is g_m. Therefore the dc gain is $A_0 = g_m/g_m = 1$, the dominating pole is $p_1 = g_m/C_L$. The noise spectral density at the output is given by

$$S_{out}(f) = S_{in}(f) \cdot \frac{1}{1 + |\omega/p_1|^2}$$

Using the concept of noise bandwidth, we find the total noise power at the output:

$$S_{out}(f) = S_{in}(f) \cdot \frac{p_1}{4} = \frac{8kT}{3} \cdot \frac{1}{g_m} \cdot \frac{g_{m1}}{4C_L} = \frac{2kT}{3C_L}$$

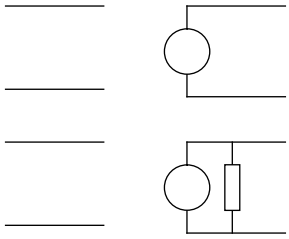
4 points.

c) Not at all according to the result in b).

1 points.

5. Amplifiers and operational amplifiers.

a) The ideal macromodel is simply given by the figure to the right. The input impedance is infinite and the output impedance is zero. The voltage gain is infinite. The common opamp will have as finite output impedance and a finite voltage gain (given by the expression in equation 5.1 in the test).



2 points.

b) $A_0 \cdot p_1 = \omega_u$. The phase margin is given by

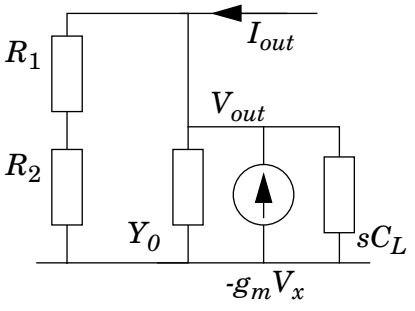
$$-180 - \arg\{H(j\omega_u)\}$$

The phase at the unity-gain is given by

$$-\text{atan}\frac{\omega_u}{p_1} \approx -\text{atan}\,A_0 = -90°$$

2 points.

c) Somewhat tricky question, since the amplifier no longer is ideal. Therefore, we have to consider its output impedance. The output impedance is found when the input signal is grounded. Therefore we have a situation as:



With voltage division, we have that

$$V_x = \frac{R_2}{R_1 + R_2} \cdot V_{out}$$

Nodal analysis gives that

$$I_{out} + \frac{(0 - V_{out})}{R_1 + R_2} + (0 - V_{out}) \cdot (Y_0 + sC_L) + g_m \cdot \frac{-R_2}{R_1 + R_2} \cdot V_{out} = 0$$

$$Y_{out} = \frac{I_{out}}{V_{out}} = \frac{1}{R_1 + R_2} + Y_0 + sC_L + \frac{g_m \cdot R_2}{R_1 + R_2} = \frac{1 + g_m \cdot R_2}{R_1 + R_2} + Y_0 + sC_L$$

$$Y_{out} = \frac{1 + g_m \cdot R_2 + Y_0 \cdot (R_1 + R_2) + sC_L \cdot (R_1 + R_2)}{R_1 + R_2}$$

The output admittance is given by $Y_0 = G_0 + sC_0$, which gives

$$Y_{out} = \frac{1 + g_m \cdot R_2 + G_0 \cdot (R_1 + R_2) + s \cdot (R_1 + R_2) \cdot (C_L + C_0)}{R_1 + R_2}$$

The dominant pole, i.e., bandwidth of the whole system is given by

$$p_{out,\,1} = \frac{1 + g_m \cdot R_2 + G_0 \cdot (R_1 + R_2)}{(R_1 + R_2) \cdot (C_L + C_0)}$$

We also have that $A_0 = g_m/G_0$, $p_1 = G_0/C_0$, and $\omega_u = g_m/C_0$. This gives that we can rewrite the pole as

$$p_{out,\,1} = \frac{\frac{1}{g_m} + R_2 + \frac{R_1 + R_2}{A_0}}{(R_1 + R_2) \cdot (1 + C_L/C_0)} \cdot \omega_u = \ldots$$

$$\ldots = \frac{R_2}{R_1 + R_2} \cdot \omega_u \cdot \left[1 + \frac{1}{A_0}\left(1 + \frac{1}{G_0 \cdot R_2} + \frac{R_1}{R_2}\right)\right] \cdot \frac{1}{1 + \frac{C_L}{C_0}}$$

We see that if the dc gain is high and the load capacitance is zero, we have the well-known formula

$$p_{out,\,1} \approx \beta \cdot \omega_u$$

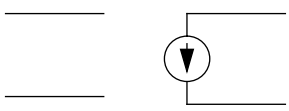
Where β is the feedback factor and ω_u is the unity-gain frequency of the open-loop opamp.

4 points.

6. Transconductance elements.

a) The input and output impedances should both be infinite. The output current is given by

$$I_{out} = G_m \cdot V_{in}$$



1 points.

b) The system function is given by

$$H(s) = A \cdot \frac{s - 0.5}{(s + 0.8) \cdot (s + 0.3)}$$

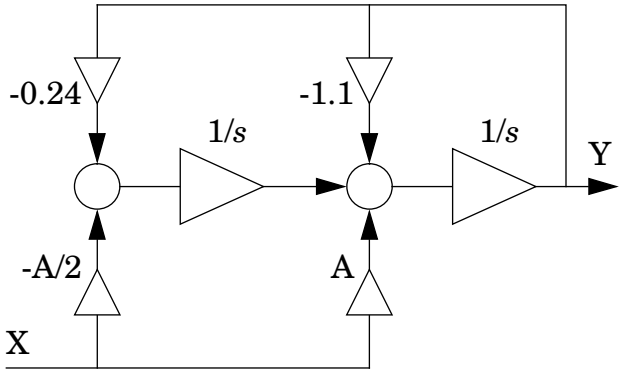
Rewrite the function as

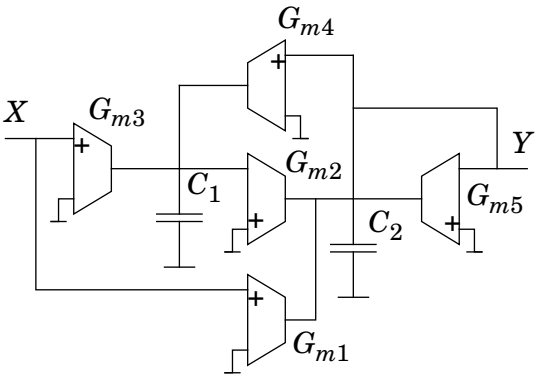
$$Y(s) \cdot [s^2 + 1.1s + 0.24] = X(s) \cdot [As - 0.5A]$$

$$Y(s) \cdot \left[1 + 1.1 \cdot \frac{1}{s} + 0.24 \cdot \frac{1}{s^2}\right] = X(s) \cdot \left[A \cdot \frac{1}{s} - 0.5A \cdot \frac{1}{s^2}\right]$$

$$Y(s) = \frac{1}{s} \cdot \left[A \cdot X(s) - 1.1 \cdot Y(s) - \frac{1}{s} \cdot [0.5A \cdot X(s) + 0.24 \cdot Y(s)]\right]$$

Now we can find the signal flow graph:. From the flow graph the Gm-C implementation is found as:





The component values can be identified by comparing the circuit implementation with the signal flow graph:

$$\frac{G_{m3}}{C_1} \cdot \frac{G_{m2}}{C_2} = \frac{A}{2}, \frac{G_{m4}}{C_1} \cdot \frac{G_{m2}}{C_2} = -0.24, \frac{G_{m1}}{C_2} = A, \frac{G_{m5}}{C_2} = 1.1$$

Choose as many components as equal as possible, e.g., $C_1 = C_2 = C$, etc.

5 points.

c) Either use a capacitance between the outputs or two capacitances connected to ground and each output wire. The first approach reduces capacitor area, but is more sensitive to parasitic capacitors. The second approach is more sensitive to capacitor-capacitor matching.

2 points.

7. Continuous-time Filters.

Sleezy question. It is so much dependent on the application and filter specification. However, as have been indicated, the number of gm-c elements tend to increase rapidly when the complexity of the net is increasing. Therefore, they may use more chip area. More transconductance elements also imply that the power dissipation becomes higher. In most application the Gm-C filter tend to have a worse accuracy (without tuning) at lower frequencies. At higher frequencies the stability of the opamps limits.

Following table tries to conclude these remarks

Specification	Active-RC	Gm-C
Power	Lower	Higher
Chip area	Lower	Higher
Accuracy (without tuning)	Higher	Lower
Speed	Lower	Higher
Complexity	Lower	Higher

3 points.

b) The filter has only one pole. Therefore it has to be a high-pass or low-pass filter. First find the transfer function from the input to the output of both opamp output nodes. Let V_x be the output node at the inverter in the filter. We have that

$$V_x = \frac{R_0}{R_1} \cdot V_{in} + \frac{R_0}{R_2} \cdot V_{out} \text{ and } V_{out} = -\frac{R_4 \parallel sC_2}{R_3} \cdot V_x$$

We see that

$$V_{out} = -\frac{R_4}{R_3 \cdot (1 + sR_4C_2)} \cdot \left[\frac{R_0}{R_1} \cdot V_{in} + \frac{R_0}{R_2} \cdot V_{out}\right], \; V_{out} = \frac{-\frac{R_4 \cdot R_0}{R_1} \cdot V_{in}}{R_3 \cdot (1 + sR_4C_2) + \frac{R_4 \cdot R_0}{R_2}}$$

Use the given values:

$$\frac{V_{out}}{V_{in}} = \frac{-1}{2 + s}$$

We see that the maximum value is found when $s = 0$, i.e., low pass filter. This maximum value is

$$\left\| V_{out} / V_{in} \right\|_{\max} = \frac{1}{2}$$

For V_x we have that

$$V_x = V_{in} - \frac{1}{2 + s} \cdot V_{in} = V_{in} \cdot \frac{2 + s - 1}{2 + s} = V_{in} \cdot \frac{1 + s}{2 + s}$$

Hence a high-pass filter. We see that for low frequencies this expression is $1/2$ and for high frequencies its limit value is 1. Therefore the max value is

$$\left\| V_x / V_{in} \right\|_{\max} = 1$$

and we do not have to scale with respect to V_x.

We have to scale from V_x to V_{out}. This is done by changing R_3, it should have half its value, $R_3 = 1/2$. But we also have to change the size of R_2 to not destroy our transfer function, R_2 should be scaled inversely to R_3, hence $R_2 = 2$.

5 points.

8. Switched-Capacitor Circuits.

a) The derivation is found in the compendium. It is a differencing integrator.

3 points.

b) Backtrack your formulas and you will find an expression as

4 points.

c) It is insensitive to parasitics.

1 points.

9. Switched-Capacitor Filters.

a) LDI is approximate and should be used for narrow-banded filters. The Bilinear transform is exact and can be used for wideband filters. However the impact of sampling frequency vs. signal bandwidth is crucial. See the compendium on page 55, for more information.

2 points.

b) Approach 1, rewrite the function with the system function approach. First rewrite the function as

$$H(z) = \frac{z^{-1}}{0.06z^{-2} - 0.5z^{-1} + 1}$$

The transfer function of the discrete-time integrator is given by

$$A(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Two poles, indicate that we need two integrators. Therefore examine a structure similar to the one in question 6. We find that we can write a general second order transfer function as

$$Y(z) = \frac{z^{-1}}{1 - z^{-1}} \cdot \left[a_1 \cdot X(z) - b_1 \cdot Y(z) + \frac{z^{-1}}{1 - z^{-1}} \cdot [a_2 \cdot X(z) - b_2 \cdot Y(z)] \right]$$

Expanding this expression, we have that

$$Y(z) \cdot (1 - z^{-1})^2 = z^{-1} \cdot (1 - z^{-1}) \cdot [a_1 \cdot X(z) - b_1 \cdot Y(z)] + z^{-2} \cdot [a_2 \cdot X(z) - b_2 \cdot Y(z)]$$

Further, by reordering the terms, we have

$$Y(z) \cdot [1 - 2z^{-1} + z^{-2} + b_1 \cdot z^{-1} \cdot (1 - z^{-1}) + b_2 \cdot z^{-2}] = \ldots$$

$$\ldots = X(z) \cdot [z^{-1} \cdot (1 - z^{-1}) \cdot a_1 + z^{-2} \cdot a_2]$$

$$Y(z) \cdot [1 + z^{-1} \cdot (b_1 - 2) + z^{-2} \cdot (1 - b_1 + b_2)] = X(z) \cdot [z^{-1} \cdot a_1 + z^{-2} \cdot (a_2 - a_1)]$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{z^{-1} \cdot a_1 + z^{-2} \cdot (a_2 - a_1)}{1 + z^{-1} \cdot (b_1 - 2) + z^{-2} \cdot (1 - b_1 + b_2)}$$

Identify the terms by comparing the transfer functions. For the nominator we have $a_1 = 1$, $a_2 = 1$. For the denominator, we have that $b_1 - 2 = 0.5$ which gives $b_1 = 2.5$ and $1 - b_1 + b_2 = 0.06$ which further gives $b_2 = 1.56$.

Implement the filter by using integrators as the one in question 9a.

Approach 2, use biquad building blocks. These are found in " Aktiva och Tidsdiskreta Filter — Tabell- och formelsamling" on page 103-4.

6 points.

10. Data Converters.

a) DNL (differential nonlinearity) describes the difference between the errors from two consecutive codes.

The INL describes the deviation from a straight line when a ramp is applied at the input of the converter.

3 points.

b) Dynamic errors are signal dependent. Static errors are dependent on errors such as component matching, finite impedance, etc.

1 points.

c) The SNR for an oversampling converter is given by

$$\mathrm{SNR} \approx 6N + 1.76 + 10\log \mathrm{OSR}$$

Where OSR is the oversampling ratio. We have that $N = 14$ and $\mathrm{SNR} = 110\,\mathrm{dB}$. This gives that

$$\mathrm{OSR} = 10^{0.1 \cdot (110 - 1.76 - 6 \cdot 14)} \approx 249$$

Without oversampling we have $\mathrm{SNR} \approx 86\,\mathrm{dB}$. To achieve the extra 24dB we need to have a sampling frequency 249 times higher than the signal bandwidth. The choice 256 is often made.

4 points.