# Written Test TSTE80, Analog and Discrete-time Integrated Circuits

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|---|---|
| Date: | August 10, 2006 |
| Time: | 14-18 |
| Place: | TER2 |
| Max.no. of points: | 25 |
| Grades: | 10p for 3, 15p for 4, and 20p for 5. |
| Allowed material: | All types of calcuclators except laptops.<br>All types of official tables and handbooks.<br>Textbooks: Johns & Martin: Analog Integrated Circuit Design.<br>Razavi: Design of Analog CMOS Integrated Circuits.<br>Sedra&Smith: Microelectronic Circuits.<br>Dictionaries. |
| Examiner: | Sune Söderkvist |
| Responsible teacher: | Sune Söderkvist. Tel.: 281355. |
| Corrrect (?) solutions: | Solutions and results will be displayed in House B, entrance 25-27, ground floor. |

**Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00 from week no. 34**

## Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

## For students who has studied earlier variants of the course :

The conditions for the test is the same as before, i.e. every problem gives max. 8 points and you get credits for project and assignments as before. Mark 3 require 30 p totalt, mark 4 require 42 p and mark 5 require 56 p. Please, tell me on the wrapper if this is of interest.

## Good Luck!

## Exercise 1.

The circuit in **Figure 1** is used to establish an appropriate bias voltage $V_{bias}$ to an operational amplifier. The transistors have following parameter values:

| | N-kanal | P-kanal |
|---|---|---|
| $V_{t0}$ [V] | 0.47 | 0.62 |
| $\mu_0 C_{ox}$ [$mu$A/V$^2$] | 180 | 58.5 |
| $\lambda$ [V$^{-1}$] | 0.03 | 0.05 |
| $\gamma$ [V$^{1/2}$] | 0.62 | 0.41 |
| $\phi_F$ [V] | 0.43 | 0.41 |

a) Show that all transistors are saturated in this circuit. (1.5p)

b) Determine $\frac{W}{L}|_i$, $i = 1, 2, 3$, for transistors $Mi$ , $i = 1, 2, 3$, if $V_{DD} = 3.3$ V, $V_{bias} = 0.6$ V and $I_D = 5$ $\mu$ A.

If the potential $V_x$ is just above 2.05 V it shows that $\frac{W}{L}|_2 = \frac{W}{L}|_1$. Choose $V_x = 2.05$ V here.

Do not neglect the bulk effekt neither the channel-length modulation. (3.5p)

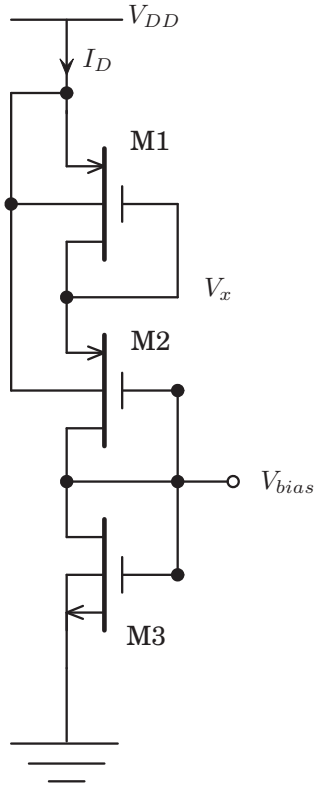


**Figure 1:** A bias circuit.

## Exercise 2.

Sketch a small-signal equivalent circuit and determine the input resistans $r_{in}$ and the output resistans $r_{out}$ for the wide-swing current mirror in **Figure 2**. All transistors are biased to operate in the saturation region. Assume that the transistors small-signal parameters are $g_{m1}$, $g_{ds1}$, $g_{m2}$, $g_{ds2}$ and $g_{m3}$, $g_{ds3}$ respectively. (5p)

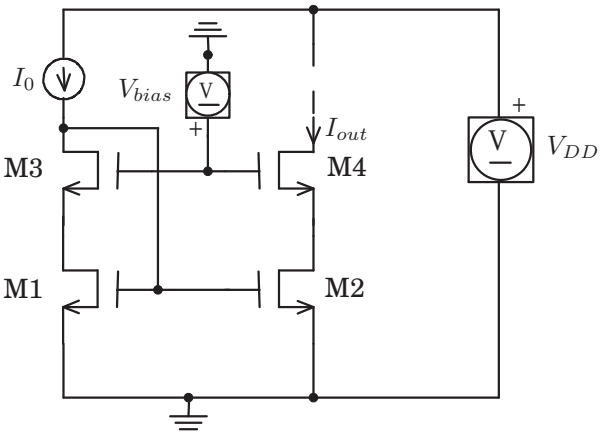


**Figure 2:** A wide swing current mirror.

## Exercise 3.

A switched capacitor circuit in clock phase 1 is shown in **Figure 3**. The value of $V_{in}$ changes only at time $t$, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_{in}(t) = V_{in}(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_{in}(z)$, for clock phase 1. Assume that the operational amplifier is ideal and that $C_3 = 2C_1$. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)

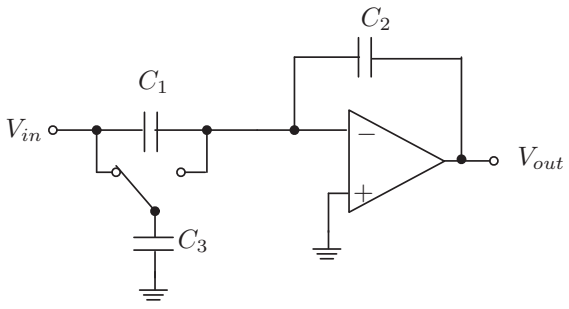


**Figure 3:** A switched-capacitor circuit in clock phase 1.

## Exercise 4.

**Figur 4** shows a simplified small-signal model of an OTA, including a compensation capacitor $C$.

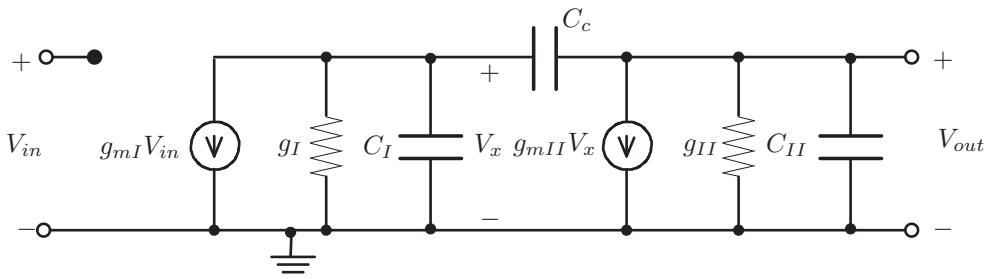


**Figure 4:** A small-signal model of a two-stage OTA.

a) Derive an expression for the transfer function $H(s) = V_{out}/V_{in}$. (3p)

b) Determine an approximation of $H(s)$ assuming that $g_{mII} >> g_I$, $g_{mII} >> g_{II}$, $g_{mII} >> g_I$, and also that $C_c >> C_I$ and $C_{II} >> C_I$. Also assume that $C_{II}$ and $C_c$ is of the same order.

Determine DC gain $A_0$, poles and zeros and also an approximation of unity-gain frequency $\omega_u$, from this approximation assuming that the poles are well separated ($|p_2| >> |p_1|$). (2p)

## Exercise 5.

Consider the two cascaded common-cource stages in **Figure 5**, where only the thermal noise generated in the transistors is of interest. The current sources are ideal and hence noiseless. Let the output load capacitance be given by $C_L$ and parasitic capacitanses are only given by gate-source capacitances, $C_{gs}$. Further $I_{bias1} = I_{bias2} = I_{bias}$. The transistors are identical with the small signal parameters $g_{m1} = g_{m2} = g_m$ and $g_{ds1} = g_{ds2} = g_{ds}$. Both transistors operate in the saturation region.

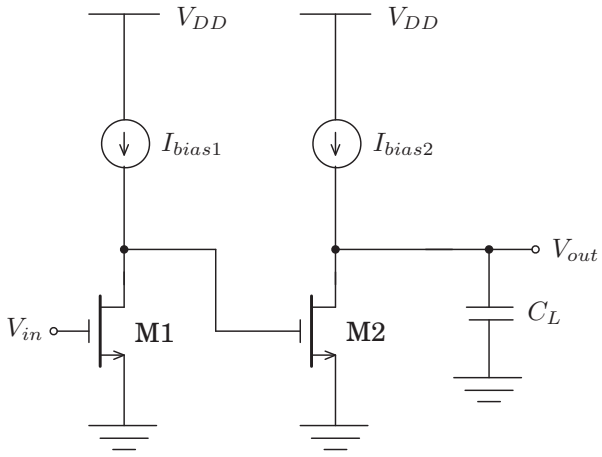


**Figure 5:** A noisy multi-stage amplifier.

a) Determine an expression for the spectral density $R_{out}$ of the output thermal noise assuming that the noise from the transistors are uncorrelated. (2p)

b) Assume that $C_L >> C_{gs}$ and derive an approximation for the total output noise power $P_{out,noise}$ using the noise-bandwidth concept. (Express $P_{out,noise}$ in small signal parameters, in $C_L$ and in constants.) (2p)

c) Express $P_{out,noise}$ in $I_{bias}$ and answer following questions. (Motivate!)
How to change $I_{bias}$ if you want to decreas $P_{out,noise}$?
How will that affect the DC-gain of the circuit? (1p)

# Transistor formulas and noise

## 1 CMOS transistors

**Current and threshold voltage formulas and operating regions for an NMOS transistor**

| | | |
|---|---|---|
| Cut-off: | $V_{GS} < V_{tn}$ | $I_D \approx 0$ |
| Linear: | $0 < V_{DS} < V_{eff}$ | $I_D \approx \alpha(2V_{eff} - V_{DS})V_{DS}$ |
| Saturation: | $V_{DS} > V_{eff}$ | $I_D \approx \alpha V_{eff}^2(1 + \lambda(V_{DS} - V_{eff}))$ |
| All regions: | $V_{tn} = V_{t0n} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$ | |
| | $V_{eff} = V_{GS} - V_{tn}$ | |

**Small-signal parameters**

| | | |
|---|---|---|
| Linear: | $g_m \approx 2\alpha V_{DS}$ | $g_{ds} \approx 2\alpha(V_{GS} - V_{tn} - V_{DS})$ |
| Saturation: | $g_m \approx 2\sqrt{\alpha I_D}$ | $g_{ds} \approx \lambda I_D$ |

**Constants:** $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\lambda = \sqrt{\frac{2K_s\epsilon_0}{qN_A\phi_0}} \cdot \frac{1}{L}$ $\gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

## 2 Circuit noise

**Thermal noise in CMOS transistors**
The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

**Thermal noise in resistors**
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$\frac{\bar{i^2}}{\Delta f} = \frac{4kT}{R}$$

**Flicker noise in CMOS transistors**
The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$