Written Test TSTE80,
Analog and Discrete-time Integrated Circuits

Date:	May 29, 2006
Time:	8-12
Place:	TER1
Max.no. of points:	25
Grades:	10p for 3, 15p for 4, and 20p for 5.
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Dictionaries.
Examiner:	Sune Söderkvist
Responsible teacher:	Sune Söderkvist. Tel.: 281355.
Corrrect (?) solutions:	Solutions and results will be displayed in House B, entrance 25-27, ground floor.

Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00, during week no.23 and 24.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

For students who has studied earlier variants of the course :

The conditions for the test is the same as before, i.e. every problem gives max. 8 points and you get credits for project and assignments as before. Mark 3 require 30 p totalt, mark 4 require 42 p and mark 5 require 56 p. Please, tell me on the wrapper if this is of interest.

Good Luck!

Exercise 1.

The circuit in **Figure 1** is a commonly used structure when designing analog circuits. Transistor M1 is assumed to be biased in saturation. Also assume that the W/L ratio of transistor M2 is K times larger than that of transistor M1. The channel-length modulation can be neglected.

a) Derive the output voltage V_{out} as a function of the factor K, i.e. $V_{out} = f(K)$ when M2 is saturated. Express V_{out} in terms of the current I_0 and transistor design parameters, but not voltages. (1p)

b) Derive the output voltage V_{out} as a function of the factor K, i.e. $V_{out} = f(K)$ when M2 is operating in the linear region. Express V_{out} in terms of the current I_0 and transistor design parameters, but not voltages. (2p)

c) Determine for which values of K transistor M2 switches from operating in the saturation region to the linear region. (2p)

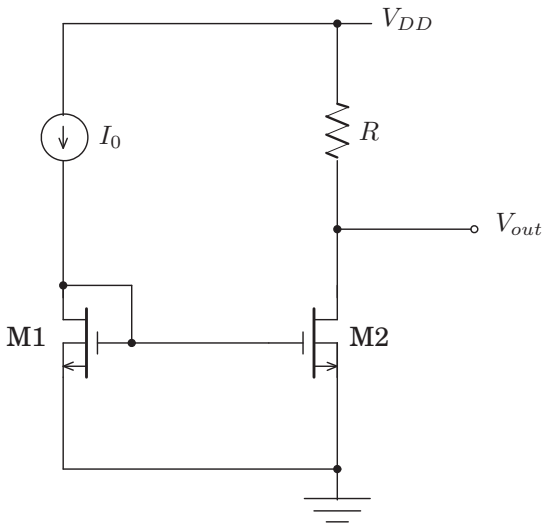

Figure 1: A commonly used analog circuit.

Exercise 2.

Figure 2 shows an gain-boosted folded-cascode amplifier. All transistors are biased to operate in the saturation region. Assume that the transistors small-signal parameters are g_{m1}, g_{mbs1}, g_{ds1}, g_{m2}, g_{mbs2}, g_{ds2} and g_{m3}, g_{mbs3}, g_{ds3} respectively.

a) Sketch a small-signal equivalent circuit and determine an exact expression for the transfer function $H(s) = V_{out}(s)/V_{in}(s)$. The bulk effect can **not** be neglected. However, all capacitors but C_L can be neglected. (3p)

b) Now, neglect the bulk effect and assume that $g_m >> g_{ds}$ to get an approximation of $H(s) = V_{out}(s)/V_{in}(s)$. From this approximative expression, determine the DC gain, the first pole, and the unity-gain frequency. (1p)

c) Express the DC gain in terms of the design parameters W_i, and L_i for the transistors Mi, $i = 1, 2, 3$, and answer (motivate) following questions.

How is the DC gain changed: If the current I_0 is increased? If the channel-length of transistor $M3$ is increased? If the channel-width of transistor $M3$ is increased? Assume that all transistors remain saturated. (1p)

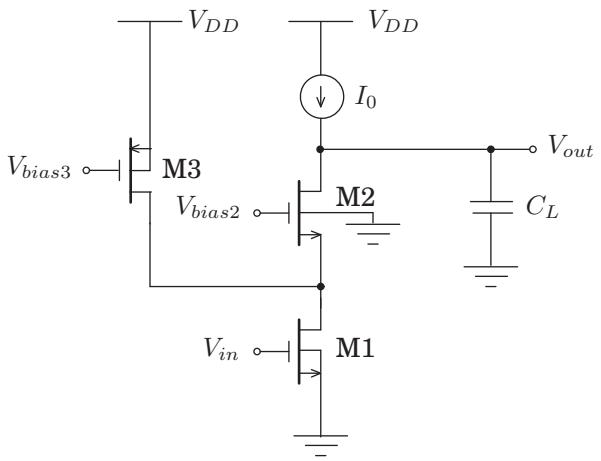

Figure 2: A gain-boosted folded-cascode amplifier.

Exercise 3.

A switched capacitor circuit in clock phase 1 is shown in **figure 3**. The value of V_{in} changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_{in}(t) = V_{in}(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_{in}(z)$, for clock phase 1. Assume that the operational amplifier is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)

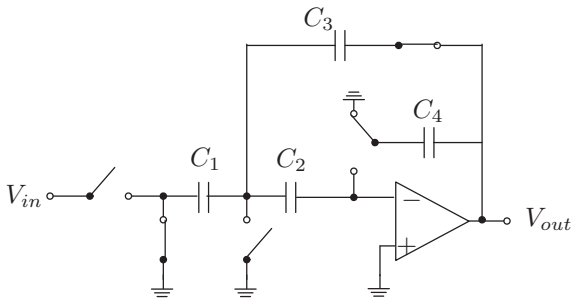

Figure 3: A switched-capacitor circuit in clock phase 1.

Exercise 4.

Figur 4a shows a differential gain-stage with single-ended output, and **Figur 4b** shows a differential gain-stage with fully differential output, where $V_{out} = V_{outp} - V_{outn}$. In the following you can neglect the parasitics and the current source, I_0, is assumed to be ideal. Furthermore, the transistors in the gain-stages are matched, i.e. M2 and M4 are identical, as well as M1 and M3. Also the transistors M01 and M02 in the current mirror are identical.

a) For the gain-stage in **figure 4a**, derive an expression for the transfer function from GND to the output V_{out} and use this expression determine an expression for Power Supply Rejection Ratio (PSRR). Assume that the gain-stage has the gain A_{single}. (2p)

b) Assume that A_{single} can be approximated with $A_{single} \approx \frac{g_{m3}}{g_{ds3}+g_{ds4}}$. Enter that expression in the expression you derived in a) and use this new expression to explain how to change the design of the current mirror to increase PSRR. (1p)

c) Now, regard the gain-stage in **figur 4b** and derive an expression for the transfer function from GND to the differentiell output signal, and use this expression to determine an expression for PSRR if the gain-stage has the gain A_{diff}. (1p)

d) Explain what happens to PSRR in c) if you have mismatch between transistors M2 and M4 as well as between M1 and M3. (1p)

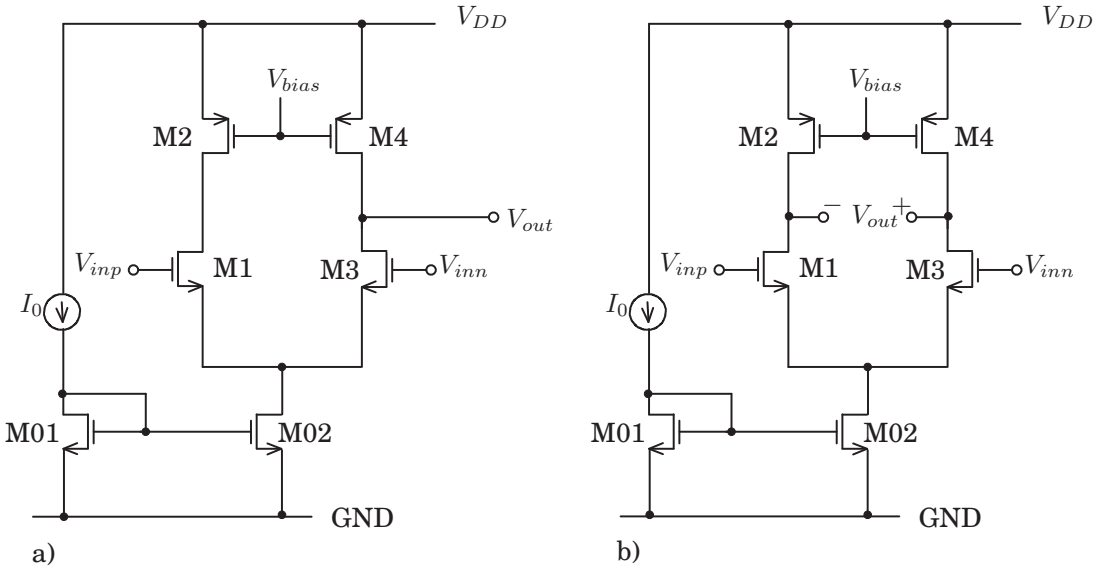

Figure 4: Differentialförstärkare.

Exercise 5.

The inverting amplifier in **Figure 5a** is used in an application where low noise is of major importance. Hence, a low noise design of the amplifier is required. In this exercise, only the thermal noise in the op.amp. is considered. The gain of the op.amp. $A = g_{m1}/g_{out} = g_{m1}/(g_{ds2} + g_{ds4})$. Further, the ratio between R_2 and R_1 is $R_2/R_1 = a$.

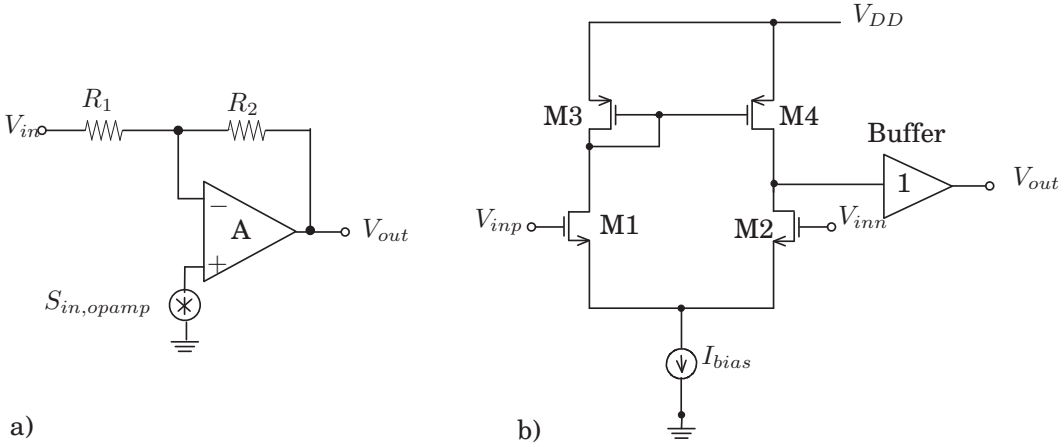

Figure 5: a) A noisy inverting op.amp. b) The principal schematic of the op.amp.

a) Assume that the resistors do not generate any thermal noise while the op.amp. has an equivalent voltage input noise spectral density of

$$S_{in,opamp} = \frac{16kT}{3}\frac{1}{g_{m1}}[1 + \frac{g_{m4}}{g_{m1}}]$$

where the number in the index refers to the op.amp. implementation in **Figure 5b**. Compute the equivalent output noise spectral density for the circuit in **Figure 5a** caused by the noisy amplifier. (4p)

b) State one approach to decrease the equivalent output noise spectral density of the circuit in **Figure 5a** caused by the operational amplifier. How does this impact the DC gain of the open loop amplifier? (1p)

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_T$	$I_D \approx 0$
Linear:	$V_{GS} - V_T > V_{DS} > 0$	$I_D \approx \alpha(2(V_{GS} - V_T) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_T < V_{DS}$	$I_D \approx \alpha(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
All regions:	$V_T = V_{T,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_T - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}$ $\lambda = \sqrt{\frac{2K_s\epsilon_0}{qN_A\phi_0}} \cdot \frac{1}{L}$ $\gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{8kT}{3}\frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$\frac{\bar{i^2}}{\Delta f} = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$