Written Test

TSTE80,
Analog and Discrete-time Integrated Circuits

Date:	January 12, 2006
Time:	8-12
Place:	TER2
Max.no of points:	70; 40 from written test, 15 for project, 15 from assignments
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Dictionaries.
Examiner:	Sune Söderkvist
Responsible teacher:	Sune Söderkvist Tel.: 281355.
Corrrect (?) solutions:	Solutions and results will be displayed in House B, entrance 25-27, ground floor.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

1. Large-signal analysis

For the amplifier in **Figure 1**, $0 \leq V_{in} \leq 1.5$ V and $V_{DD} = 3$ V. The transistors have following parameter values:

	N-channel	P-channel
$V_{T,0}$	0.5 V	0.6 V
$\mu_0 C_{ox}$	20 nA/V^2	6 nA/V^2
λ	0.03 V^{-1}	0.05 V^{-1}
γ	0.5 V$^{1/2}$	0.3 V$^{1/2}$
ϕ_F	0.4 V	0.4 V

a) Let $V_{bias1} = 2.5$ V and $V_{bias2} = 2$ V and determine the output swing, i.e. $V_{out,min}$ and $V_{out,max}$, when both transistors are operating in the saturation region. (3p)

b) Determine W/L for both transistors if their drain currents shall be limited to $I_D \leq 0.1$ μA at the limit of saturation. $V_{bias1} = 2.5$ V and $V_{bias2} = 2$ V. (3p)

c) Determine the limit values of V_{bias1} and V_{bias2} allowing both M1 and M2 to operate in the saturation region, independent of the variations of V_{in}. ($0 \leq V_{in} \leq 1.5$ V) (2p)

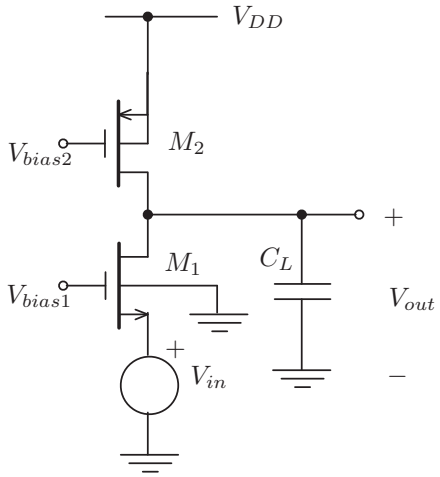

Figure 1: Amplifier.

2. Small-signal analysis

Once again, look at the capacitive-loaded amplifier in **Figure 1**. Assume that the transistors small-signal parameters are g_{m1}, g_{mbs1}, g_{ds1} and g_{m2}, g_{mbs2}, g_{ds2} respectively.

a) Sketch a small-signal equivalent circuit and determine an exact expression for the transfer function $H(s) = V_{out}(s)/V_{in}(s)$. The bulk effect can **not** be neglected. However, all capacitors but C_L can be neglected. Also, determine the DC gain. (4p)

b) Determine an exact expression for the small-signal input impedance, $Z_{in}(s)$. (3p)

c) Determine an exact expression for the small-signal output resistance, r_{out}. (1p)

3. Noise in CMOS circuits

The transistors M1 and M2 in the circuit shown in **Figure 2** generate thermal noise while the biasing voltage V_{b1} and the biasing currents I_{bias1} and I_{bias2} are assumed to be noise less. Both transistors are biased in saturation and are here modeled by the small-signal parameters g_m and g_{ds}.

a) Derive the total output noise spectral density. (5p)

b) Which transistor gives the largest contribution of the generated noise if the input referred noise spectral density is considered? (1p)

c) Propose one approach to increase the maximum signal-to-noise ratio, SNR for the circuit shown in **Figure 2** without changing the input signal power. Which design parameters should be changed to obtain this improvement? (2p)

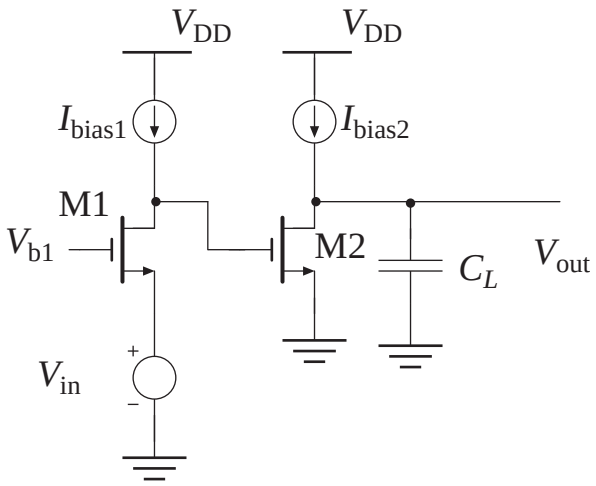

Figure 2: A noisy analog circuit.

4. Switched Capacitor Circuit

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau$, $t + 4\tau$, etc. is shown in **Figure 3**. Assume that the input signal is constant between clock phase 1 and 2, i.e., $V_{in}(t) = V_{in}(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_{in}(z)$, for clock phase 1 of the switched capacitor circuit shown in **Figure 3**. Assume that the operational amplifier is ideal. Motivate your answer carefully. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)

c) Express the output voltage, $V_{\text{out}}(z)$, as a function of the input voltage, $V_{\text{in}}(z)$ and offset voltage, V_{os}, for clock phase 1 of the switched capacitor circuit shown in **Figure 3**. Assume that the OTA suffers from an offset voltage, V_{os}. (3p)

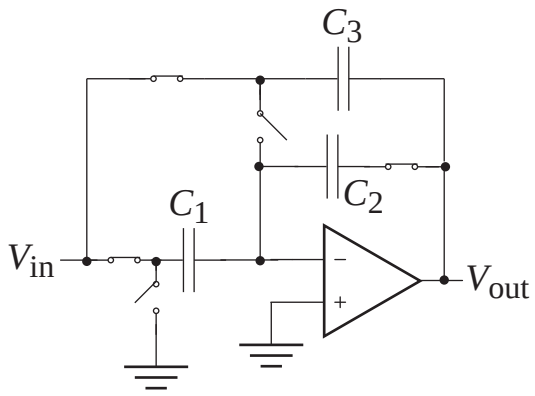

Figure 3: An SC circuit in clock phase 1.

5. A mixture of questions

a) In an active RC filter we need to have an operational amplifier with the following performance

Performance measure	Value
A_0	80 dB
f_u	100 MHz
C_L	5 pF
Slew rate	80 V/μs
Output range	[0.5 - 2.8] V
Common-mode range	[0.1 - 2.0] V
V_{DD}	3.3 V
Power consumption	$\leq$ 10 mW

How would you design the operational amplifier? Draw the block diagram of the operational amplifier and give a specification of each block in your design, like the one above and the name of the type of building block and the type of the input transistors. (3p)

b) The same task as in a) but here we have an operational transconductance amplifier that will be used in an SC filter. (2p)

c) In analog filters tuning circuits are commonly used. Explain why tuning is required in analog circuits. Also, explain the basic principle of tuning in analog active-RC filters. (2p)

d) State benefits and drawbacks with fully differential circuit compared with their single-ended counterpart. (1p)

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_T$	$I_D \approx 0$
Linear:	$V_{GS} - V_T > V_{DS} > 0$	$I_D \approx \frac{\mu_0 C_{ox}}{2} \frac{W}{L}(2(V_{GS} - V_T) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_T < V_{DS}$	$I_D \approx \frac{\mu_0 C_{ox}}{2} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
All regions:	$V_T = V_{T,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx \mu_0 C_{ox} \frac{W}{L} V_{DS}$	$g_{ds} \approx \mu_0 C_{ox} \frac{W}{L}(V_{GS} - V_T - V_{DS})$
Saturation:	$g_m \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D}$	$g_{ds} \approx \lambda I_D$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{8kT}{3}\frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$\frac{\bar{i^2}}{\Delta f} = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\bar{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$