

Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date: May 27, 2004

Time: 8 – 12

Place: T1

Max. no of points: 70;
40 from written test,
15 for project, and 15 for assignments.

Grades: 30 for 3, 42 for 4, and 56 for 5.

Allowed material: All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.

Examiner: Lars Wanhammar.

Responsible teacher: Robert Hägglund.
Tel.: 0705 - 48 56 88.

Correct (?) solutions: Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Assignments

1. Large-signal analysis

The three amplifiers shown in Figure 1.1 are commonly used in for example operational amplifiers. In this exercise the analysis of these amplifier is considered. All transistor should operate in the saturation region.

- a) Determine the width-over-length ratios for the two transistors in Figure 1.1a for a given output range OR , $V_{out,DC} = (OR_{min} + OR_{max})/2$, and current through the transistors I . Do not neglect the channel-length modulation nor the body effect. (2p)
- b) Determine the width-over-length ration of the common drain circuit shown in Figure 1.1b for given valus of the voltages $V_{in,DC}$, $V_{out,DC}$, V_{bias} , and the current through the transistors I . Do not neglect the channel-length modulation nor the body effect. (2p)
- c) Determine the input range of the common-drain amplifier shown in Figure 1.1b for the same parameters as in exercise 1b. Neglect the channel-length modulation, but not the body effect. (This exercise can be solved even though exercise 1b is not solved.) (2p)
- d) Determine the output range of the amplifier shown in Figure 1.1c as a function of the bias voltages, current, power supply voltage, and device parameters. (2p)

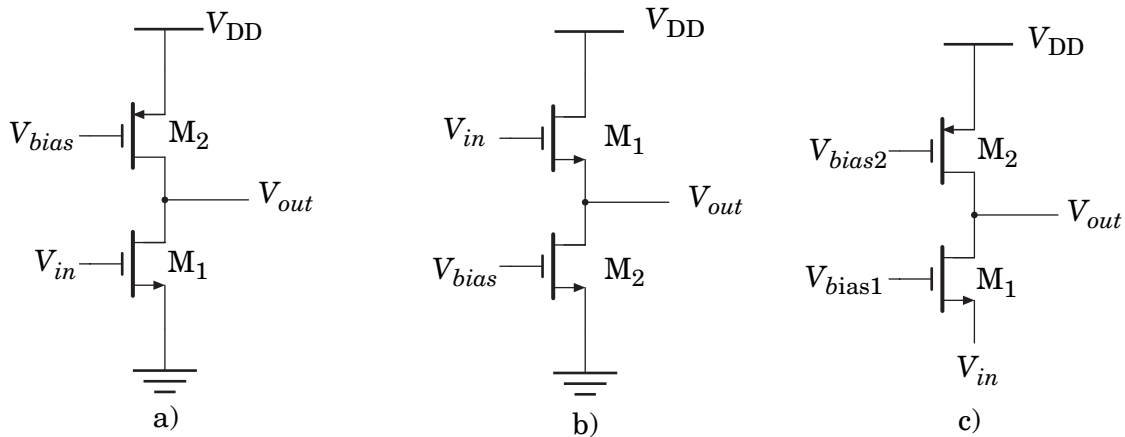


Figure 1.1 Simple amplifiers commonly used as building block in op amps.

2. Small-signal analysis

The transistor in the circuit shown in Figure 2.1 is biased in the saturation region. Neglect the influence of all internal parasitics in the transistor.

- a) Compute the small-signal transfer function of the circuit shown in Figure 2.1, $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect. (1p)
- b) How will the DC gain, unity-gain frequency and the first pole be changed when the supply current, I , increases (i.e., when the DC input voltage level is increased). Assume that $g_{ds} \ll 1/R$. (2p)
- c) The resistor and the transistor generate thermal noise. Compute the input referred noise power within the unity-gain frequency band, i.e., $\omega_u = g_{m1}/C_L$, of the circuit shown in Figure 2.1 caused by the thermal noise. Neglect the channel-length modulation. (4p)
- d) How should the amplifier be designed to have a small input referred noise power within the unity-gain frequency? (1p)

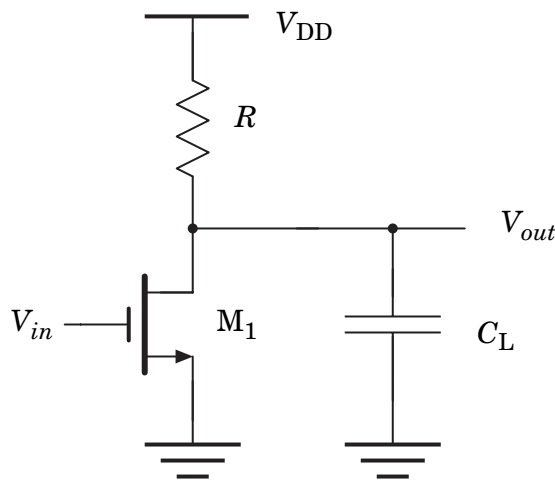


Figure 2.1 An amplifier structure implemented using CMOS transistors.

3. Operational amplifiers

The trend is to decrease the minimum feature sizes in CMOS process. This causes the low-frequency gain of a single transistor to decrease. If high DC gain is required in a modern process, a multi-stage amplifier may be an appropriate choice. In this exercise, the small-signal equivalent of the differential response of a three-stage amplifier shown in Figure 3.1a is considered. The common-mode gain is zero. Throughout this exercise, assume that $C_L \gg C_1 = C_2 = C$, $R_1 = R_2 = R_L = R$.

- Derive the transfer function from the input to the output of the circuit shown in Figure 3.1a, i.e., $H(s) = V_{out}(s)/V_{in,diff}(s)$. (1p)
- Compute an approximative expression for the unity-gain frequency given that the higher-order poles are located at much higher frequency than the unity-gain frequency. Motivate your solution. (1p)
- The amplifier is connected in a close-loop configuration as shown in Figure 3.1b. For such a circuit, the transfer function can be given in the form

$$H(s) = \frac{A(s)}{1 + \beta A(s)} \tag{3.1}$$

where β is the feedback factor and $A(s)$ is the gain of the amplifier. Determine the feedback factor for the circuit shown in Figure 3.1b.

- For the circuit in Figure 3.1b compute an analytic expression for the factor K , which relates the second pole p_2 and the unity-gain frequency ω_u , in the expression $p_2 = K \cdot \omega_u$ in order to obtain a specific phase margin, i.e., compute $K = f(\phi_m)$. Assume that at the unity-gain frequency the first pole has caused a -90 degree phase shift at ω_u . (2p)
- Compute the value of the K factor to obtain a phase margin of 45 and 75 degrees, respectively. (2p)
- Is the approximation in 3b good for the two cases in exercise 3e? Motivate your answer carefully. (1p)

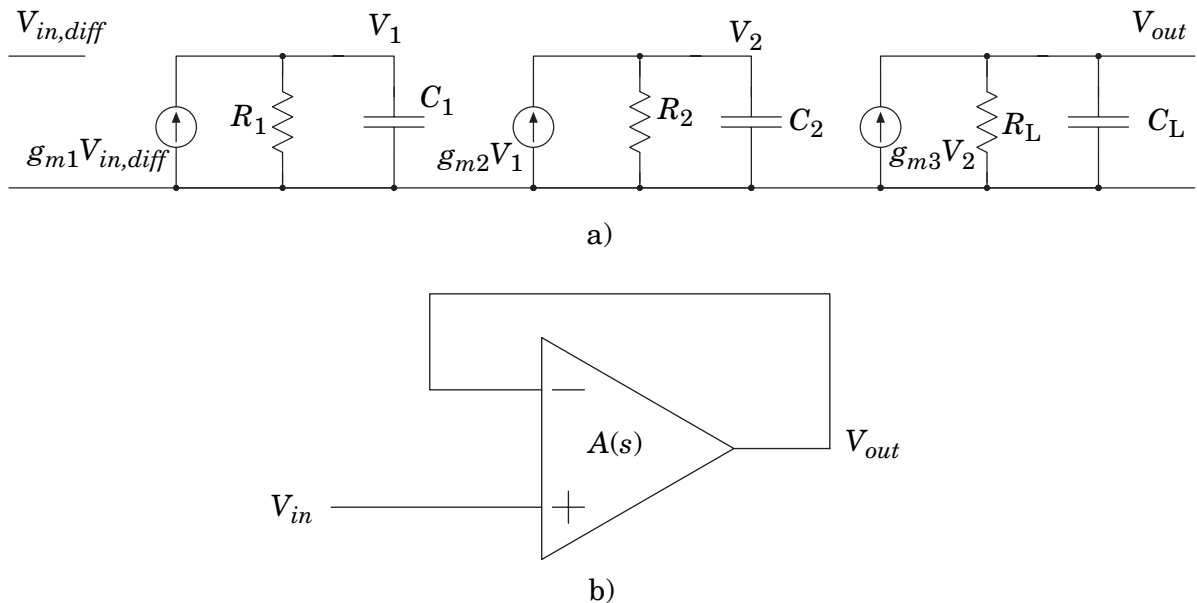


Figure 3.1 a) A small-signal model of the differential gain of a three-stage amplifier. b) The three-stage amplifier in a feedback configuration.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time $t, t + 2\tau, t + 4\tau$, etc. is shown in Figure 4.1. Assume that the input signal are constant between clock phase 1 and 2, i.e., $V_1(t) = V_1(t + \tau)$.

- Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_1(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal. (4p)
- Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)
- Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA suffers from an offset voltage, V_{os} . (3p)

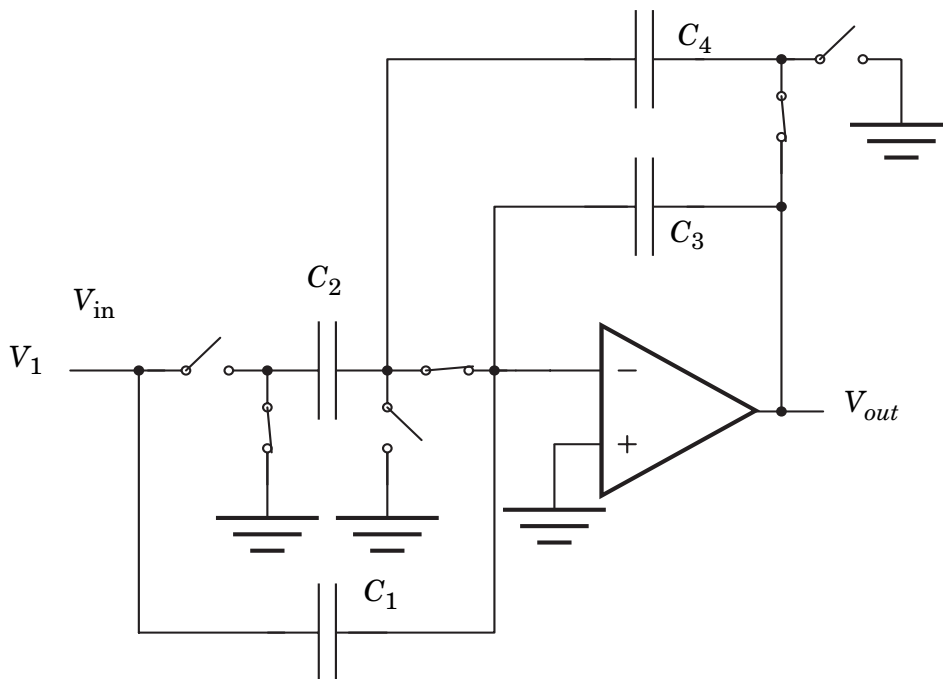


Figure 4.1 A switched-capacitor circuit in clock phase 1.

5. A mixture of questions

- Draw the small-signal model and compute the DC gain, input and output resistance for the circuit shown in Figure 5.1. (4p)
- State advantages and disadvantages of using switched capacitor filters compared with active-RC filters. (1p)
- State benefits and drawbacks of using a fully differential compare with a single-ended circuit structure in an integrated analog circuit. (2p)
- Why is it uncommon to use the minimum channel length and channel widths for a transistor in an analog design. (1p)

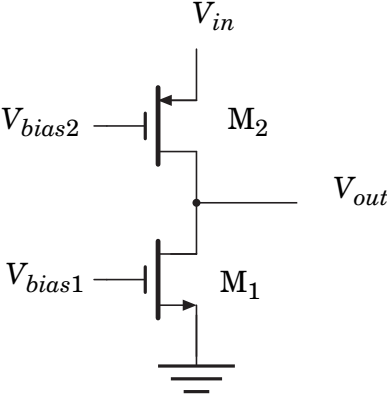


Figure 5.1 An amplifier realized using CMOS transistors.

Transistor formulas and noise

CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

All regions:

$$V_T = V_{T,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$