Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	January 12, 2004
Time:	8 - 12
Place:	Garn
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercises

1. Large-signal analysis

The circuit shown in Figure 1.1 is to be analyzed using large-signal analysis. Throughout this exercise assume that the power supply voltage is much larger than the threshold voltages, i.e., $V_{DD} \gg V_{T1} + V_{T2}$. Further, neglect the channel-length modulation.

a) Assume that the transistors M_1 and M_2 are saturated. Express V_{out} as a function of V_{in}. (2p)

b) Determine the possible range of the voltage V_x in order to ensure that the transistors M_1 and M_2 are saturated. The DC voltages at the input and output should is set to $V_{in,\,DC} = V_{out,\,DC} = V_{DD}/2$. (4p)

c) For matching purposes, the resistance values are chosen equal, i.e., $R_1 = R_2 = R$. Further, $V_{in,\,DC} = V_{out,\,DC} = V_{DD}/2$. Select a suitable value of the voltage V_x and determine the width over length ratio as a function of the resistance, R, the power consumption, power supply voltage, and transistor parameters. (2p)

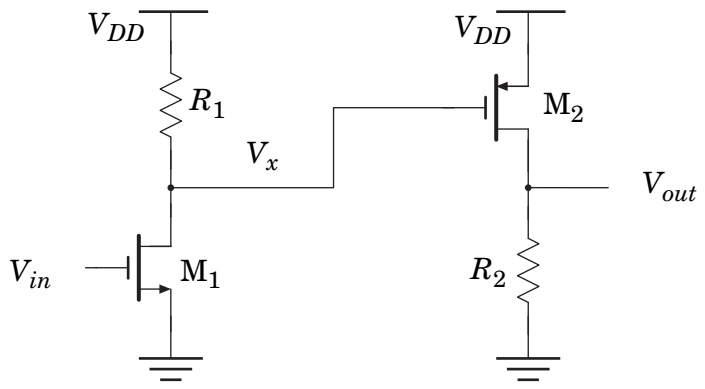

Figure 1.1 A simple amplifier circuit.

2. Small-signal analysis

The circuit shown in Figure 2.1 is to be used in an amplifier circuit. Assume that the transistors are saturated. Do not neglect the bulk effect.

a) Compute the transfer function from the input to the output of the circuit. Determine approximative expressions for the DC gain and possible poles and zeros. Assume that $C_L g_{ds} \gg C_{gs4} g_m$. (4p)

b) State two ways to increase the phase margin of this circuit. (2p)

c) Compute the output resistance of the circuit. (2p)

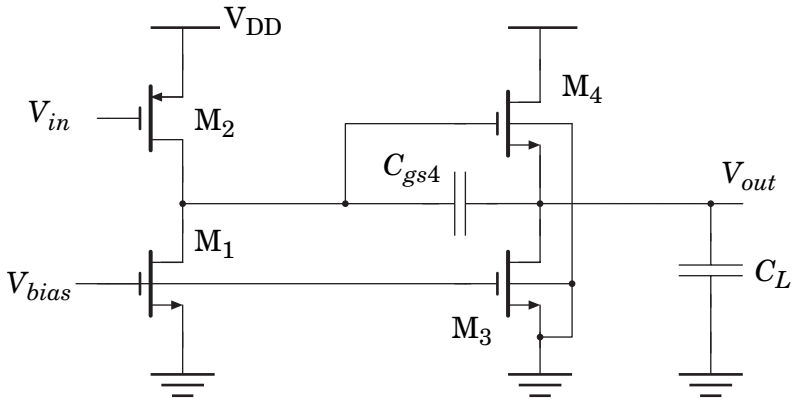

Figure 2.1 A CMOS circuit.

3. Analysis of operational amplifiers in a context

The transfer function

$$H(s) = -\left(\frac{a_0 + a_1 s + a_2 s^2}{b_0 + b_1 s + s^2}\right) \tag{3.1}$$

is to be realized in an integrated circuit. A signal-flow graph of a possible implementation is shown in Figure 3.1. The coefficients a_i are positive.

a) Express a_i and b_i as a function of α_j and β_j. Are there any restrictions of the α and β coefficients in order to have a stable filter? (2p)

b) Realize a stable transfer function using the signal-flow graph in Figure 3.1. The implementation should contain only resistors, capacitors, and operational amplifiers. Further, identify the coefficients a_i and b_i in terms of resistance and capacitance values. (6p)

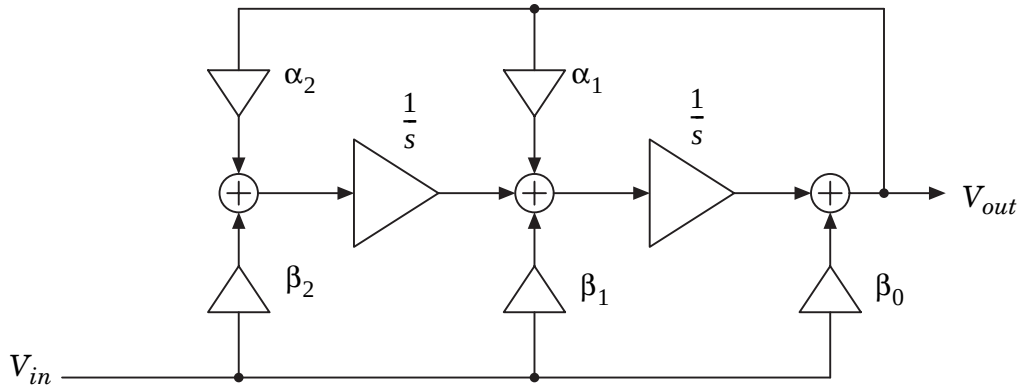

Figure 3.1 A signal-flow graph that can be used to realize a transfer function.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure 4.1.

a) Determine the output voltage as a function of the input voltage, $V_{out}(z) = f(V_{in}(z))$ for clock phase 1 of the circuit shown in Figure 4.1. Assume that the operational amplifier is ideal except that it suffers from an offset voltage. (6p)

b) Is the circuit insensitive of capacitive parasitics. Motivate for all parasitic capacitors in the circuit. (2p)

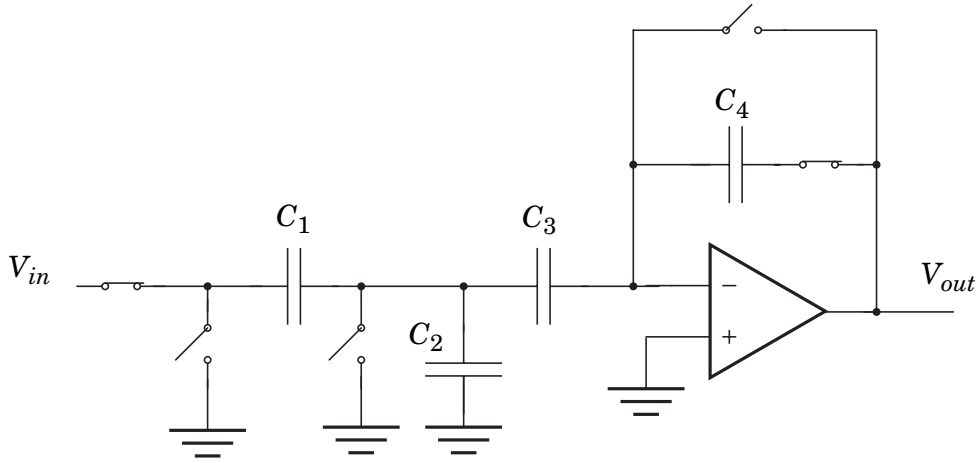

Figure 4.1 A switched-capacitor circuit.

5. A mixture of questions

a) Compute the input-referred noise spectral density of the circuit shown in Figure 5.1. Assume that the resistor and the saturated transistor generate thermal noise. (2p)

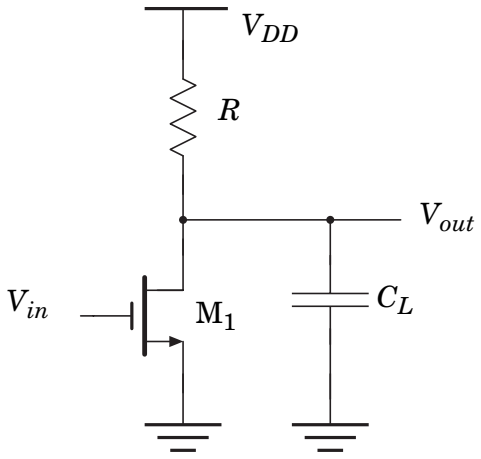

Figure 5.1 A noisy circuit.

b) Which of the accumulator circuits in Figure 5.2 is preferred to be used in an integrated filter? Assume that the input voltage is sampled according to $V_{in}(t + \tau) = V_{in}(t + 2\tau)$. Motivate your answer carefully. (1p)

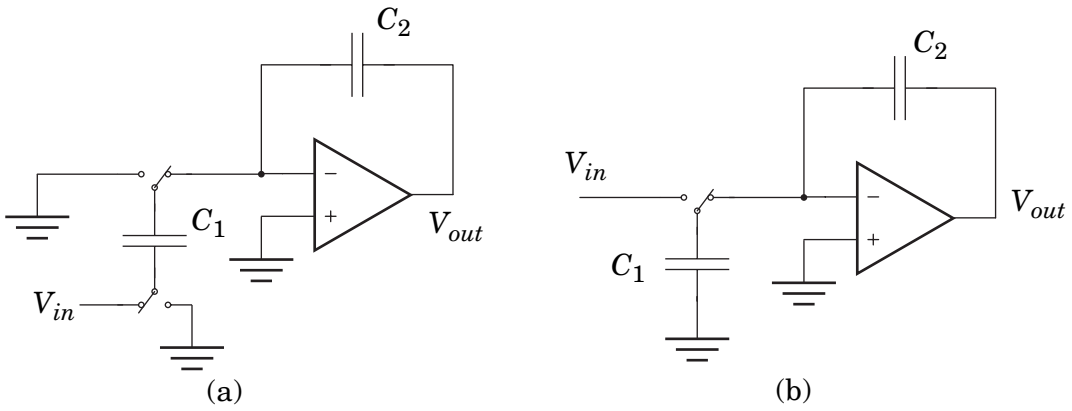

Figure 5.2 Two switched-capacitor circuits.

c) State two advantages of using an oversampled digital-to-analog converter instead of a Nyquist-rate converter. (2p)

d) What are the benefits and drawbacks of using a fully-differential compared to a single-ended operational amplifier? (3p)

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$