Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	May 28, 2003
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large-signal analysis

The circuit in Figure 1.1 is a commonly used structure when designing analog circuits. In all following exercises assume that transistor M1 is biased in saturation. Also assume that the *W/L* ratio of transistor M2 is X times larger than that of transistor M1, i.e., $W_2/L_2 = XW_1/L_1$.

a) Derive the output voltage as a function of the factor X, i.e., $V_{out} = f(X)$, when transistor M2 is saturated. Express the output voltages in terms of the current I_0 and transistor design parameters, but not voltages other than the power supply voltage. (1p)

b) Derive the output voltage as a function of the factor X, i.e., $V_{out} = g(X)$, when transistor M2 is operating in the linear region. Express the output voltages in terms of the current I_0 and transistor design parameters, but not voltages other than the power supply voltage. (4p)

c) Determine for which value of X transistor M2 switches from operating in the saturation region to the linear region. (2p)

d) Sketch the output voltage as a function of the X, i.e., $V_{out} = h(X)$, for $X > 0$. (1p)

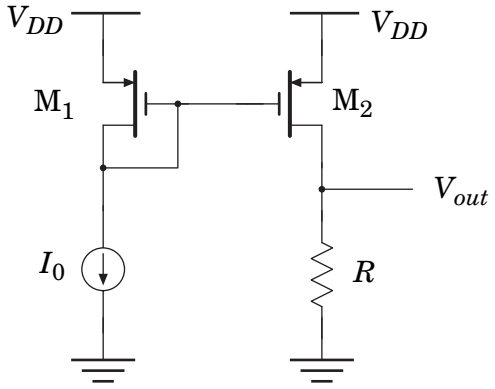

Figure 1.1 A simple current mirror.

2. Small-signal analysis

The circuit in Figure 2.1 is going to be implemented in a CMOS process. The parasitic of interest is the gate-source capacitor. The feedback amplifier has a gain of $-A$ where A is positive and $A \gg 1$. Further, assume that $C_{GS,2} \ll C_L$.

a) Derive the transfer function, i.e., V_{out}/V_{in}, of the circuit shown in Figure 2.1. Do not neglect the bulk effects. (2p)

b) Derive expressions for the DC gain, first pole, second pole, possible zeros, and the unity-gain frequency in terms of I_1, I_2, W_1, W_2, L_1, and L_2. Neglect the influence of the bulk effect. (4p)

c) How is the phase margin effected if the bias current I_1 is increased, i.e., how is the phase effected at the unity-gain frequency of the circuit?(2p)

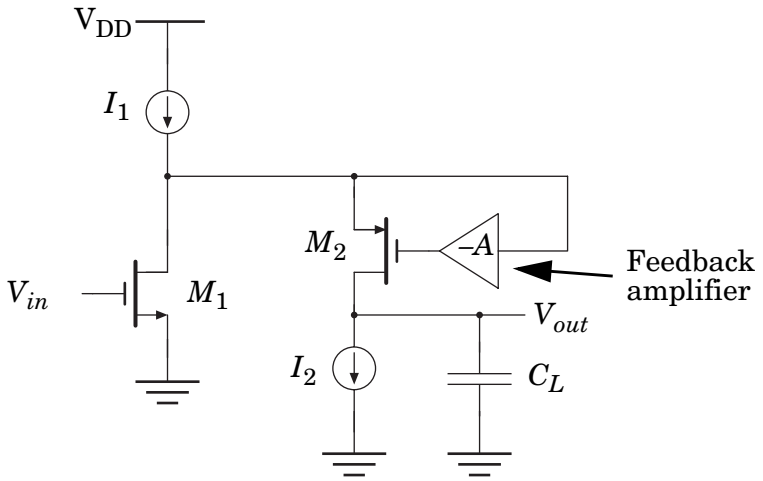

Figure 2.1 A CMOS circuit.

3. Noise analysis

An operational amplifier is used in a CMOS circuit. Assume that the OPamp is ideal.

a) Derive the transfer function of the circuit shown in Figure 3.1. (3p)

b) Derive the equivalent thermal output noise spectral density of the circuit. Assume that the operational amplifier is noiseless while the resistors generate thermal noise according to $V_R^2 = 4kTR$. (5p)

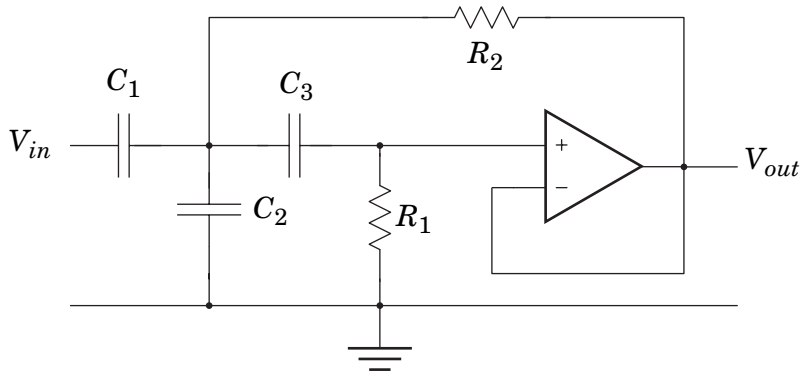

Figure 3.1 An operational amplifier configuration.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure 4.1. The input signal is sampled according to $V_{in}(t) = V_{in}(t + \tau)$. Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA is ideal. (8p)

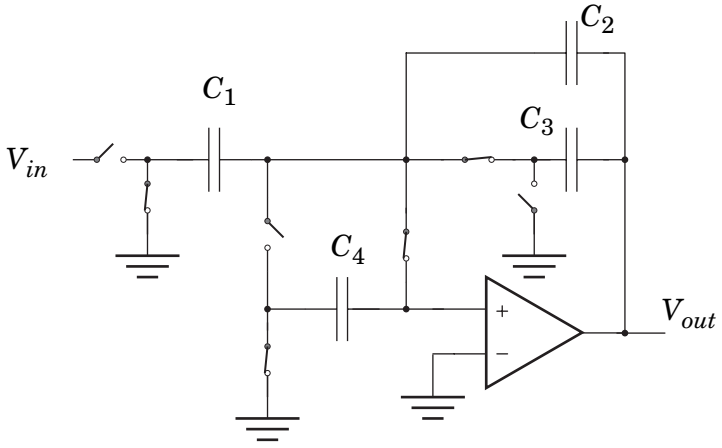

Figure 4.1 A switched-capacitor circuit.

5. A mixture of questions

a) You have designed and fabricated a digital-to-analog converter with 62dB SNR, where the noise power is dominated by the quantization noise. The application requires 86dB SNR. How can you increase the SNR of the data converter? (3p)

b) Derive expressions for the common-mode and the output ranges of the circuit shown in Figure 5.1 in terms of currents, I_{D5} and I_{D3}, and transistor parameters. The amplifier circuit is symmetric with respect to the transistor sizes, i.e., $W_1/L_1 = W_2/L_2$ and so on. (4p)

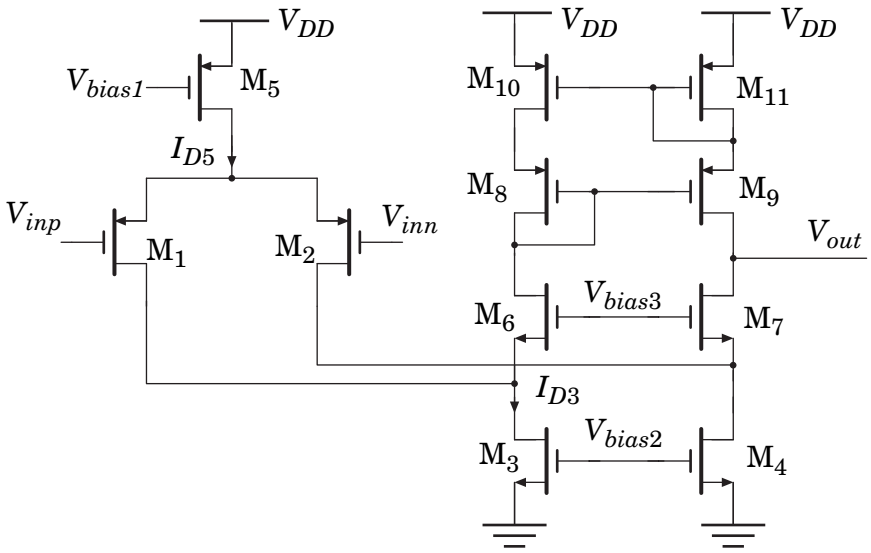

Figure 5.1 A CMOS amplifier structure.

c) A three terminal switch, Figure 5.2(a), is realized with two PMOS devices, Figure 5.2(b), in an SC circuit. The gates of the transistors are connected to the clocks ϕ_1 and ϕ_2, respectively. The waveforms for two different types of 2-phase clocks are shown in Figure 5.2(c) and (d), where ϕ_1 is solid and ϕ_2 is dashed. Which of these two 2-phase clocks ((c) or (d)) should be used in order to guarantee a good operation of the SC circuit. Motivate your answer carefully. (1p)

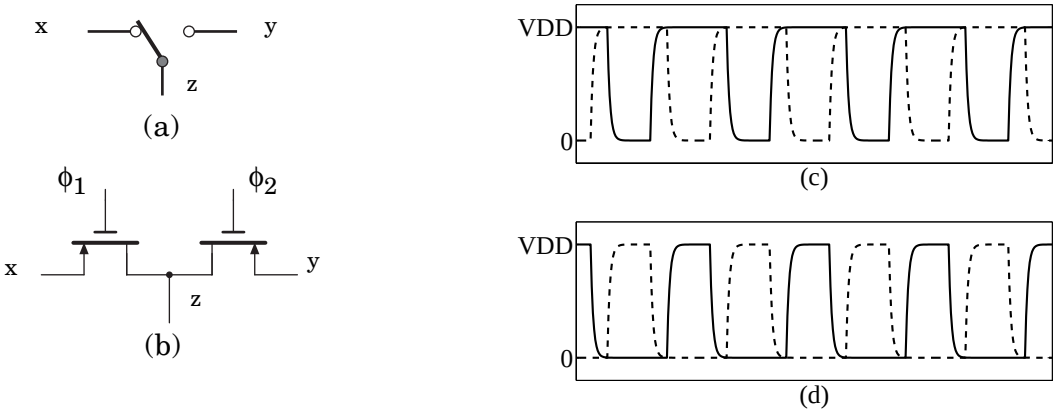

Figure 5.2 (a) A schematic view of a switch within an SC circuit. (b) Transistor implementation of the switch. (c) and (d) two different 2-phase clocks.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$