Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	June 3, 2002
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

NOTE: Exercise 6 is only for those that have taken the course before 2002, and have not handed in more than one assignment during the course.

Exercise

1. Basic building block

In an operational amplifier a buffer at the output is needed to increase the output conductance of the amplifier and thereby be able to drive resistive loads. The buffer is shown in Figure 1.1. In this exercise neglect the influence of the channel length modulation.

a) Derive a large signal expression for the output voltage as a function of the input voltage. Assume that all transistors are operating in the saturation region. (2p)

b) Express the first pole as a function of the bias voltage, V_{bias}. (3p)

c) What is the maximum value of the pole when both transistors are operating in the saturation region? (3p)

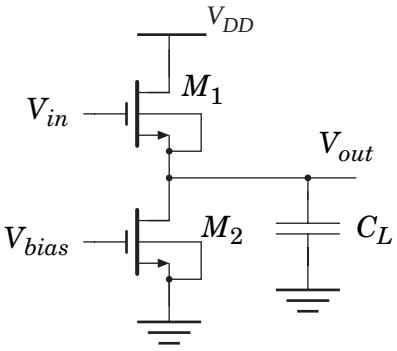

Figure 1.1 A CMOS gain stage.

2. Small signal analysis

A new type of transistor has been developed. The approximate expression for the transistor is as follows:

$$I_1 = I_2 / V_{AC} \tag{2.1}$$

$$I_2 = I_{BS} e^{\frac{V_{AC}}{V_T}} \left(1 + \frac{V_{BC}}{K}\right) \tag{2.2}$$

$$I_3 = I_1 + I_2 \tag{2.3}$$

where I_{BS} and K are process dependent constants and $V_T = \frac{kT}{q}$.

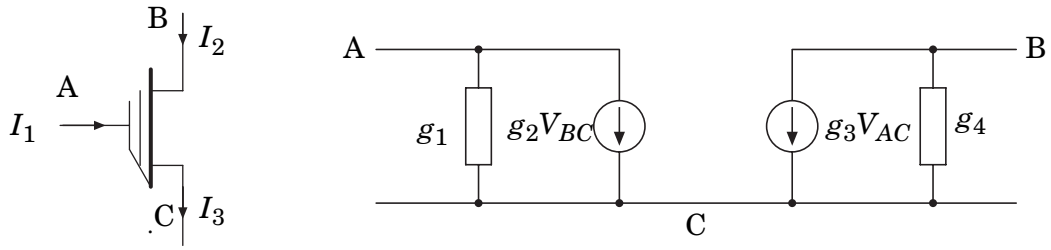

Figure 2.1 A new type of transistor a) the transistor symbol b) the small signal model.

a) Derive a small signal model equivalent to the one shown in Figure 2.1 for the transistor. (7p)

b) Is it good to use this transistor as input transistor in an operational amplifier that are going to be used in a switched capacitor circuit? Motivate your answer carefully. (1p)

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3. Operational amplifier / Operational transconductance amplifier

An operational amplifier is used in a feedback configuration shown in Figure 3.1. The transfer function of the amplifier is given by

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{3.1}$$

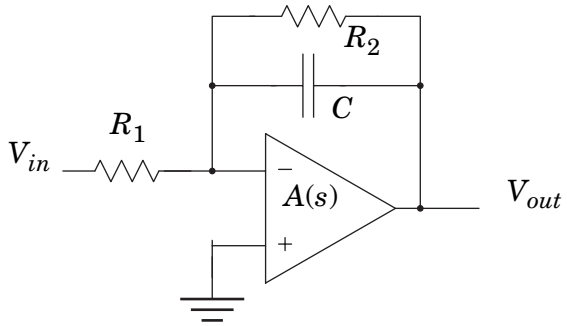

Figure 3.1 A operational amplifier in a feedback configuration.

a) Find an expression for the feedback factor, β. Sketch the magnitude and

phase responses of the loop gain as a function of the frequency. Assume that $R_2 = 10R_1$ and that $R_2C = 0.5/p_1$ (5p)

b) Assume that the last stage, a common drain gain stage, in the operational amplifier is the stage that limits the slew rate. How large must the current through the last stage be to have a slew rate of $SR = 40V/\mu s$ (1p)

c) In the circuit shown in Figure 3.1 the capacitor and the resistor forms the time constant in the building block. Process and temperature variations yields a large component spread, low matching of the time constant. Assume instead that we can form the time constant by a capacitor ratio. State two ways to improve the matching of the two capacitors where $C_2 = C_1 = 50\text{pF}$. (2p)

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4. Switched capacitor circuit

A switched capacitor circuit in clock cycle 1 is shown in Figure 4.1.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit shown in Figure 4.1, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) What are the benefits and drawbacks of an SC circuit compared to a continuos time circuit? (2p)

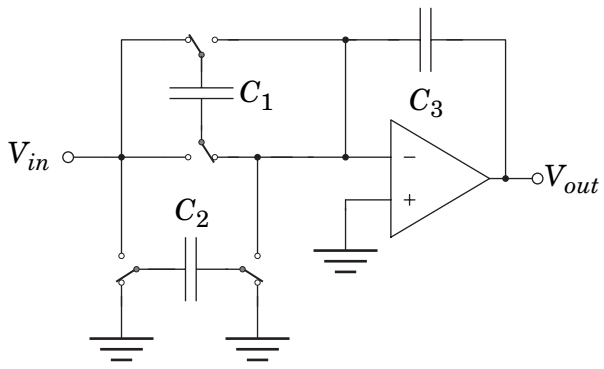

Figure 4.1 A switched capacitor circuit.

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5. A mixture of questions

a) Linus has a 10-bit DA converter och needs a SNR of more than 65dB. Propose one way to achieve this SNR. (2p)

b) We have designed a folded cascode operational transconductance amplifier but the Common-Mode Rejection Ratio is too low. This comes from the fact that when the input common-mode voltage is increased the current generated by current source transistor will increase. How can we decrease this sensitivity to common-mode signals? (1p)

c) In mixed signal designs it is common that the noise from the digital circuits is passed via the substrate to the analog circuits. Assume that we have a common source amplifier with resistive load that are close to a digital switching network. We assume that the switching noise can be modelled as a white noise source with the spectral density of $V_n^2 = S_{sub}$. Derive the equivalent input referred noise spectral density. The only noise to be considered except the substrate noise is the thermal noise of the transistor and the resistor. (3p)

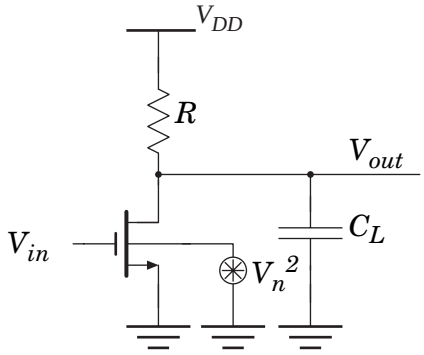

Figure 5.1 A noisy common source amplifier with resistive load.

d) State two ways to decrease the input noise power in exercise c) and thereby the SNR (if the input signal power is constant) by changing two different relevant design parameters? What will happen to the DC gain of the circuit in both cases? Assume that the resistance R is much smaller than the output resistance of the transistor. (2p)

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6. Extra exercise

NOTE: This exercise is only for the students that have taken the course before 2002 and not handed in three assignments during the course.

The circuit shown in Figure 6.1 is to be used in a analog signal processing circuit.

a) Draw a small signal model of the amplifier, neglect the influence of the parasitic capacitanses introduced in the transistors. (1p)

b) The transfer function of the amplifier can be computed to

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}(g_{m3}+g_{ds3})\alpha}{(g_{ds4}g_{ds5}+\alpha sC_L)(g_{ds3}+g_{m3})+(g_{ds1}+g_{ds2})(g_{ds4}g_{ds5}+(g_{ds3}+sC_L)\alpha)}$$

where $\alpha = g_{ds4}+g_{ds5}+g_{m4}$ when the body effect is neglected.
Approximate the transfer function and find simple expressions for the DC gain, first pole, and the unity-gain frequency. (3p)

c) What will happen to the DC gain and the first pole if we ...
...increase the current through transistor M_2.
...increase the size of the load capacitor.
...insert a gain boosting stage to transistor M_3 and M_4
Assume that the increased sizes does not change the operation region of the transistors. (6p)

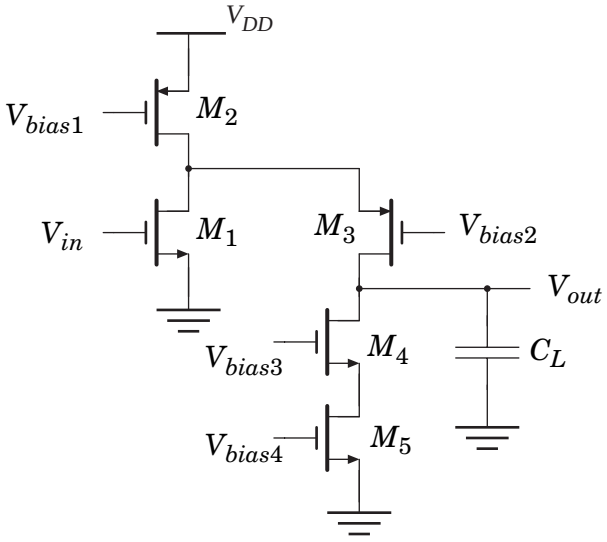

Figure 6.1 A CMOS amplifier stage.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$