Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	May 31, 2001
Time:	8 - 12
Place:	Garnisonen
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	No LapTops. No text book in analog design such as Johns & Martin *"Analog Integrated Circuit Design"*. No dedicated compedia such as Eriksson *"Aktiva RC-filter och SC-filter"* or *"Exempelsamling"*. Pocket calculators are allowed. Written material, downloaded web-material, except old exams are allowed.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed June in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

This exam covers nearly the whole course except the filter chapters. Our advise to you is to start by reading through the exam and then begin to solve the exercises that you are familiar with.

Exercise

1. Basic CMOS building blocks

Consider the circuit in Figure 1.1 where only the load capacitance and the parasitic capacitance between gate and source of transistor M4 are of importance. Assume that $C_{gs} \ll C_L$.

a) Determine the gain and poles of the circuit. (3p)

b) Explain the use of each building block. (2p)

c) How do we increase the unity-gain frequency without increasing the total power dissipation? What will then happen with the gain of the circuit? (2p)

d) How do we increase the output swing without changing the unity-gain frequency? What will happen with the gain of the circuit? (2p)

e) Assume that the we like to use building blocks, like the one shown in Figure 1.1, to increase the output resistance of a common-source gain stage with cascodes. How are they connected to the common-source stage? Explain with a schematic of the gain-boosted circuit where only transistors are shown together with a short text. (4p)

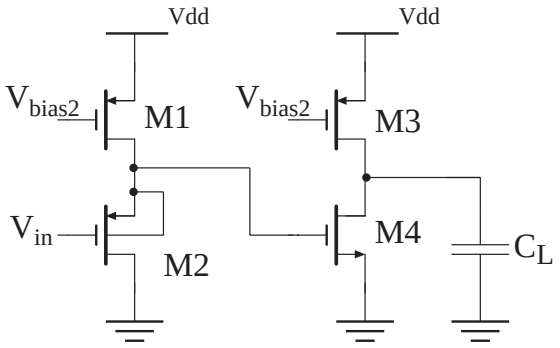

Figure 1.1 Gain-boosting circuit.

2. Operational transconductor amplifiers

The power supply of the circuit are 3.3V and 0V respectively. Assume that all internal parasitics are small.

a) Explain the function of every transistor in Figure 2.1. (2p)

b) Derive the common-mode range, CMR, and the output range, OR, of the circuit. Propose **two** ways to increase the output range. (3p)

c) Propose one way to increase the DC-gain. What will then happen with the unity-gain frequency and the phase margin? (3p)

d) The amplifier is connected as in Figure 2.2. What will the output voltage from the amplifier look like when the input voltage is $V_{in} = V_{DC} + 0.1\sin(2\pi 100 \cdot 10^3 t)$? Assume that $V_{CMR,\,min} < V_{DC} < V_{CMR,\,max}$ (2p)

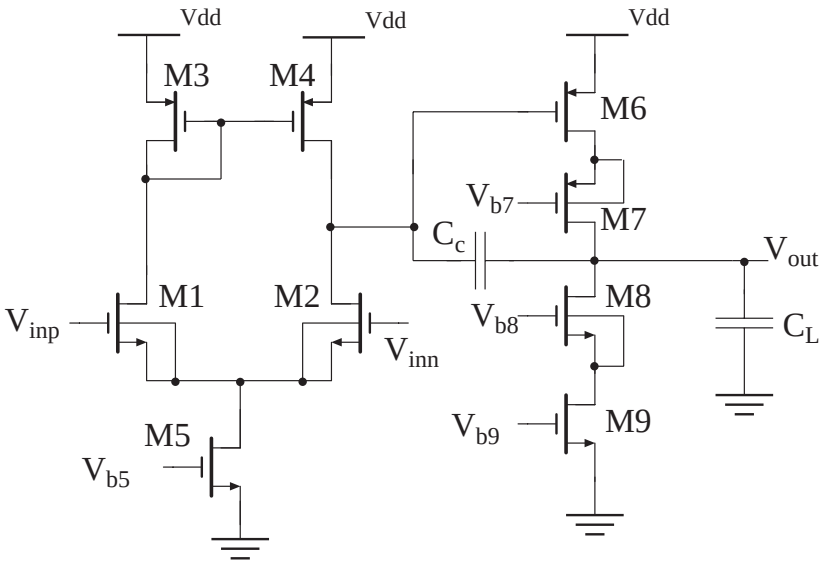

Figure 2.1 An operational transconductor amplifier.

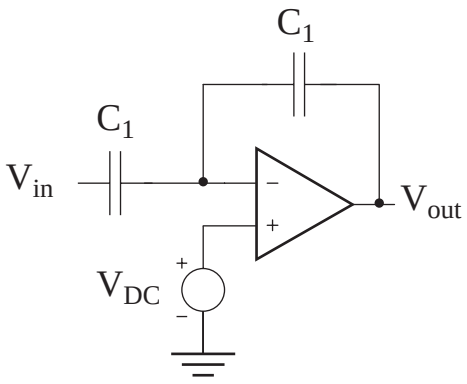

Figure 2.2 Operational transconductance amplifier in a feedback configuration.

3. Noise

Assume that transistors M1 and M2 generate thermal noise only. Furthermore, I_{bias1} and I_{bias2} can be seen as DC current sources. Assume that $C_{gs} \ll C_L$.

a) Derive the total output noise power. (3p)

b) Derive the noise voltage that can be referred to the input. (2p)

c) Propose one way to increase the maximum signal to noise ratio, SNR in the circuit shown in Figure 3.1. What will happen to the DC-gain, unity-gain frequency, bandwidth and the phase margin of the circuit? (2p)

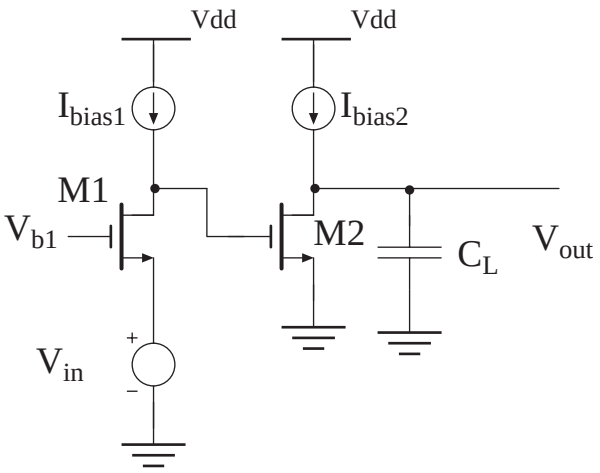

Figure 3.1 The noisy circuit.

4. Switched capacitor circuits

Assume that the operational amplifier is ideal except that it has an input offset voltage.

a) Find the transfer function form V_1 to V_2 in Figure 4.1. (2p)

b) Is the circuit insensitive to parasitics? (1p)

c) Sketch (sw. skissera) a typical output voltage, V_2, over 5 clock periods. Assume a DC-input voltage. (2p)

d) What will be the impact of the circuit if a capacitor is connected between node X and ground? (2p)

Assume that the operational amplifier ideal except for a finite-gain, A, and an input offset voltage.

e) What is the transfer function? (3p)

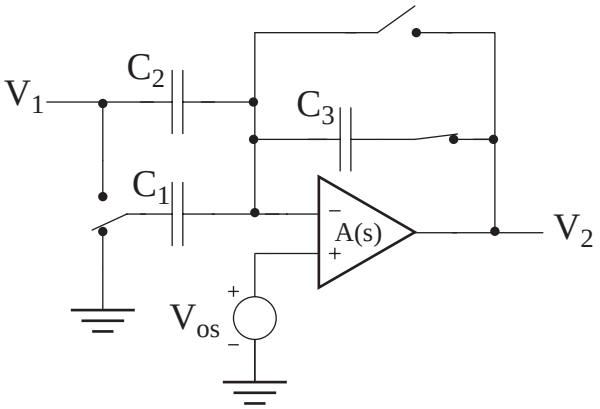

Figure 4.1 The switched capacitor circuit.

5. A mixture of questions

a) In the course we have discussed matching of transistors. What do we mean by matching? Describe **three** different ways to increase the matching between two transistors. (2p)

b) Explain the concept of oversampled analog-to-digital or digital-to-analog converters. What are the advantages and the disadvantages of an oversampled converter compared to a Nyquist-Rate converter? (2p)

c) Describe the function of a common-mode feedback circuit. Explain the function of the circuit in Figure 5.1. How can it be connected to the operational transconductor amplifier in Figure 2.1, if it was a fully differential gain stage? (2p)

d) Derive the possible input and output voltages of the circuit in Figure 5.2a. What type of circuit is it? (2p)

e) Derive the power supply rejection ratio, PSRR, from the positive supply of a common source amplifier loaded by an active load, see Figure 5.2b. Propose a way to increase the PSRR. (2p)

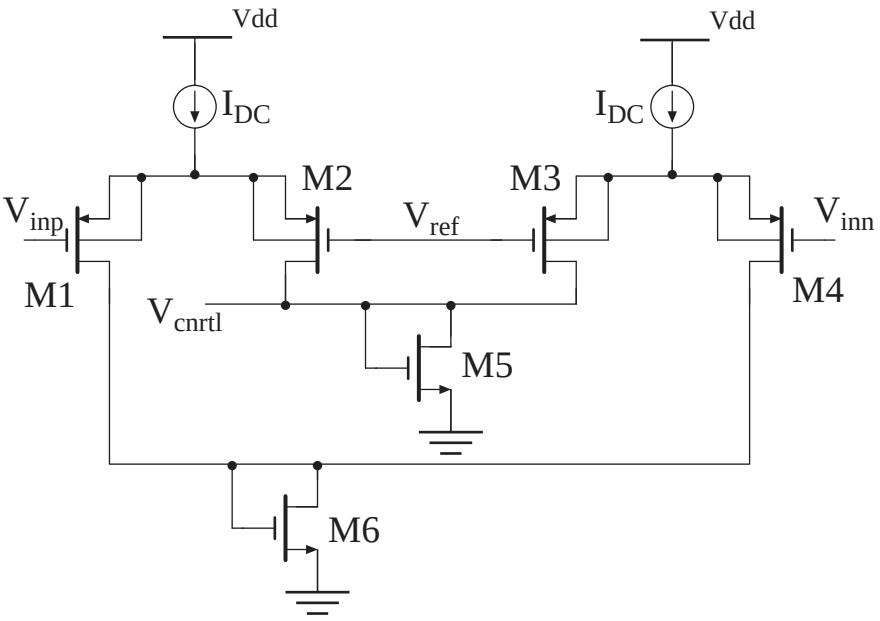

Figure 5.1 A common-mode feedback circuit.

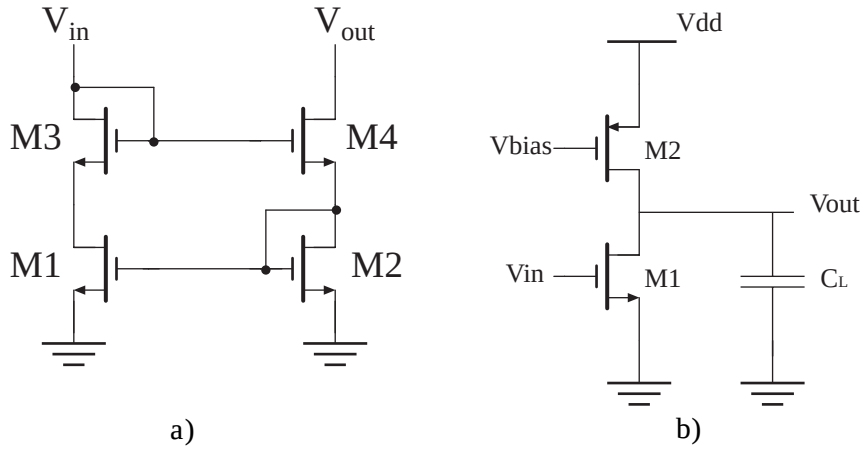

Figure 5.2 a) CMOS circuit and b) a common source gain stage.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$