Written Test
TSTE80, Analog and Discrete-time Integrated Circuits

Date	January 18, 2000
Time:	9 - 13
Place:	T2
Max. no of points:	100; 80 from written test, 15 for project, and 5 for oral test.
Grades:	36 for 3, 52 for 4, and 68 for 5.
Allowed material:	Tables as “Physics Handbook”, “Beta”, “TeFyMa”, “Digitala Kretsar - Formula”, etc., are allowed but no text books as for example Johns & Martin *“Analog Integrated Circuit Design”*. Pocket calculators are (of course) allowed but no laptops or similar.
Examiner:	Lars Wanhammar.
Responsible teacher:	J. Jacob Wikner. Tel.: 070-591 59 38.
Correct (?) solutions:	Solutions and results will be displayed January 28 in House B, entrance 29, 2nd floor and on the Internet.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish, German, or English.

Exercise

We want to design a filter, for example a switched-capacitor (SC) filter, and therefore we have to investigate all building blocks of the filter. Consider the exam as a small project assignment where you have to investigate all the details of your design.

a) — The filter specification

We want to design an SC filter for a wideband communication application (ADSL). The specification on the lower frequencies of the output signal at the SC filter output is shown in Figure 1. The sample frequency of the SC filter is chosen to be $16 \cdot 2.204 \approx 35$ MHz. Use the LDI transform and find from tables the required filter order for Butterworth and Cauer filters. Give the cut-off frequencies and attenuation levels that you find. Also sketch the ladder networks and the intermediate stages of your solution.

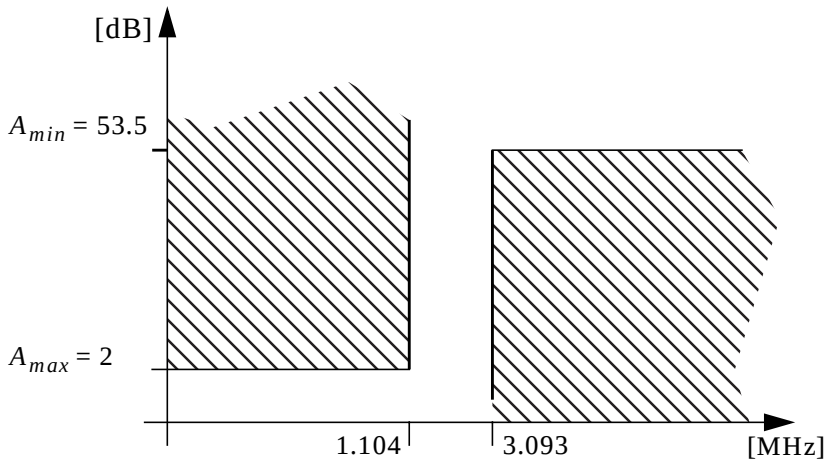

Figure 1 Filter specification.

8 points

b) — The transformations

What are the advantages and disadvantages with the LDI and bilinear transforms?

Ellaborate on sinc weighting of the signal spectrum. How does it affect the signal? How large is the sinc attenuation at the passband edge for the filter in a)?

8 points

c) — The capacitor

Give three different approaches to implement on-chip capacitors. State the advantages and disadvantages with each approach.

Explain “parasitic capacitance” and “fringing capacitance”.

6 points

d) — The filter

First give an example of an SC integrator suitable for filter implementations. Sketch the clock phases needed. What is specific for the clock phases of an SC circuit in general? What does “parasitic insensitive” mean? Is the integrator you have chosen insensitive to parasitics?

Now assume that we use the LDI transform and we want to implement a 3rd order Cauer filter with a structure shown in Figure 2.

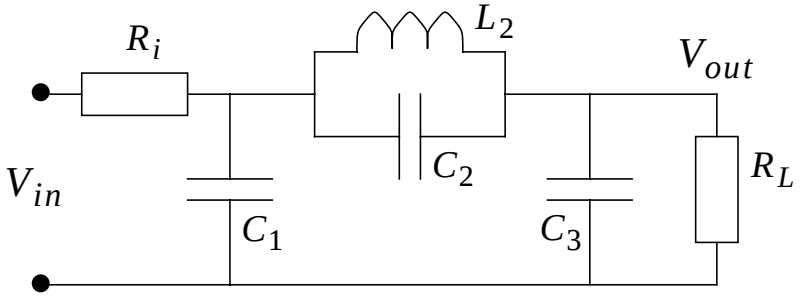

Figure 2 Ladder network for the 3rd order Cauer filter.

Draw a single-ended SC realization of the filter. Be careful with the positions of the switches. Explain how you should choose the component values (capacitor sizes).

Explain (and motivate) the approximations that occur in the filter due to the LDI transform (compare this with what you have written in b, ...)

10 points

e) — The switch

Consider a sampling circuit using an NMOS transistor switch as shown in Figure 3.

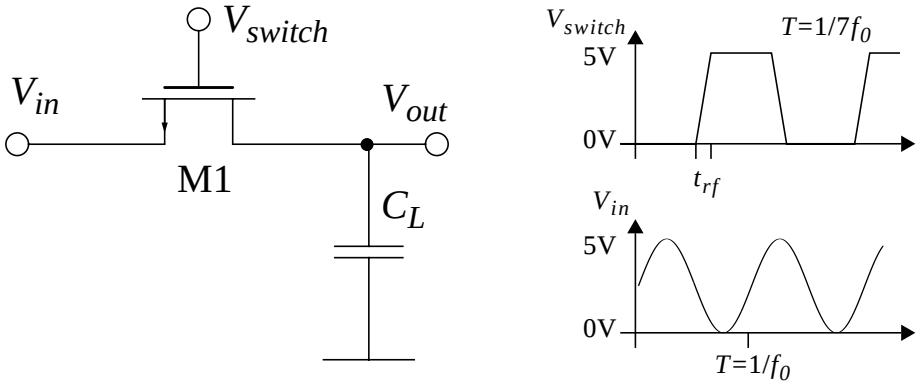

Figure 3 Sampling circuit.

Explain the concept of Clock feedthrough (CFT). What should you do to minimize the CFT?

What is the channel charge and what can be done to reduce the influence of the channel charge injection?

How large is the on-resistance of the switch? What should you do to reduce the on-resistance and how does this affect the CFT and channel charge injection?

Let the input signal be given by a sinusoid as

$$V_{in}(t) = 2.5 \cdot (1 + \sin(2\pi \cdot f_0 \cdot t))$$

The switch signal, $V_{switch}(t)$, is given by a pulse signal that has a duty cycle of 50%, a frequency of $7 \cdot f_0$, and is changing from 0 to 5V with a rise and fall time of $t_{rf} = 1/(21 \cdot f_0)$. Sketch (Sw. "Skissera") the output signal and determine the CFT.

12 points

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f) — Active components

What is the difference between an operational transconductance amplifier (OTA) and an operational amplifier (OP)? When can you use an OTA instead of an OP? For example, why can you use an OTA in an SC filter?

What is the difference between an active transconductor (Gm) and an operational transconductance amplifier (OTA)? When can you use an OTA instead of a Gm?

Sketch the typical transfer characteristics (gain and phase) of the amplifiers when assuming two-pole systems. Denote dominant poles, DC gain, phase margin, unity-gain bandwidth.

When should you choose an SC filter? When should you choose an active-RC filter? When should you choose an Gm-C filter?

12 points

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g) — The operational transconductance amplifier (OTA)

Describe the typical properties of the folded-cascode OTA shown in Figure 4, such as typical output impedance, bandwidth, gain, etc. What functions

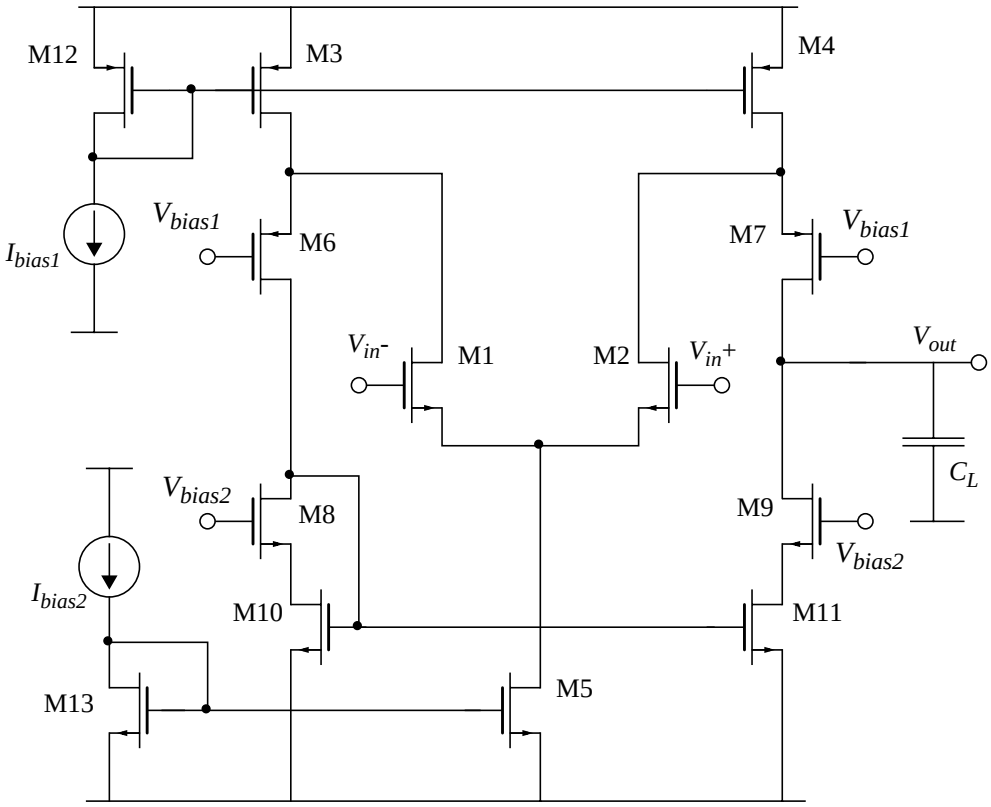

Figure 4 Folded-Cascode OTA.

do the individual transistors have?

How should you size the currents through the branches (I_{bias1} and I_{bias2}) of the OTA for high gain and high slew rate?

What (transistors, etc.) determines the dominant pole and what determines the non-dominant pole?

Give three different approaches to increase the gain of the OTA in Figure 4. State the advantages and disadvantages with each approach.

Give three different approaches to increase the output impedance of the OTA in Figure 4. State the advantages and disadvantages with each approach.

14 points

h) — Noise

Consider the circuit in Figure 5 a). Assume that both transistors are noisy.

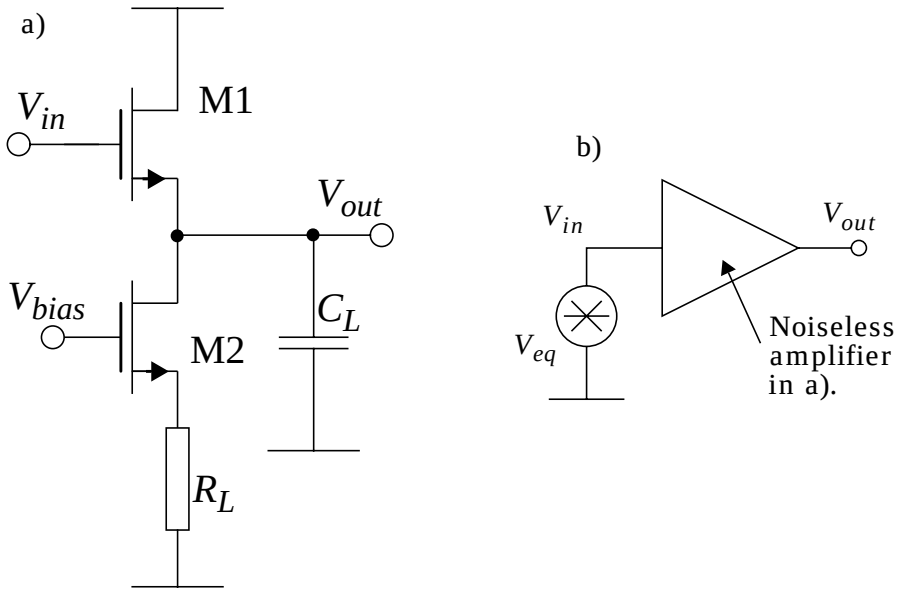

Figure 5 a) CMOS circuit and b) equivalent noise at the input.

Use reasonable approximation, i.e. which noise sources are dominating?

What is the equivalent noise at the input, i.e., find an equivalent noise source at the input as illustrated in Figure 5 b).

Give some examples on how you can reduce the equivalent noise at the input by 50%. Ellaborate on which parameters that actually are possible to change?

What is the total noise power at the output?

Give some examples on how you can reduce the total noise power at the output by 50%. Ellaborate on which parameters that actually are possible to change?

10 points

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_G - V_T - V_D)$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} = \sqrt{\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox} f}$$