Written Test
TSTE80, Analog and Discrete-time Integrated Circuits

Date	August 20, 1999
Time:	14.00 - 18.00
Place:	GARN
Max. no of points:	100; 80 from written test, 15 for project, and 5 for oral test.
Grades:	36 for 3, 52 for 4, and 68 for 5.
Allowed material:	Every possible non-human ones, but no text books as for example Johns & Martin *"Analog Integrated Circuit Design"*. Pocket calculators are (of course) allowed but no laptops or similar.
Examiner:	Lars Wanhammar.
Responsible teacher:	J. Jacob Wikner. Tel.: 070-591 59 38.
Correct (?) solutions:	Solutions will not be displayed before Sept 1. They will be announced in House B, entrance 29, 2nd floor, and published on the Internet.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write in Swedish, German, or English.

The points you achieve on the test will be displayed at around Sept 1, 1999.

Questions

1. Continuous-Time Filters.
Scale and find the new resistance values of the RC-filter in Figure 1.1. The scaling factors should be chosen so that the maximum *(over all frequencies)* absolute voltage gain from the input node to each opamp output node is 1. Also explain why you should scale the filter and how the scaling affects transfer function and performance. Initially, all resistances have the value $R_k = k \cdot 1\Omega$ and the capacitance has the value $C_1 = 1\,\mathrm{F}$.

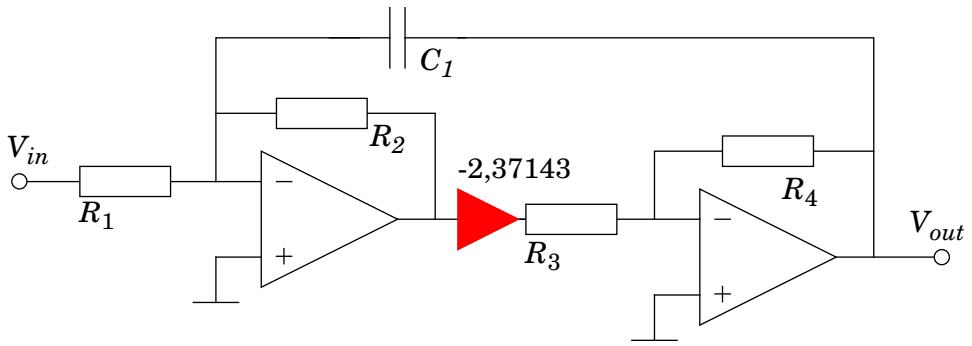

Figure 1.1 Active-RC filter implementation. Note the ideal inverter.

5 points

2. CMOS Circuit and Noise.

Consider the circuit configuration in Figure 2.1. Ignore the body effects of the transistors. The load capacitance, C_L, is the dominant capacitive load to the circuit. The circuit is tuned to have a proper operating point.

a) Describe briefly the properties and usage of transistors M1, M2, M3, M4, and M5, respectively.

b) Find the small signal schematics of the circuit. Make proper approximations.

c) Explain and show two ways to increase the dc gain by a factor two. Also explain what then happens to the unity-gain frequency and bandwidth for the different methods.

d) Describe (not only the formula) the two most dominating noise sources in common analog CMOS circuits for telecommunications.

e) Assume that all transistors are noisy. Derive the *total output thermal noise power* on node V_{out}.

f) How is the SNR affected when you change the bias voltage V_{bias1}?

g) Explain how mismatch between transistor sizes in M1 and M2 influences the transfer function. Discuss some different techniques to improve matching.

h) Find and explain what the slew rate (SR) is in the circuit.

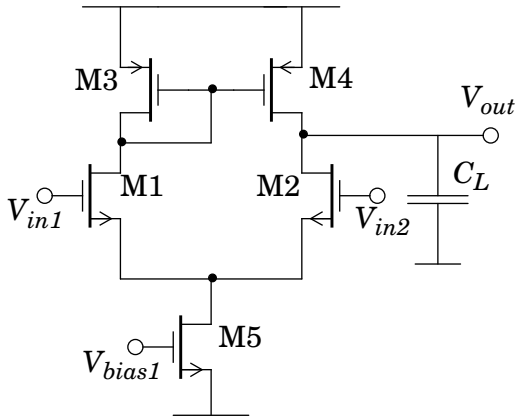

Figure 2.1 CMOS circuit. The supply voltages are 0V and V_{dd}.

35 points

3. Operational Amplifiers and Transconductances.

a) With a macromodel, describe the ideal operational amplifier. What is the input and output impedance? What would be the macromodel for a common CMOS operational amplifier?

b) With a macromodel, describe the ideal transconductor. What is the input and output impedance?

c) Describe the concept of a “Miller integrator”. Hint, what is the “Miller effect”?

d) Assume a dual-pole system:

$$V_{out}(s) = \frac{A_0}{(1 + s/p_1) \cdot (1 + s/p_2)} \cdot V_{in}(s) \qquad (3.1)$$

Describe the relationship between bandwidth, dc gain, unity-gain frequency, and phase margin. Assume that $p_1 \ll p_2$.

e) Derive an expression for the bandwidth of the circuit in Figure 3.1. The opamp transfer function is given by Eq. (3.1), assume that there is one dominant pole in the OP’s transfer function. Express the bandwidth in terms of the bandwidth, unity-gain products, etc., as found in d).

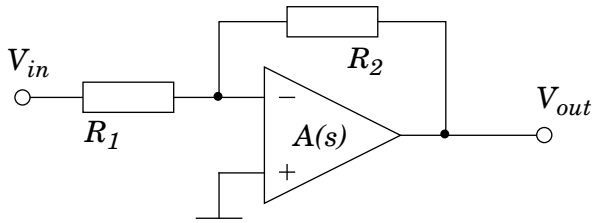

Figure 3.1 Operational amplifier used in a feedback configuration.

15 points

4. Switched-Capacitor Circuits.

Consider the SC circuit in Figure 4.1.

a) Derive the transfer function from inputs to the output of the circuit. What kind of circuit is this?

b) What happens with the transfer function if the operational amplifier has a finite gain? Simply, derive the transfer function if the gain is A. What influences the error?

c) Is the circuit insensitive to parasitics? Explain!

d) Determine the feedback factor for both clock phases. Do not forget the load and parasitic capacitances. Which clock phase determines maximum speed?

e) Explain the concept of clock feedthrough (CFT)

f) What can be said about the matching in this circuit configuration?

g) And again ... describe the difference between the bilinear transform and the lossless discrete integrator transform. Advantages and disadvantages please.

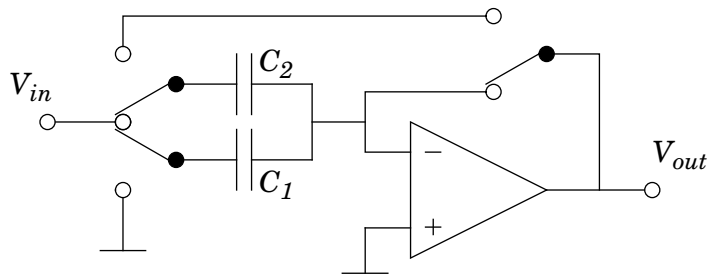

Figure 4.1 Switched capacitor circuit.

25 points

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off: $V_{GS} < V_T$ $\quad I_D \approx 0$

Linear: $V_{GS} - V_T > V_{DS} > 0$ $\quad I_D \approx \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)(2(V_{GS} - V_T) - V_{DS})V_{DS}$

Saturation: $0 < V_{GS} - V_T < V_{DS}$ $\quad I_D \approx \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

Small-signal parameters

Linear region: $g_m \approx (\mu_0 C_{ox})\left(\frac{W}{L}\right)V_{DS}$ $\quad g_{ds} \approx (\mu_0 C_{ox})\left(\frac{W}{L}\right)(V_G - V_T - V_D)$

Saturation region: $g_m = \frac{dI_D}{dV_{GS}} = \sqrt{\mu_0 C_{ox}(W/L)I_D}$ $\quad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is $\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is $\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$